Oversampled ADC based on pulse frequency modulator and TDC

L. Hernández and E. Gutiérrez

Oversampled converters based on voltage controlled ring oscillators are an attractive solution because of their digital implementation and simplicity. However, the voltage-to-frequency conversion of ring oscillators displays a poor linearity. Replacing the ring oscillator by a pulse frequency modulator (PFM) that provides improved linearity at the expense of feedback and analogue amplification is proposed. Compared to the equivalent continuous time sigma–delta modulators, the PFM may be more tolerant to circuit impairments. In addition, the output data of the proposed architecture is a multibit sequence through the use of a time-to-digital converter TDC instead of a Flash quantiser or a multibit digital-to-analogue converter. A high dynamic range can be achieved without severe constraints on analogue mismatch or clock jitter.

Introduction: Analogue-to-digital converters (ADCs) based on voltage controlled oscillators (VCOs) have been under research since the beginning of oversampled data conversion [1]. One of the reasons for the interest in such architecture is a convenient hardware implementation using digital ring oscillators. However, this implementation suffers from distortion due to the nonlinear conversion between voltage and delay in starved inverters [2]. This Letter presents an alternative solution using a pulse frequency modulator (PFM) based on an integrator and a monostable triggered by a threshold voltage. The proposed architecture may extend the advantages of VCO ADCs to applications where the required linearity is unattainable with ring oscillators even if calibration [2] or other linearisation techniques are used [3]. To mimic the behaviour of a polyphase ring oscillator, we propose to implement the monostable with a digital delay line based on inverters. This configuration has the advantage that intemediate taps in the delay line form a time-to-digital converter (TDC) when sampled at the sampling clock. Hence, the VCO output is converted into a multibit sequence.

Pulse frequency modulators: In a VCO-based ADC, the square wave output of a digital VCO is sampled and differentiated afterwards with an XOR gate to produce a noise-shaped sequence [1]. Fig. 1*a* shows an alternative implementation using a PFM. PFMs have been used in instrumentation applications as voltage-to-frequency converters. A PFM generates a pulse train $y(t)$ whose instantaneous frequency $f(t)$ depends on a slow analogue input $x(t)$.

The operation of the PFM of Fig. 1*a* can be explained with the chronogram of Fig. 1*b* that depicts one oscillation cycle. We will assume that the integrator output $V_i(t)$ starts at an initial value V_0 and no pulse is being generated ($y(0) = 0$). If we consider that signal $x(t)$ is defined between $-1 < x(t) < 1$ and the DC constant is such that always $x(t) + \mathrm{DC} > 0$, $V_i(t)$ will increase up to threshold voltage V_{th}. At this point, the comparator will trigger the generation of a square pulse of fixed duration T_d and amplitude 1 at $y(t)$. Then, a negative feedback loop around the integrator forces $V_i(t)$ to decrease. After an initial transitory, we will reach at the end of the monostable pulse (T_o in Fig. 1*b*), the same initial voltage V_0 such that a stable oscillation is sustained. The instantaneous oscillation frequency can be calculated by imposing that the area of the pulse at $y(t)$ matches with the area of the input signal during the oscillation period T_o. Defining the oscillation frequency at rest f_o and the peak frequency deviation as f_d we obtain

$$f(t) = \frac{1}{T_o(t)} = \frac{K_x}{K_f T_d}\left[x(t) + \mathrm{DC}\right], \quad f_o = \frac{\mathrm{DC}\,K_x}{K_f T_s}, \quad f_d = \frac{K_x}{K_f T_d} \qquad (1)$$
$$V_0 = V_{th} + \left(K_x\left[x(t) + \mathrm{DC}\right] - K_f\right) T_d$$

Therefore, the pulse frequency at $y(t)$ is proportional to $x(t)$. It can be shown that sampling $y(t)$ with a sampling period T_s and setting $T_d = T_s$ produces the same sequence as a conventional single bit VCO-based ADC. A Fourier series representing $y(t)$ in Fig. 1*a* with sinusoidal inputs was described in [4], showing that the spectra of $y(t)$ contains $x(t)$ and modulation sidebands at every harmonic of f_o. Note that, to different conventional VCO ADCs, $y(t)$ contains in its lowpass components the spectra of $x(t)$, and therefore no XOR operation is needed to obtain the ADC output. Based on the Fourier series [4], we may estimate the bandwidth of the sidebands around f_o to calculate an approximated relation between the oversampling ratio (OSR) of the desired ADC converter, the oscillation centre frequency and the peak frequency deviation. Defining f_o and f_d as fractions of the sampling frequency, we obtain

$$f_o = f_s/M, \quad f_d = f_o/D, \quad M \ll 2 \cdot \mathrm{OSR} \cdot (D-1)/D \qquad (2)$$

Polyphase PFM: The system of Fig. 1*a* can easily be transformed into a polyphase oscillator if the monostable is implemented with the circuit proposed in Fig. 2*a*, where a multitap delay line made of digital inverters defines the pulse duration T_d. The first and last taps in the delay line define the beginning and end of the monostable pulse using an edge triggered set-reset flip-flop which captures the rising edge at the comparator output. To sample $y(t)$ in Fig. 2*a*, we may attach a parallel register to the taps of the delay line as in a TDC. The circuit of each bit of the sampling register is depicted in Fig. 2*b*. This circuit uses two D flip-flops to detect the rising edge of the monostable pulse as it travels through the delay line in the TDC and to synchronise it with the sampling clock. This way, a thermometer coded multibit output is generated as in a polyphase ring oscillator which can be transfomed into a binary coded sequence $y[n]$.

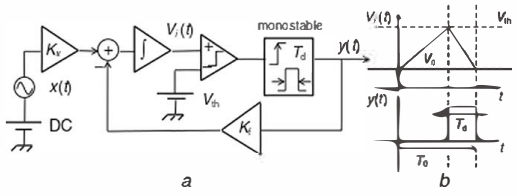

Fig. 1 *Operation of ideal PFM*
a Pulse frequency modulator block diagram
b Chronogram of Fig. 1a

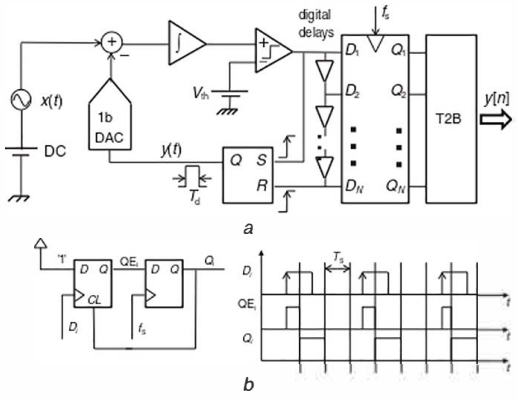

Fig. 2 *PFM with digital delay line*
a PFM with polyphase output
b Data capture circuit

Hardware implementation: The main advantage of the architecture of Fig. 2*a* is that the oscillation frequency linearly depends on $x(t)$ (1). It may be claimed that the PFM resembles a first-order continuous time sigma–delta modulator (CTSDM), which also requires an analogue integrator, comparator and feedback digital-to-analogue converter (DAC). However, the ADC of Fig. 2*a* has several implementation advantages over a CTSDM. First, its output is multibit without requiring a high linearity multibit DAC and a Flash quantizer. On the other hand, sampling is performed outside of the loop which desensitises the modulator from the sampling clock jitter. In addition, for high OSRs, the oscillation frequency f_o does not need to be exactly at $f_s/2$ (as is usually made in ring oscillator ADCs) and can be brought to a lower frequency ($M > 2$), with little signal-to-noise ratio (SNR) loss. In this case, the TDC delay can be increased to $T_d = MT_s$. This permits relaxing the speed and power requirements of the comparator, DAC and integrator without losing the linearity advantage, whereas in a ring oscillator, power could be traded-off by oscillation frequency, but linearity would not improve significantly [2]. The 1-bit DAC operates without a clock signal in an asynchronous manner. This could pose a problem due to ringing and different rise and fall times. However, by observing Fig. 1*b* and (1), we may see that only the area of the pulse influences the frequency. By choosing $f_o \leq f_s/2$, we ensure that the DAC always

generates an RZ pulse, and therefore pulse distortion only translates into a gain mismatch in K_f (Fig. 2*a*).

Circuit impairments: To test the robustness of the proposed ADC, we have simulated the effect of several circuit impairments in the system of Fig. 2*a*. Some effects that may influence the signal-to-noise and distortion ratio (SNDR) are jitter in the TDC delay line and mismatch in the digital delays. In addition, integrator DC gain and sampling clock jitter will have effect as in a conventional sigma–delta modulator. The simulation conditions have been set as follows: $f_s = 1$ GHz, OSR = 128, 16 delay taps, $f_o = 250$ MHz ($M = 4$) and $f_{cl} = f_s/8$ ($D = 2$). With these parameters, the tap delay is 266 ps and the DAC pulse width is 4 ns which seem perfectly doable in the current CMOS technologies. The analogue bandwidth is 3.9 MHz and the expected resolution can be extrapolated from a conventional first-order 4-bit sigma–delta modulator as follows:

$$\mathrm{SNR}_{\mathrm{peak}}(\mathrm{dB}) = 6N + 1.76 - 5.17 + 30\log_{10}\mathrm{OSR} = 83.8\,\mathrm{dB} \quad (3)$$

A simulation with an ideal behavioural model of Fig. 2*a* produces a SNDR = 77 dB for a −3 dBfs input, corresponding to 13 equivalent number of bits (ENOB).

Fig. 3 shows the dynamic range of the simulated ADC if each TDC delay has an independent jitter of 2.6 ps root-mean-square (rms) (1% of the nominal delay) and the total monostable pulse width has a +10% delay over its nominal value of 4 ns. In this case, the SNDR drops to 73.2 dB (12.4 ENOB), revealing the robustness of the proposed architecture. We have also simulated the effect of a non-ideal integrator. Fig. 4 shows the fast Fourier transform of the output data when the integrator has a limited DC gain $G_{dc} = 40$ dB.

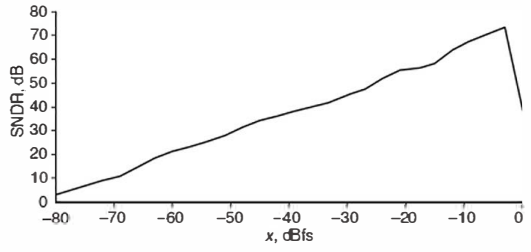

Fig. 3 *Dynamic range with TDC jitter and mismatch*

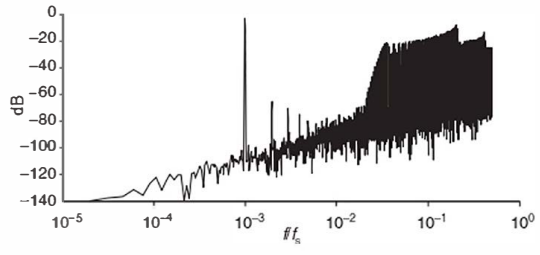

Fig. 4 *Simulation with finite integrator gain $G_{dc} = 40$ dB*

It can be seen that finite DC gain produces 'distortion' rather than quantisation noise leakage, as it would in a conventional CTSDM. This fact can be explained by noting that the Fourier series of $y(t)$ [4] does not change its spectral content with finite DC gain. Only the relative amplitude of harmonic sidebands change, resulting in noticeable aliased tones after sampling. Therefore, the effect of finite DC gain could be compensated digitally at the ADC output by recalculating (1). If the DC gain is raised to $G_{dc} = 50$ dB, the modulator recovers a SNR of 76 dB.

Finally, we have checked the robustness of the proposed architecture against sampling clock jitter. Fig. 5 shows the SNDR of the modulator of Fig. 2*a* (solid line), against the rms value of the clock period jitter assuming a white Gaussian distribution. As a reference, we have shown the SNDR of an equivalent CTSDM subjected to the same sampling clock (dashed line). As can be seen, the proposed architecture tolerates a period jitter nearly one order of magnitude larger than a conventional CTSDM.

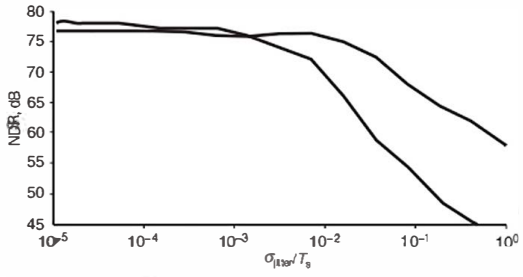

Fig. 5 *Sampling clock jitter*

Conclusion: We have presented a new data converter topology which permits implementing a multibit oversampled converter without requiring multibit DACs or Flash quantisers. This architecture can be compared in features to a ring oscillator based ADC, yet it retains the linearity inherent to the closed-loop sigma–delta modulators. Simulations show that the typical circuit impairments such as jitter and mismatches do not severely impede a CMOS hardware implementation.

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L. Hernández and E. Gutiérrez (*Electronics Technology Department, Carlos III University, Madrid, Spain*)

E-mail: luis.hernandez@uc3m.es

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