



Universidad
Carlos III de Madrid



This is a postprint version of the following published document:

C. Vázquez, P. Contreras, S. Vargas. "Low power consumption in silicon photonics tuning filters based on compound ring resonators", *Proc. SPIE 8629, Silicon Photonics VIII*, 86291F (March 14, 2013). Available in [doi:10.1117/12.2004812](https://doi.org/10.1117/12.2004812).

© 2013 Society of Photo Optical Instrumentation Engineers. One print or electronic copy may be made for personal use only. Systematic electronic or print reproduction and distribution, duplication of any material in this paper for a fee or for commercial purposes, or modification of the content of the paper are prohibited.

Low power Consumption Silicon Photonics Tuning Filters based on Compound Microring Resonators

C. Vázquez^a, P. Contreras^a, S. Vargas^b

^aDept. Tecnología Electrónica, Universidad Carlos III Madrid, Av. Universidad 30, 28911 Leganés, Madrid, Spain;

^bUniversidad Tecnológica de Panamá, 0819-07289

ABSTRACT

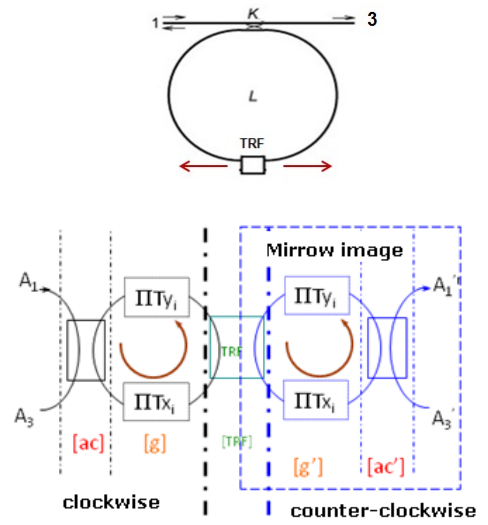
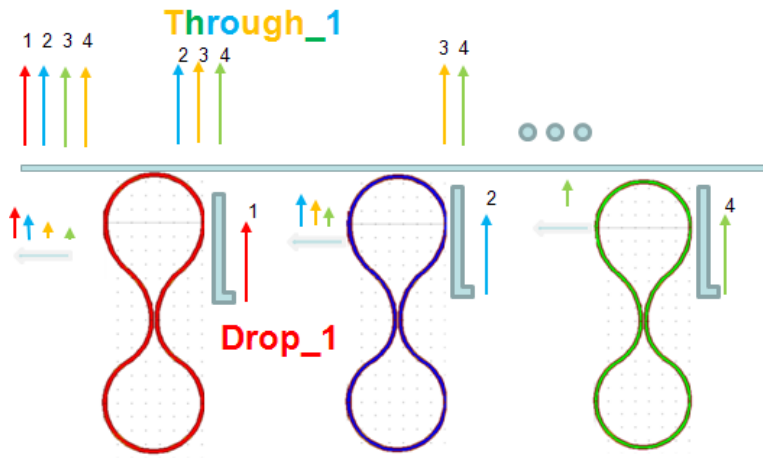
Scalable integrated optics platforms based on silicon-on-insulator allow to develop optics and electronics functions on the same chip. Developments in this area are fostered by its potential as an I/O technology that can meet the throughputs demand of future many-core processors. Most of the optical interconnect designs rely on small footprint and high power efficiency microring resonators. They are used to filter out individual channels from a shared bus guide. Second-order microring filters enable denser channel packing by having sharper pass-band to stop-band slopes. Taking advantage of using a single physical ring with clockwise and counter-clockwise propagation, we implement second order filters with lower tuning energy consumption as being more resilient to some fabrication errors. Cascade ability, remote stabilization potential, energy efficiency along with simple design equations on coupling coefficients are described. We design second-order filters with FWHM from 45 GHz to 20 GHz, crosstalk between channels from -40 dB to -20 dB for different channel spacing at a specific FSR, with energy efficiencies of single ring configurations and compatible with silicon-on-insulator (SOI) state of the art platforms.

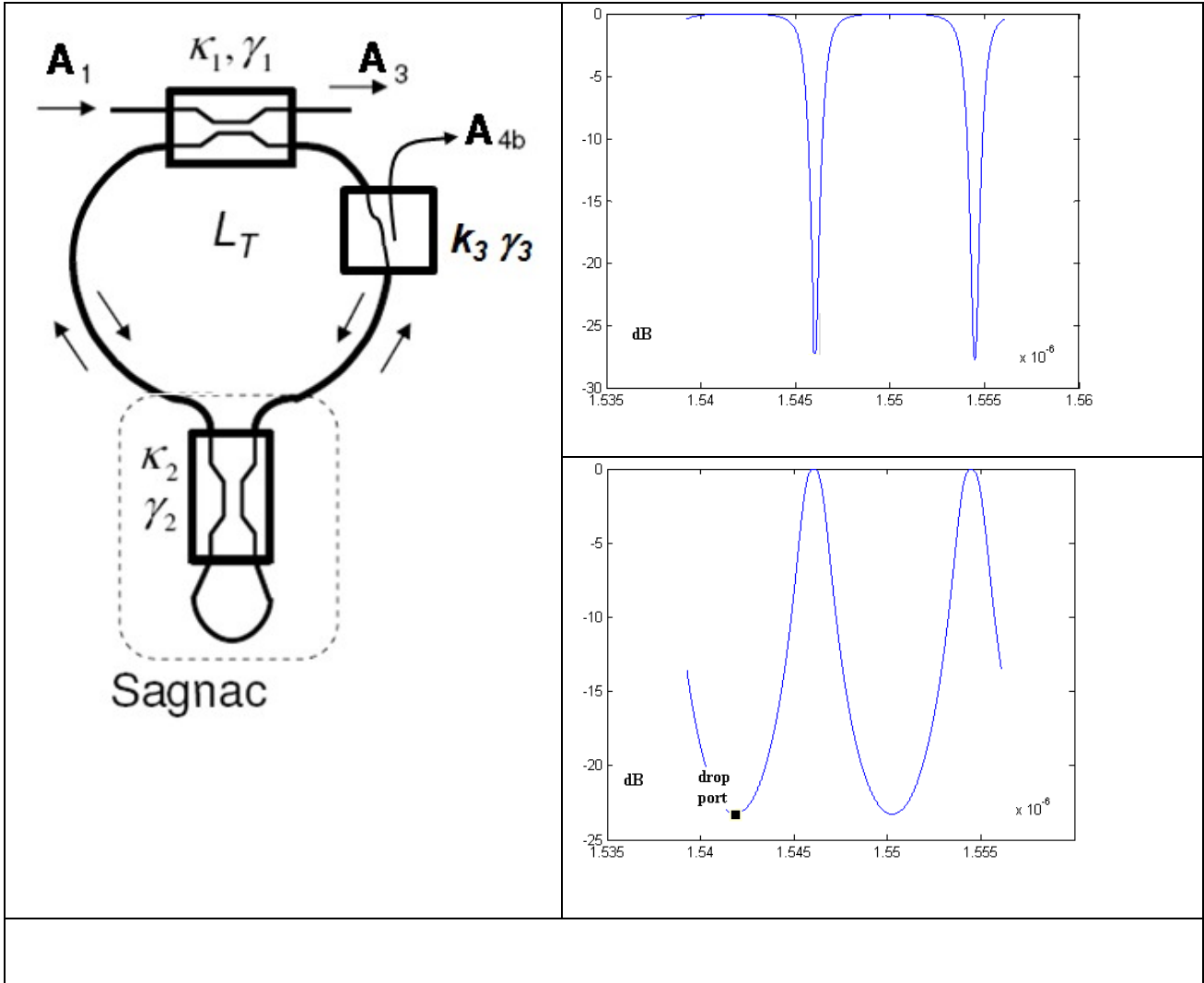
Keywords: power efficiency, compound microrings, silicon photonics, thermal tuning, add-drop filters, post-manufacturing trimming, integrated optic devices

1. INTRODUCTION

Last developments in integrated optics, specially in silicon photonics, make affordable an increment in the integration scale and system complexity. Platforms based on silicon-on-insulator (SOI) allow to develop optics and electronics functions on the same chip. Developments in this area are fostered by the need of optical interconnects, for improving many-core processor performance in terms of speed, footprint and power efficiency. International Roadmap for Semiconductors (ITRS) foresees a saturation in power dissipation by 2022 [1]. From those data, Miller [2] estimates that new systems should be able to consume energies below 170fJ/bit in 2022, for clock processor speeds of 67.5 GHz (off-chip). The power consumption of recent silicon WDM photonic interconnect links [3-6], shows that there is still space for improvement. Most of those designs rely on small footprint and high power efficiency microring resonators [7]. They perform channel modulation and multiplexing on the transmitter size, and channel demultiplexing on the receiver size. But those microrings are temperature and fabrication variation sensitive, requiring tuning and stabilization mechanisms that represent an important area on link power consumption breakdown. A single ring may not perform properly when a high number of channels with minimal crosstalk within a free spectral range (FSR) is required. In those cases, filterbanks consisting of second- or higher-order microring can be used. But the control of the resonant frequency of each ring requires dimensional precision in the order of tens of picometer, so more thermal tuning is required to overcome the frequency mismatch between the two rings of a channel and each channel location mismatch [8].

As part of those new silicon photonics devices we proposed compound structures, with novel tuning capabilities, which can be implemented with state of the art SOI technology and CMOS processes [9]. Special attention is given to evaluate the power consumption of those configurations from manufactured device data reported in the literature [8]. The proposed devices are based on microrings with embedded multireflection configurations [10-12] and thermal tuning. Special attention is given to second-order filters based on clockwise and counter-clockwise propagation so any manufacturing tolerance will affect in the same way both propagations. As a result, lower post-processing energy consumption is expected in comparison with solutions based on two physically separated microrings.





Both, through A_3 and drop A_{4b} ports have the same 2 complex conjugated poles. Meanwhile through port, A_3 , has two zeroes, which can be complex conjugate if $k_1 < k_c$, being k_c given by:

$$k_c = -8A + 4\sqrt{4A^2 + A} \text{ and } A = \frac{k_2 \times (1 - k_2)}{(1 - 2k_2)^2} \quad (2)$$

The drop port selectivity at the resonance frequencies increases as you get closer to the condition

$$(1 - \gamma_3)^{1/2} (1 - k_3)^{1/2} e^{-\alpha L_T} (1 - \gamma_1)^{1/2} (1 - \gamma_2) (1 - k_1)^{1/2} = 1 \quad (3)$$

where γ_1 , γ_2 and γ_3 are the excess losses in each coupling region.

For complex conjugated zeroes, the through output field rejection at the resonance frequencies increases as you get closer to the condition

$$(1 - \gamma_3)^{1/2} (1 - k_3)^{1/2} e^{-\alpha L_T} (1 - \gamma_1)^{1/2} (1 - \gamma_2) = 1 \quad (4)$$

As shown before, and in contrast to single microring transfer function behavior, the conditions for reaching high selectivity at drop port and high rejection ratio at through port are decoupled.

For selecting channels at the drop port at the same frequencies than the channels rejected at the through port, the coupling coefficient k_2 has to be closed to zero.

Through and drop port transmission functions for $k_2=2.6\%$, $k_3=1\%$, $k_1=48.2\%$, 8% overall losses, and FSR=1 THz (8nm at 1550 nm), can be seen in Figure 2.b. A 1 dB bandwidth of 0.82 nm and 0.1 nm at through and drop port respectively are obtained. In the next section, other designs are reported.

2.2 Circuit design

In photonic interconnects designs for computing systems, single channel rates typically range from 4 Gbs to 25 Gbs [3-6]. A 20 channels manufactured filter bank, including data of the power needed to tune the different channels and the thermal crosstalk between rings can be seen in [8], where each second-order filter has a channel bandwidth of 20 GHz. A 20 GHz bandwidth can accommodate 12.5 Gbs NRZ data transmission without bit error rate penalties, as the full width at half maximum (FWHM) bandwidth is greater than 1.5 times the symbol rate. The channel spacing was set to 124 GHz with a 2 THz (16 nm) free spectral range. In interconnect applications, all wavelengths on a given waveguide are transmitted or received at a single location for all channels and travelling the same optical paths, so crosstalk requirements between channels is less restricted than in other telecommunications applications, being 20 dB a general accepted value [21]. Most of the second order filter bank designs based on SOI used radius of 7 μm in the manufactured devices and with projections to reduce those values to 3-4 μm . In terms of waveguide and bend losses, they depend on the material used in the manufacturing process. For being able to cover main CMOS materials with potential application for integrated photonics, we select the higher values as those reported for polycrystalline silicon (poly-Si) around 6dB/cm at 1550 nm. In terms of manufacturing potential, power coupling coefficients below 0.045% have already been reported [8].

In Table I, some designs of second-order filters with FWHM from 45 GHz to 20 GHz, crosstalk between channels from -40 dB to -20 dB for different channel spacing at a specific FSR, and compatible with current integrated optics technologies on SOI are reported.

Those values are obtained from drop and through port amplitude transfer functions [16] using a transmission matrix framework to express the various couplings and using MATLAB in the simulations. It can be seen how k_3 value only affects through port rejection ratio (RR), meanwhile most critical parameter designs are k_2 and k_1 . A k_2 value closed to zero is selected and k_1 is calculated from Eq. (2). FSR is estimated considering a group index of 2.94, a ring radius of 4 μm and a total length of around 2.6 times the length of a single microring with the same radius, or an equivalent

clockwise single ring radius of 10.4 μ m, to allocate the Sagnac loop. From this length and considering an average loss of 6dB/cm, the round trip loss is calculated.

Table 1. Second order mRRSG filter parameters, $\alpha=6$ dB/cm, FSR=1.562THz. ¹CT=crosstalk at adjacent channel. ²RR=rejection ratio at resonance frequency. $k_3=0.001$

k_2	k_1	FWHM (GHz)	Drop (dB) CT ¹ (125GHz)	Drop (dB) CT (62.5GHz)	Drop (dB) CT (37.5GHz)	Through (dB) RR ²
1%	11.9%	45	-28.3	---	---	-41
0.1%	11.9%	45	-29.3	---	---	-52.8
0.08%	10.7%	40	-31.2	-20	---	-50
0.05%	8.6%	31.8	-35	-23	---	-45
0.03%	6.7%	24.9	-39.2	-27.3	---	-42.4
0.02%	5.5%	20	-42.5	-30.5	-21.8	-40

Some designs shown on table I allow multiplexing 13 channels at 125 GHz, or 26 channels at 62.5 GHz or 42 channels at 37.5 GHz channels spacing respectively, with crosstalk adjacent channel (CT) >-20 dB. Through port RR>-40 dB is obtained in all cases. These designs meet the target from medium to high bandwidth scenarios [21], [5], scaling up to 42 channels or 525 Gb/s with less post-fabrication trimming than current second-order filter designs, as it will be discussed in the next section. There is margin in the design values for accommodating 10% tolerances on coupling coefficients depending on the number of channels set. The ring radius can also be reduced according to state of the art available SOI technology and less total length can be considered for accommodating the Sagnac loop.

3. DISCUSSION

The second-order mRRSG filter is expected to be more tolerant to manufacturing process, so less post-manufacturing trimming should be needed. Power efficiency improvement is estimated from results reported in [8]. In the 20 channels filter bank, with 20 GHz channel bandwidth and 124 GHz channel spacing, initially most of the channels were misaligned, with frequencies mismatches between the two rings of a channel of up to 133 GHz, equivalent to the channel spacing itself. The average tuning efficiency was calculated to be 27 mW/GHz. The tuning power needed for the inter-ring frequency mismatch compensation in a channel is about 3.6 mW and the total average tuning power needed is 16 mW/channel. Around 22.5% of the power can be saved using second order filter designs intrinsically more tolerant to fabrication as the one proposed in this paper. In most of the link power efficiency interconnect system analysis, single order filters are considered [22]. Second order filters are taken into account [6] by cascading two single ring filters, with power consumptions based on adding contribution of each ring with a total of 2.8 mW/channel, following [22] rather than [8]. Inter-ring tuning power consumption and some feedback can be avoided with the configuration proposed in this paper, meaning more than 40% efficiency improvement. The impact of the thermal stabilization in the receiver module on the link power efficiency can be reduced from 8.8% to 4.5% for the scenario of a total 2.5pJ/bit efficiency.

On the other hand, the power budget takes into account a power tap for the thermal stabilization of each stage of 0.5 dB [6]. The tap can be avoided using the proposed mRRSG filter, as the light reflected back from the configuration can be used for monitoring and thermal stabilization if necessary. Although initial identification of each channel can be difficult, individual heating can help to associate each channel to each mRRSG and the tuning can be done afterwards. The thermal corrections to the resonant peaks are strictly unidirectional and to minimize the tuning energy, its mRRSG device can be tuned to the closest order resonance to a specific wavelength channels, using a symmetric resonant comb spectrum [22].

4. CONCLUSIONS

The potential of improving power efficiency in optical interconnects demanding second-order filters for denser channel packing can be achieved with the novel approach reported in this paper. Taking advantage of using a single physical ring with clockwise and counter-clockwise propagation, the impact of the thermal stabilization in the receiver module on the link power efficiency can be reduced from 8.8% to 4.5% for scenarios of a total 2.5pJ/bit efficiency. The mRRSG

second-order filter with slightly different ring radii can be cascaded within one FSR to construct a filter bank for being used for wavelength division demultiplexing. Simple design equations for selecting coupling coefficients are described. Second-order filters with FWHM from 45 GHz to 20 GHz, crosstalk between channels from -40 dB to -20 dB for different channel spacing at a specific FSR, with energy efficiencies of single ring configurations and compatible with current integrated optics technologies on SOI are reported.

If finally, optical interconnects based on microresonators succeed, a reduction in each single device consumption should imply a big total reduction. This strategy is aligned with the global efforts to reduce carbon footprint related to Information and Communications Technologies.

5. ACKNOWLEDGEMENT

This work has been sponsored by the Spanish CICYT (grant n°. TEC2012-37983-C03-02 & TEC2009-14718-C03-03) and Fundación Caja Madrid.

REFERENCES

- [1], <http://www.itrs.net/Links/2007ITRS/ExecSum2007.pdf>
- [2] D. A.B. Miller, "Device Requirements for Optical Interconnects to Silicon Chips" Proceedings of the IEEE, 97 (7), 1166-1185, (2009).
- [3] G. Li, X. Zheng, J. Lexau, Y. Luo, H. Thacker, T. Pinguet, P. Dong, D. Feng, S. Liao, R Shafiiha, M Asghari, J Yao, J Shi, Ivan N. Shubin, D. Patil, F. Liu, K. Raj, R. Ho, J. E. Cunningham, A. V. Krishnamoorthy "Ultralow-power silicon photonic interconnect for high-performance computing systems" Proc. of SPIE Vol. 7607, 760703-15 (2010).
- [4] M. Georgas, J. Orcutt, R. J. Ram, V. Stojanovic "A Monolithically-Integrated Optical Receiver in Standard SOI", IEEE Journal of Solid State Circuits, 47(7), 1693-1702 (2012).
- [5] M. Georgas, J. Leu, B. Moss, C. Sun, V. Stojanovic "Addressing Link-Level Design Tradeoffs for Integrated Photonic Interconnects". Proc. Custom Integrated Circuits Conference (CICC), 2011 IEEE
- [6] N. Ophir, K. Bergman, C. Minero, D. Mountain "A Silicon Photonic Microring Link Case Study for High-Bandwidth Density Low-Power Chip I/O" IEEE Micro, in press (2013).
- [7] M. Lipson, "Guiding, modulating, and emitting light on silicon-challenges and opportunities," J. Light. Tech., 12, 4222-4238 (2005).
- [8] M. S. Dahlem, C. W. Holzwarth, A. Khilo, F. X. Kartner, H. I. Smith, and E. P. Ippen, "Reconfigurable multi-channel second-order silicon microring-resonator filterbanks for on-chip WDM systems", Opt. Exp., 19 (1), 306-316 (2011).
- [9] J.S Orcutt, A. Khilo, A., et al..J. R. Ram. "Nanophotonic integration in state-of-the-art CMOS foundries". Optics Express, 19: 2335-2346 (2011).
- [10] S. Vargas, C. Vázquez, "Synthesis of Optical Filters Using Sagnac Interferometer in Ring Resonator" IEEE Photonics Tech. Lett., Vol. 19,23, 1877 (2007).
- [11] C. Vázquez, S. Vargas, J.M. S. Pena, P. Corredera "Tunable Optical Filters Using Compound Ring Resonators for DWDM" IEEE Photonics Technology Letters 15 (8), 1085 - 1088 (2003).
- [12] Salvador Vargas, Carmen Vázquez "Synthesis of optical filters using microring resonators with ultra-large FSR" Opt. Express 18, 25936-25949 (2010).
- [13] K. Feng, G. Keiser, S. Lee "Power consumption in hybrid access and home networking network". Proc. Optical Fiber Conference (2011).
- [14] M. Pickavet, W. Vereecken, S. Demeyer et al "Worldwide Energy Needs for ICT:the Rise of Power"- Proc. Conference IEEE Aware Networking ANTS (2008).
- [15] <http://www.eweekurope.co.uk/news/news-it-infrastructure/alcatel-lucent-vows-to-boost-network-efficiency-1000-fold-2985>
- [16] C. Vázquez, S. Vargas, J. M. S. Pena "Sagnac Loop in Ring Resonators for Tunable Optical Filters" Journal of Lightwave Tech, 23(8), (2005).
- [17] M. R. Watts, T. Barwicz, M. Popovic, P.T. Rakich, L. Socci, E. P. Ippen, H. I. Smith, F. Kaertner "Microring resonator filter with doubled free-spectral-range by two-point coupling". Proc. Conference on Lasers and Electro-Optics (2003).

- [18] F. Xia, M. Rooks, L. Sekaric, Y. Vlasov, "Ultra-compact silicon WDM optical filters with flat –top response for on-chip optical interconnects", Proc. *Optical Fiber Comm. Conf. 2005* (Optical Society of America, Washington, DC, 2007)
- [19] M. A. Popović, et al., Tunable, Fourth-Order Silicon Microring-Resonator Add-Drop Filters, 33rd European conference and Exhibition on Optical Communication, Berlin, Germany (2007).
- [20] S. Xiao, M. H. Khan, H. Shen, M. Qi Multiple-channel silicon micro-resonator based filters for WDM applications, *Optics Express* 15 (12), 7489-7498 (2007).
- [21] J. S. Orcutt [Monolithic Electronic-Photonics Integration in State-of-the-Art CMOS Processes], PhD, MIT (2012)
- [22] A. V. Krishnamoorthy, X. Zheng, G. Li, J. Yao, T. Pinguet, Attila Mekis, H. Thacker, I. Shubin, Y. Luo, K. Raj, J. E. Cunningham "Exploiting CMOS Manufacturing to Reduce Tuning Requirements for Resonant Optical Devices" *IEEE Photonics Journal*, 3 (3), 567-579 (2011).