Departamento de Tecnología Electrónica

PROYECTO FIN DE CARRERA

Diseño del driver y calibración de un sensor óptico

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Título: Diseño del driver y calibración de un sensor óptico
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Realizado el acto de defensa y lectura del Proyecto Fin de Carrera el día de Octubre de 2015 en Leganés, en la Escuela Politécnica Superior de la Universidad Carlos III de Madrid, acuerda otorgarle la CALIFICACIÓN de

VOCAL

SECRETARIO PRESIDENTE

Agradecimientos

Me gustaría agradecer a mis padres, abuelos y a mi hermana todo el apoyo que me han dado durante estos duros meses de trabajo, su compresión y dedicación constante. Para mí ellos han sido mi principal apoyo y el motor que me ha impulsado a seguir hacia delante.

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Por último agradecer a todos mis amigos por los momentos de desconexión que me han brindado, la ayuda psicológica que me han prestado y el que hayan hecho que cada momento duro sea más ameno.

Resumen

Este proyecto está basado en el diseño y montaje de un driver encargado de controlar un láser. El objetivo principal del trabajo es que el driver permita ajustar la potencia emitida (punto de trabajo). Por otro lado también debe permitir modular la potencia emitida a partir de una señal de entrada en el rango de decenas de kiloherzios. Para ello partimos de una amplitud de 3,3 V.
Por último, diseñar la PCB, utilizando la herramienta OrCad Capture para el diseño del esquemático y OrCad Layout para el rutado y la creación de huellas.

Summary

This Project is based on the design and the assembly of a driver to responsible for controlling a laser. The main objective of this project is that the driver should be allowed to adjust the output power (operating point). On the other side, the driver should also make possible to adjust the output power from an input signal in the range of tens of KHz. We start with a 3.3 V amplitude.

Finally, I should design the PCB using Orcad Capture to make the design and Orcad Layout to root the PCB and to create the footprints.

Índice general

Índice de figuras

Índice de tablas

Listado de Acrónimos

1. LASER: *Light Amplification by Stimulated Emision of Radiation*
2. PCB : *Printed Circuit Board*
3. GND: *Ground, tierra.*
4. OTA: *Operational Transconductance Amplifier*
5. SMD: Surface Mounted Device

1. Introducción y objetivos

1.1 Introducción

Este trabajo de final de grado comienza con el estudio previo de un sensor óptico compuesto por los siguientes bloques:

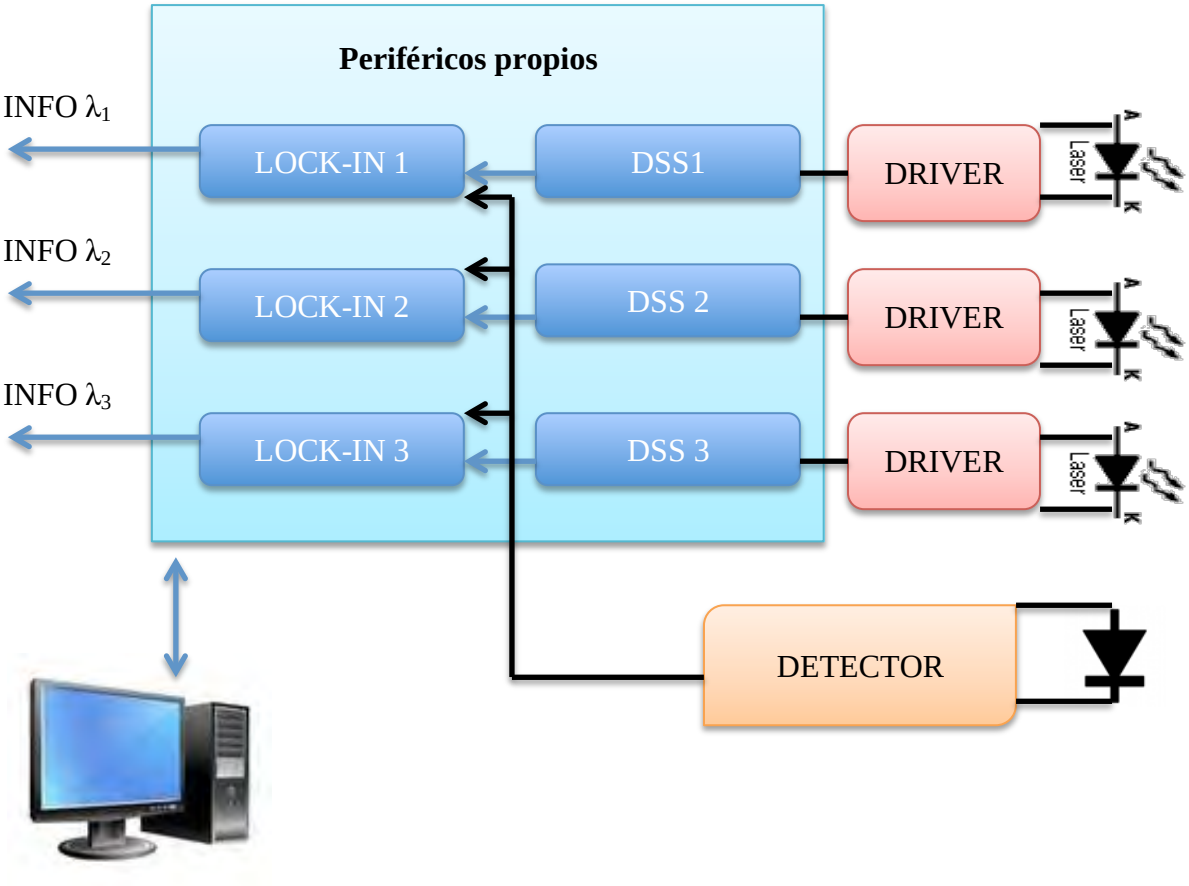


Ilustración 1 Esquema de bloques de un sensor óptico

Mi trabajo en concreto se centra en el diseño del bloque llamado “DRIVER”.

Inicialmente los diodos láseres utilizados para este sensor eran de fibra óptica. Una de las modificaciones de mi trabajo ha sido sustituirlos por otros sin fibra.

Otra modificación importante es que los láseres irán soldados a su driver consiguiendo así un montaje individual y más flexible.

Por último, otra modificación que se ha hecho es añadir unos puntos de test (Test points) que nos permitirán tomar medidas de corriente y tensión necesarias para calibrar el driver según el láser que incorporemos, algo que resultará muy cómodo a la hora de hacer pruebas. En el driver hemos incorporado tres puntos de test utilizando unos conectores de tipo jumper convencionales:

1. **Jumper J1:**

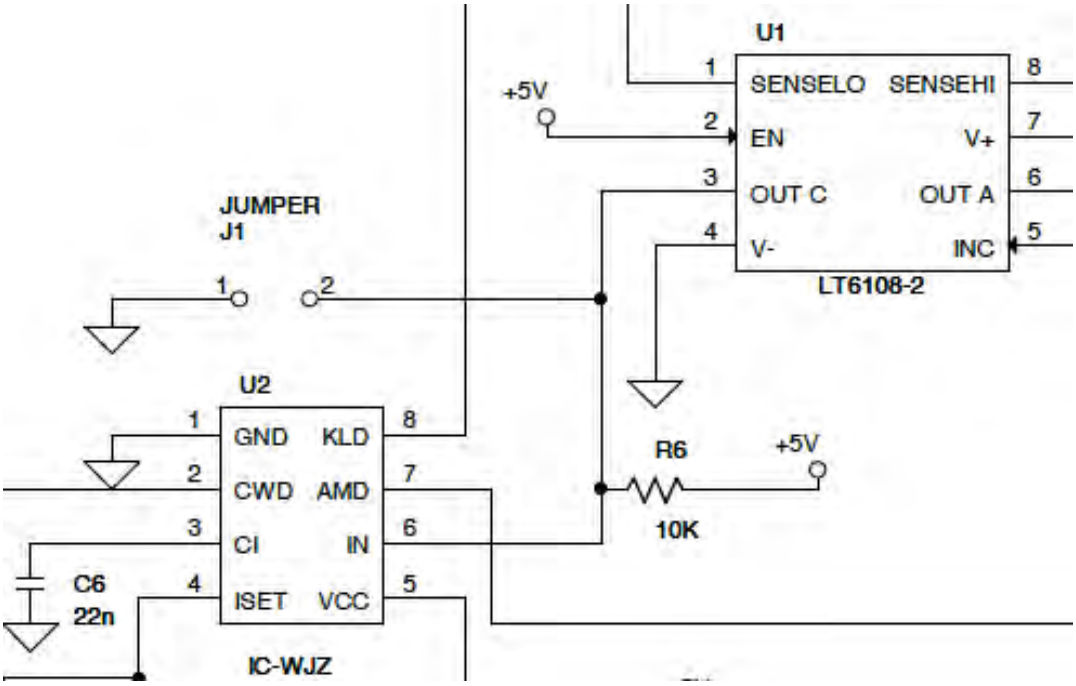


Ilustración 2 Localización del Test point 1 en el circuito

Es el encargado de detectar la sobrecorriente, cuando se produce una sobrecorriente por el láser el LT6108-2 da un valor 0 por la salida OUT C y corta la corriente para evitar que el láser se estropee. Estos valores se analizarán en apartados siguientes.

2. Jumper J2:

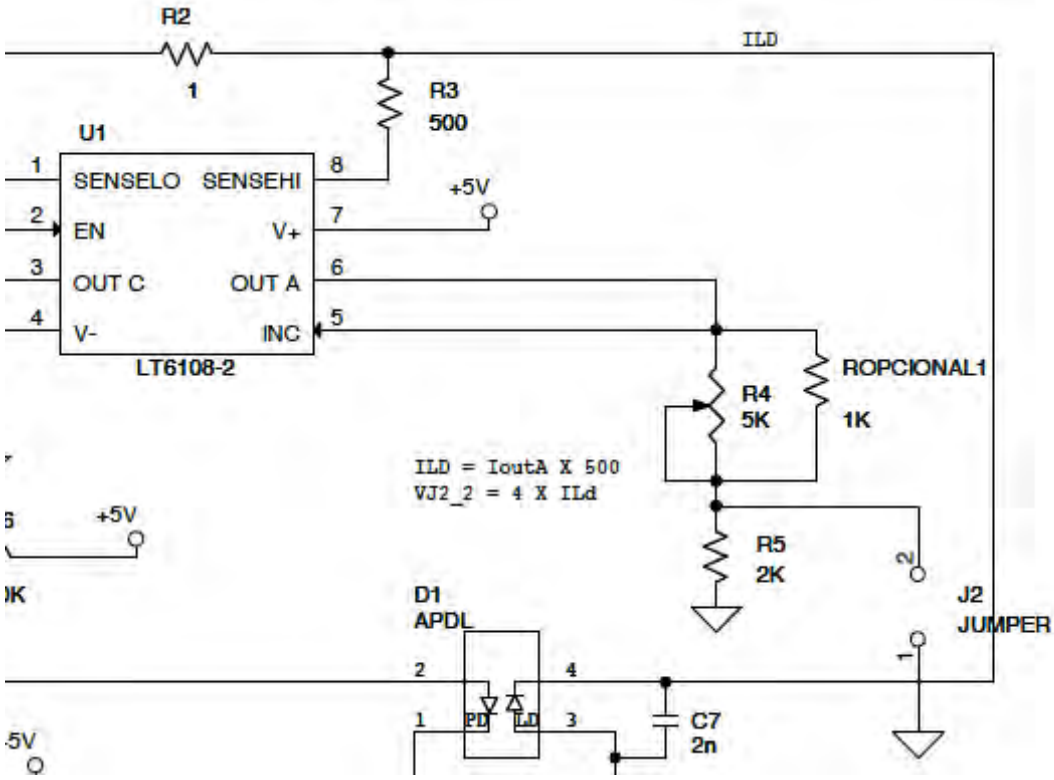


Ilustración 3 Localización del Test point 2 en el circuito

Este punto de test es uno de los más importantes, puesto que nos permite calibrar la corriente que queremos permitir que pase por el láser (I_{LD}), algo que resulta muy útil si queremos asegurarnos de que al introducir el láser en el circuito no se produzca una sobrecorriente por él y deje de funcionar. Por tanto, este punto de test nos permitirá visualizar el valor de I_{LD} mientras que lo vamos regulando con el potenciómetro R_4. Las ecuaciones necesarias para obtener el valor de la corriente que circula por el láser a partir de la tensión medida en el punto de test se explicarán detalladamente en apartados siguientes.

3. Jumper J3:

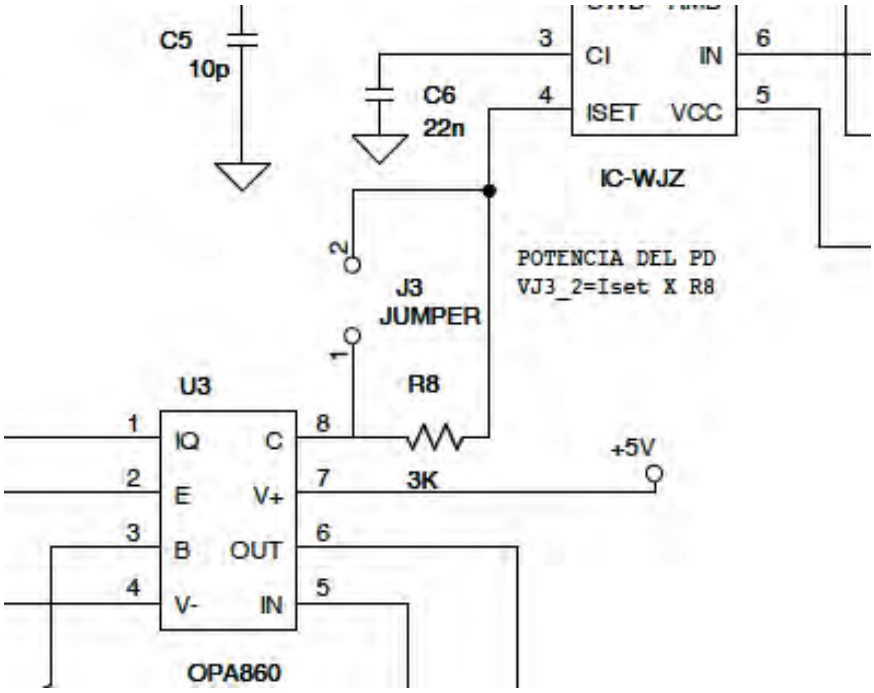


Ilustración 4 Localización del Test point 3 en el circuito

El último punto de test del circuito es el encargado de medir la corriente de referencia que fija el IC-WJZ en el fotodiodo monitor. La ecuación para tomar la medida de esta corriente a partir del valor de tensión medido en el punto de test es extraída de la Ley de Ohm.

1.2 Objetivos

El objetivo principal del proyecto es el diseño de circuito driver para diodos láser que:

1. Permita ajustar el punto de trabajo del diodo láser de manera que emita una potencia media constante.
2. Permita modular la potencia emitida por el láser hasta 100 KHz.
3. Incorpore una limitación de corriente máxima por el diodo láser.
4. Incluya puntos de test en el circuito para monitorizar la potencia óptica de emisión y el ajuste de corriente máxima.

Para completar este proyecto se han cumplido cada uno de ellos.

1.3 Medios empleados

Este proyecto se ha realizado en los laboratorios del Grupo de Optoelectrónica y tecnología Láser. Los medios empleados han sido la instrumentación básica del laboratorio (generador de onda, fuentes de alimentación, osciloscopio…) además de los equipos informáticos utilizados.

Para la fabricación de la PCB se ha hecho uso de las facilidades del Departamento de Tecnología Electrónica de la UC3M.

1.4 Estructura de la memoria

A continuación se va a presentar un resumen por capítulos de cómo esta estructurada la memoria:

- En este primer apartado se hace una pequeña introducción al trabajo de final de grado, en la que se explican los objetivos y se estructura como va a ser la memoria.

- En el segundo apartado se desarrollan los conceptos base para este trabajo, comentando desde que es un sensor óptico hasta lo que es un driver.

- En el apartado 3 se explica el diseño del driver partiendo del análisis de los elementos que lo componen y de cómo funcionan en un circuito electrónico y por otro lado, también se explica el montaje de la PCB a partir del esquemático realizado y todos los materiales y programas que han sido necesarios.

- En el apartado 4, se detallan los procedimientos a seguir y los detalles a tener en cuenta a la hora de poner el driver en funcionamiento con un láser.

- En el apartado 5 se dictan las conclusiones del proyecto.

- Para terminar en el apartado 6 se encuentran todos los anexos, desde las hojas de características de los componentes que tiene el driver hasta las de los tres láseres que se quieren utilizar y además contiene una hoja de presupuesto.

- Finalmente, mostramos todas las referencias bibliográficas que se han consultado para poder realizar este trabajo.

2. Estado del arte

2.1 Sensores ópticos

2.1.1 Definición

Los detectores ópticos basan su funcionamiento en la emisión de un haz de luz que es interrumpido o reflejado por el objeto a detectar.

2.1.2 Partes

Los sensores ópticos constan de las siguientes partes:

- Fuente
- Receptor
- Lentes
- Circuito de salida

2.2 Diodo laser

Un diodo láser es un dispositivo semiconductor similar a los diodos Led que bajo las condiciones adecuadas emite luz láser.

Cuando el cátodo está cargado negativamente respecto al ánodo, a un voltaje mayor que el mínimo para no producir una interrupción en su funcionamiento, es decir, a más de 0.6V, la corriente fluye a través del diodo.

Para este trabajo de final de grado se han escogido tres diodos láser con diferentes longitudes de onda para detectar tres tipos de materiales diferentes (asfalto seco, agua y hielo).
Las características de cada uno de ellos se encuentran adjuntas en el Anexo llamado "Hojas de características" (apartado 6.3).

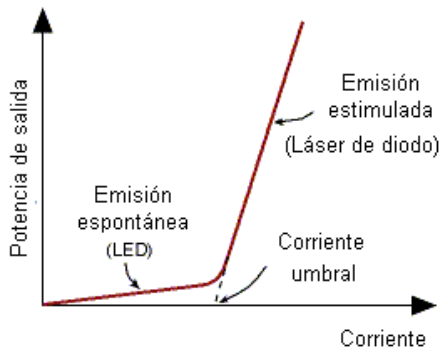


Ilustración 5 Potencia vs Corriente

En la Ilustración 5 podemos ver que para que un diodo laser funcione correctamente, la salida óptica únicamente puede ser generada y mantenida, sólo si la entrada de corriente de polarización o en inglés Bias Current, está por encima del umbral (I_{TH}).

La corriente de modulación será la que nos permita enviar o no información, ya que esta corriente genera impulsos a la salida, y en los instantes en los que haya un impulso será cuando el diodo láser estará emitiendo luz, por lo tanto estaremos enviando información.

2.3 Driver

En este trabajo de final de grado está centrado en el diseño de un driver capaz de controlar cada uno de estos tres diodos laser. Este driver es el encargado de fijar una corriente de referencia en el fotodiodo monitor del láser en función de la potencia que emite este. Este driver está compuesto por 5 grandes bloques:

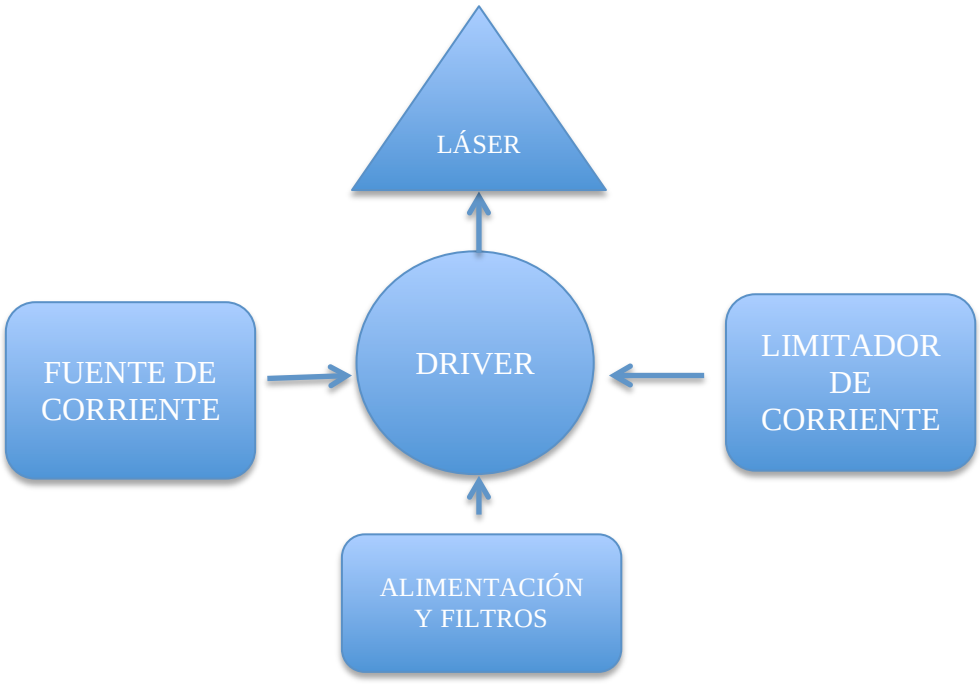


Ilustración 6 Diagrama de bloques del Driver

- IC-WJZ: es el driver encargado de fijar la corriente de referencia en el fotodiodo monitor.
- Alimentación y filtros: generan la tensión necesaria en los diferentes puntos del circuito.
- Fuente de corriente: genera un valor de corriente a partir de un valor de tensión.
- Limitador de corriente: limita la corriente máxima que circula por el láser.
- Láser : emite luz laser con una longitud de onda determinada.

3. Diseño y Montaje

Para el diseño del driver he utilizado la herramienta Orcad Capture, que es una herramienta que permite dibujar esquemas de circuitos electrónicos tanto digitales como analógicos. Por otro lado, para el diseño de la PCB he usado la herramienta Orcad Layout que permite diseñar placas de circuitos impresos.

Este apartado queda dividido en el diseño previo de un esquemático, estudiando la relación que existe entre todos sus componente. Una vez terminado el esquemático, procedemos al diseño de la PCB que posteriormente será impresa y en la que se soldarán todos los componentes.

3.1 Diseño del esquema

A la hora de diseñar el esquema, dividimos el proceso en tres bloques:

3.1.1 Diseño del driver

Partimos del circuito integrado IC-WJZ de IC-HAUS [3], que es un driver utilizado para diodos láser. Permite operar en continua y modular hasta 300 KHz.

Este circuito permite fijar la potencia emitida por el láser en un punto de trabajo concreto, fijando una corriente de referencia en el fotodiodo monitor.

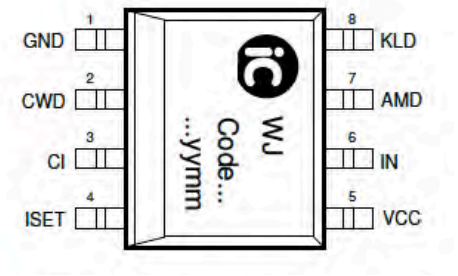


Ilustración 7 Colocación de los pines del IC-WJZ

Este componente esta compuesto de 8 pines. El pin 1 y 5 son los pines de alimentación GND y VCC. El pin 2 es un mecanismo de seguridad llamado “Watchdog” que provoca un “Reset” en el caso en el que el sistema se haya quedado bloqueado. El pin 3 es el encargado del control de potencia. El pin 4 es el encargado de fijar la corriente de referencia. Por último los pines 7 y 8 son los del ánodo del fotodiodo monitor y el cátodo del diodo láser que provocan a su vez que el ánodo del diodo láser y el cátodo del fotodiodo monitor estén unidos.

Según el catálogo del fabricante [3], el pin 4 tiene una tensión constante, por lo que si coloco en este pin una resistencia R_{SET} unida a su vez a tierra puedo calcular la I_{SET_ref} con la siguiente expresión:

$$R_{SET} = \frac{CR1 \cdot V(I_{SET})}{I_{AV}(AMD)} \qquad [ecuación\ 1]$$

Con CR1 = 3, ya que usamos el IC-WJZ y V(I_{SET}) = 1.22V.

Pero las especificaciones de mi diseño requieren que esta corriente esté modulada, por lo que sustituyo esta R por una fuente de corriente controlada por tensión tal y como se explica en el siguiente apartado.

El circuito genérico quedaría así:

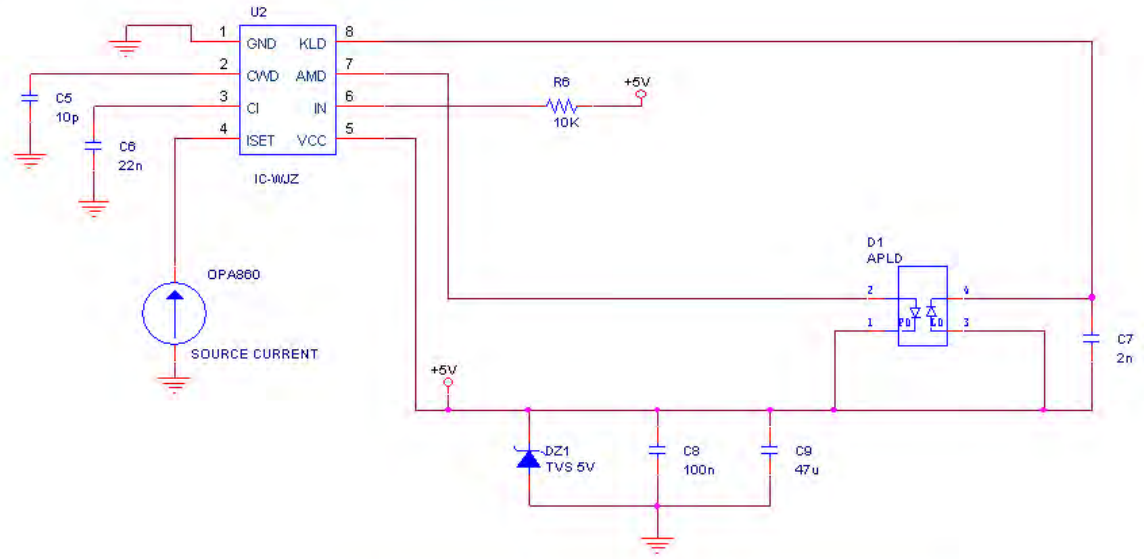


Ilustración 8 Esquema genérico del driver

La Ilustración 8 resume el funcionamiento del IC-WJZ en mi trabajo, tiene un diodo Zener (DZ1) que protege de la sobretensión, dos condensadores (C_8 y C_9) que son estabilizadores de tensión, para eliminar el ruido y se observa que he unido al pin 4 una fuente de corriente que será explicada en el siguiente apartado.

3.1.2 Diseño de una fuente de corriente para modular.

El OPA860 es un componente que funciona como una fuente de corriente controlada por tensión. Su función es la de modular la corriente (en los rangos necesarios) por el láser a partir de un valor de tensión.
Incluye un amplificador operacional de transconductancia (OTA) y buffer de tensión. El OTA puede entenderse como un transistor con sus tres terminales, uno de alta impedancia de entrada (base), uno de baja impedancia de entrada/salida (emisor) y la salida de corriente (colector), es preciso señalar, que el OTA no es un transistor, su funcionamiento en un circuito es muy similar al de un transistor ya que ambos son fuentes de corriente controladas por tensión, pero tal y como se aprecia en la Ilustración 9, vemos que hay una diferencia en el sentido de la corriente por el colector, ya que en el OTA puede circular en ambos sentidos en cambio en un transistor no.

Nosotros usaremos la configuración del OTA en base común, que es el de transconductancia, que puede ser ajustado con una ganancia (g_m).

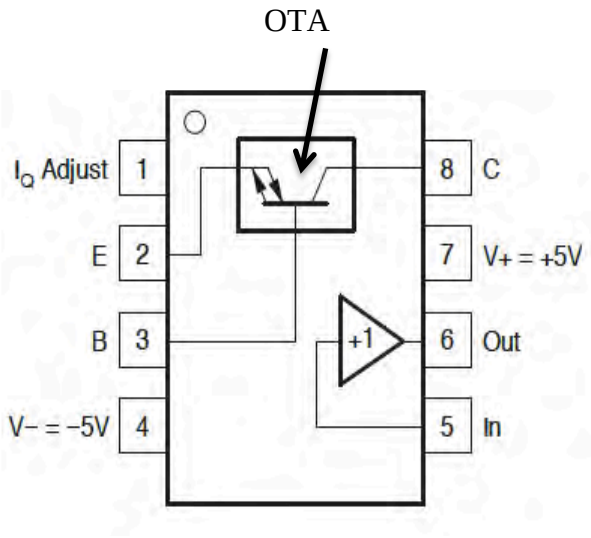


Ilustración 9 Colocación de los pines del OPA860

Introduciendo el OPA860 en el esquemático se ve de la siguiente manera:

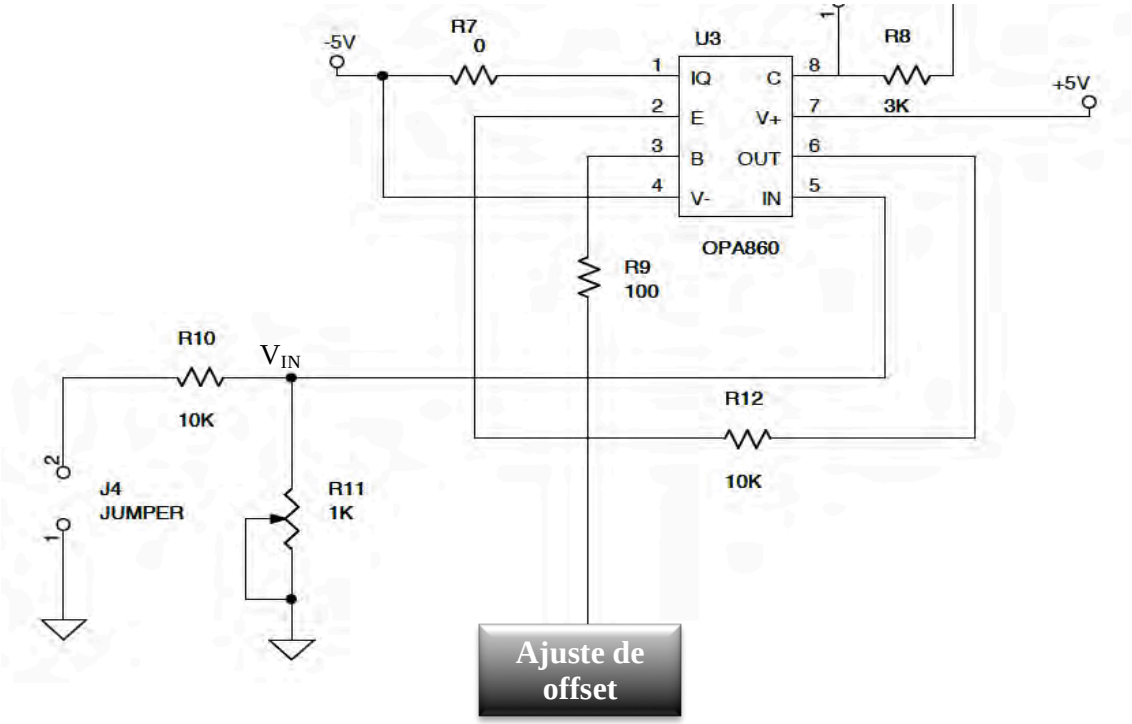


Ilustración 10 Esquema de la fuente de corriente

Si nos fijamos en la Ilustración 10, la resistencia R_{12} es la encargada de fijar la ganancia del circuito G_m. Por otro lado tenemos un circuito externo encargado de ajustar el offset que produce el OPA860 que se explicará en el siguiente apartado. El potenciómetro R_{11} se encarga de regular la tensión V_{IN} que controla la fuente de corriente.

Control de la I_{SET}:

Partimos de una tensión de entrada modulada de valor 0-3,3V. Si fijamos esta tensión a 3,3V analizamos que en la etapa de entrada tenemos:

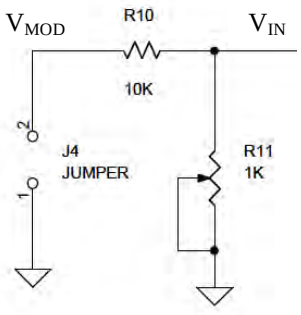


Ilustración 11 Esquema de la tensión de entrada modulada

Atendiendo a la configuración comentada al principio del apartado del OTA operando en base común tenemos:

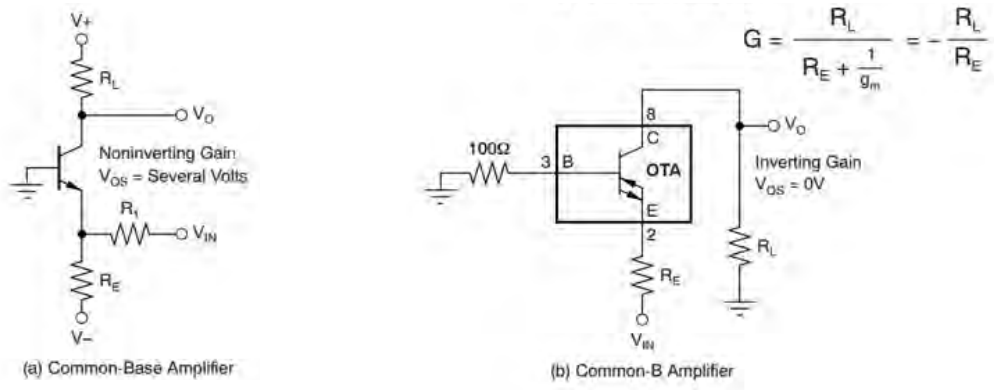


Ilustración 12 Análisis del OTA en base común

Como se puede ver el la Ilustración 12 la ganancia depende de la resistencia de carga R_L, en nuestro diseño tenemos una corriente de referencia, por lo que la ecuación queda transformada en la siguiente:

$$G_y = I_{SET} / V_{IN} = \frac{1}{R_{12} + \frac{1}{gm}} \qquad \text{[ecuación 1]}$$

Según las hojas de características:

$$I_Q = 11{,}2\text{mA} \rightarrow gm = 102\frac{mA}{V} \rightarrow \frac{1}{gm} = 10\Omega \qquad \text{[ecuación 2]}$$

Usando la ecuación [2] con la [1] y tomando R_{12} =10KΩ >> 10 Ω, la expresión queda reducida a:

$$I_{SET} / V_{IN} = \frac{1}{R_{12}} \qquad \text{[ecuación 3]}$$

Por lo que para un valor V_{IN} máximo = 0,3V tenemos una I_{SET} = 30 uA.
Como consecuencia, la corriente del fotodiodo monitor (I_{PD}) puede variar entre:

0 mA para R_{11} “arriba” (R_{11} = 0Ω)
30uA · 3 para R_{11} “arriba” (R_{11} = 1KΩ)

De esta forma, regulando el potenciómetro R_{11} podemos modificar la V_{IN} y a su vez fijar una corriente I_{SET} que posteriormente será utilizada en el integrado IC-WJZ como ya se ha comentado.

Corrección del offset del OPA860

Uno de los inconvenientes del OPA860 es el offset que genera, para ello le incorporamos un circuito de corrección de offset cuyo objetivo sea que para un V_{IN} = 0V tengamos un valor de I_{SET} = 0A. Antes de añadir este circuito, teníamos valores bastante considerables en I_{SET} para un V_{IN} = 0A.

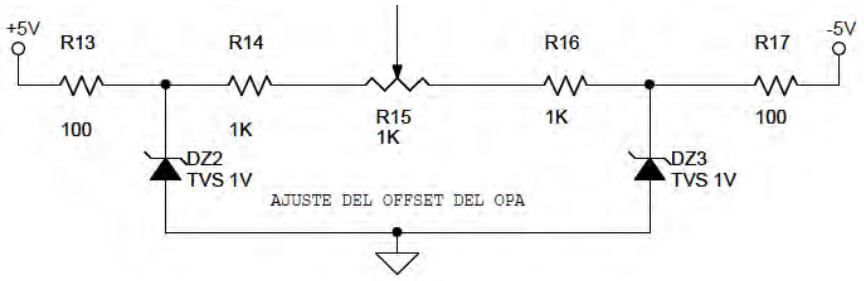


Ilustración 13 Circuito de corrección de Offset

En la Ilustración 13 podemos ver que hemos colocado dos diodos Zener que fijan un valor de tensión de 1V en los puntos A y B y que añadiendo dos resistencias de 1K conseguimos dos valores de tensión entre las patas del potenciómetro R_{15} de:

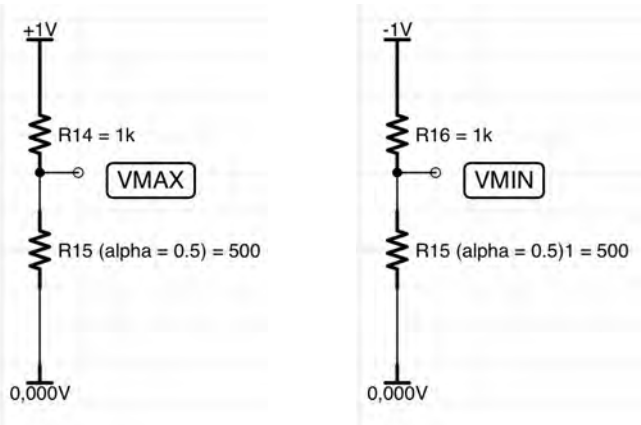


Ilustración 14 Calculo de los limites de tensión del potenciómetro

$$V_{MAX} = \frac{R15}{R15+R14} \qquad [ecuación\ 1]$$

$$V_{MAX} = \frac{500}{1K + 500} \cdot 1 = +0.33V$$

Por lo que usando la ecuación 1 para el circuito 2 tenemos que

V_{MIN} = - 0.33V

Rango de tensión es (-0.33, +0.33) V

3.1.3 Limitación de corriente máxima por el láser

Para limitar la corriente máxima que circula por el láser vamos a usar el LT6108-2 [5], que es un limitador de corriente que incorpora un dispositivo amplificador de detección de corriente, un voltaje de referencia integrado y un comparador.

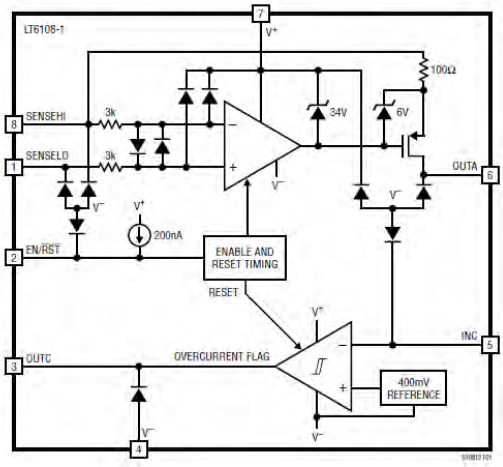


Ilustración 15 Análisis interno del LT6108-2

En la figurada descrita anteriormente podemos ver la configuración de los pines del LT6108. Es un componente formado por 8 pines, dos de alimentación (7 y 4), otros dos encargados de monitorizar la corriente I_{SET} (1 y 8), también cuenta con un pin OUTC encargado de cortar la corriente en caso de que el limitador de corriente salte (6), y con el pin 6 que es el que controla la corriente límite del fotodiodo.

Si integramos este elemento en nuestro circuito:

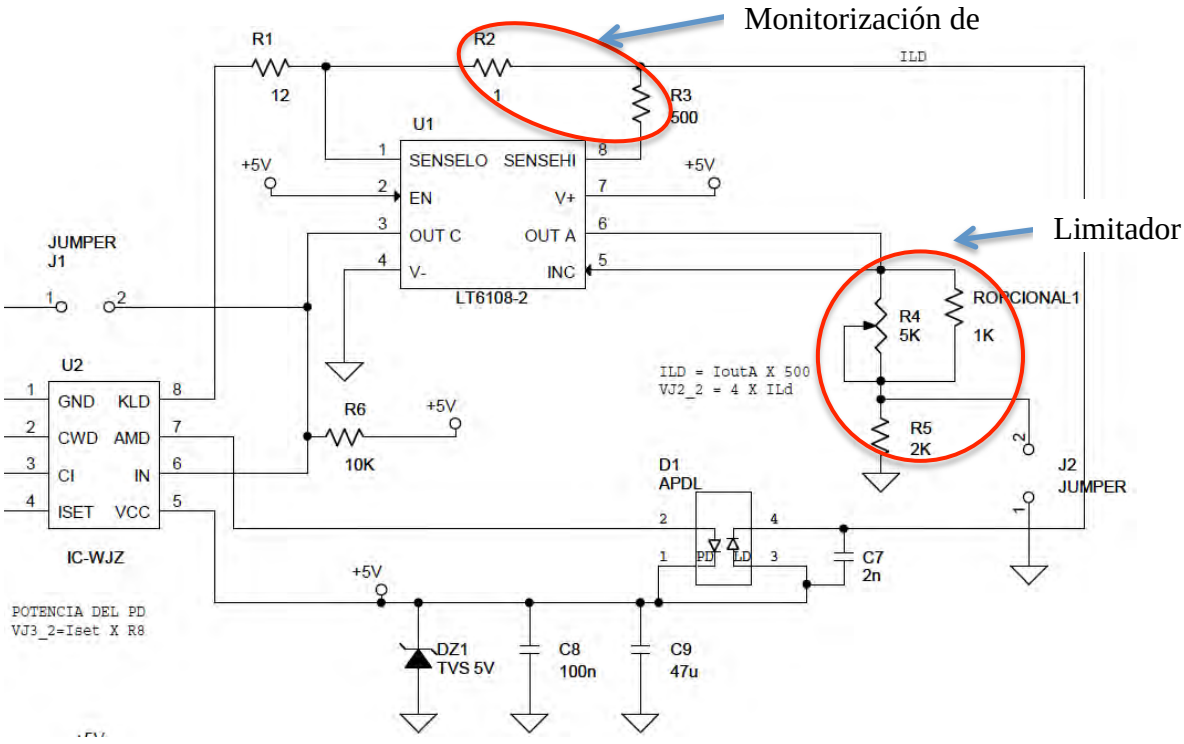


Ilustración 16 Esquema del Limitador de Corriente

El circuito proporciona en el pin OUTA una corriente proporcional a la corriente que circula por la carga (por el diodo laser). Según las hojas de características del fabricante del LT6108 [5] tenemos la siguiente ecuación:

$$I_{OUTA} = \frac{R_{sense} \cdot I_{LD}}{R_{IN}} \qquad [ecuación\ 1]$$

En el esquema de la Ilustración []:

R_{SENSE} es $R_2 = 1\ \Omega$
$R_{IN} = R_3 = 500\ \Omega$

El circuito proporciona una salida en colector abierto que se pone a '0' (se activa) cuando $V_{INC} > 400$ mV (tal y como se muestra en la Ilustración []). En mi circuito:

$$V_{INC} = I_{OUTA} \cdot [(\alpha \cdot R_4) + R_5)] \qquad [ecuación\ 2]$$

Siendo R4 el potenciómetro que determina la corriente máxima por el láser de valor máximo 5KΩ.

Cálculo del límite máximo y el límite mínimo de corriente por el láser.

El límite será máximo o mínimo dependiendo de la posición del potenciómetro:

* Si $\alpha = 1$:

$$V_{INC} = 400mV = I_{OUTA} \cdot 2k\Omega \qquad [ecuación\ 3]$$

$$I_{OUTA} = \frac{R_{sense} \cdot I_{LD}}{R_{IN}} = \frac{1\Omega \cdot I_{LD}}{500\Omega} \qquad [ecuación\ 4]$$

Combinando la *ecuación 3* y la *ecuación 4* tenemos que:

$$I_{LD\_min} = \frac{500\Omega \cdot 400mV}{2K\Omega \cdot 1\Omega} = 0.1A = 100\ mA$$

* Si $\alpha = 0$:

$$V_{INC} = 400mV = I_{OUTA} \cdot (2k\Omega + 5K\Omega) \quad \text{[ecuación 5]}$$

$$I_{OUTA} = \frac{R_{sense} \cdot I_{LD}}{R_{IN}} = \frac{1\Omega \cdot I_{LD}}{500\Omega} \quad \text{[}ecuación\ 6\text{]}$$

Combinando la *ecuación 5* y la *ecuación 6* tenemos que:

$$I_{LD\_max} = \frac{500\Omega \cdot 400mV}{2K\Omega + 5K\Omega} = 0.0286A = 28.6\ mA$$

3.2 Diseño

Una vez tenemos el esquemático hecho, nos fijamos a ver si todos los componentes tienen su huella asociada, y a continuación generamos la netslist y la cargamos con el programa Orcad Layout ya comentado anteriormente.
Llegado a este punto suele surgir un problema, y es que Orcad solo tiene en su base de datos huella generales, cuando utilizas componentes creados o específicos necesitas crear tu la huella y asociarla al nombre que le has dado en el esquemático.

3.2.1 Creación de huellas

Para crear la huella de un componente lo más importante es mirar la hoja de características que te proporciona el fabricante y basándote en las medidas de sus huellas de soldadura dibujas utilizando el editor de huellas de Orcad Layout.

Para este trabajo en concreto, fue necesario crear varias:

- **Láser**

La primera huella que se tuvo que crear es la del láser, ya que en nuestro nuevo diseño queríamos que el láser estuviese apoyado en la placa (dos de sus patas en la capa Top y las otras dos en la Bottom). Para ello es muy importante analizar dónde está el cátodo y el ánodo del diodo laser y del fotodiodo monitor.

Según la hoja de características del láser proporcionada por el fabricante y adjunta en el apartado anexos podemos ver los pines:

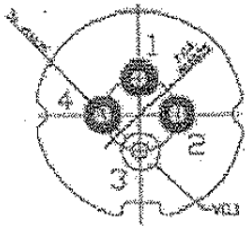


Ilustración 17 Patillaje del diodo Láser

Por lo que la configuración de los pines en el láser debe ser de la siguiente manera:

PIN	FUNCION
1	PD Cathode
2	PD Anode
3	LD Anode, GND
4	LD Cathode

Tabla 1 Pines del diodo láser

Por tanto, en nuestro esquemático el láser irá representado de la siguiente manera:

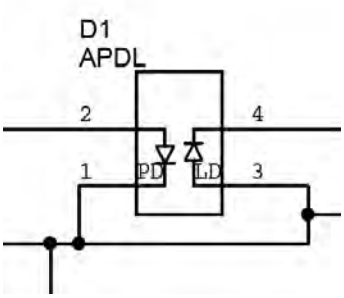


Ilustración 18 Esquema del diodo láser

Una vez conocida la función de cada pin, creamos la huella:

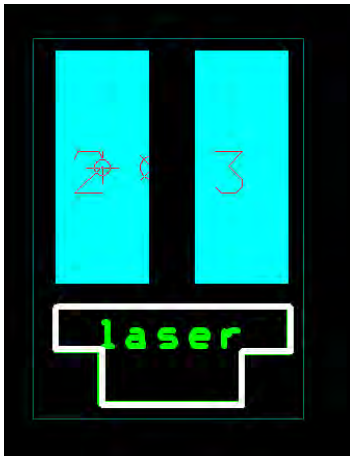


Ilustración 19 Capa Top de la huella del diodo láser

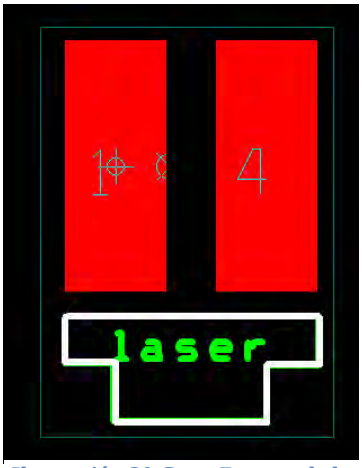


Ilustración 20 Capa Bottom de la huella del diodo láser

Como podemos ver la huella pertenece a la capa Top en la que soldaremos el pin 2 y 3 (PD Anode y LD Anode) mientras que en la capa Bottom irán el pin 1 y 4 (PD Cathode y LD Cathode). Quedando las patas del láser en la placa de la siguiente manera:

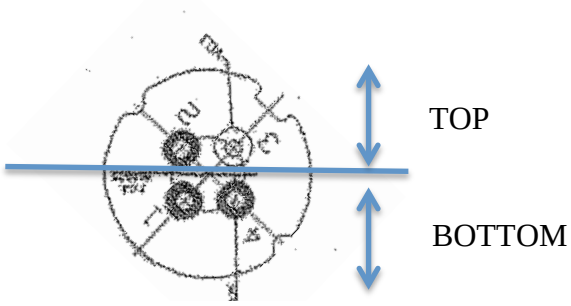


Ilustración 21 Colocación del diodo láser en la PCB

- **Potenciómetros**

Debido a que decidimos comprar unos potenciómetros que se adaptasen a nuestras necesidades, dos multi-vuelta de 1KΩ y 5KΩ y uno de montaje superficial de 1KΩ, tuvimos que fabricar sus huellas:

Para los potenciómetros que van a ser accesibles en la placa decidimos usar los de tipo Trimmer de 5 vueltas, y la huella a fabricar fue la siguiente:

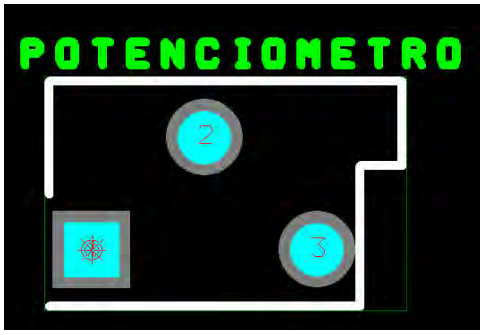


Ilustración 22 Capa Top de la huella del Potenciómetro

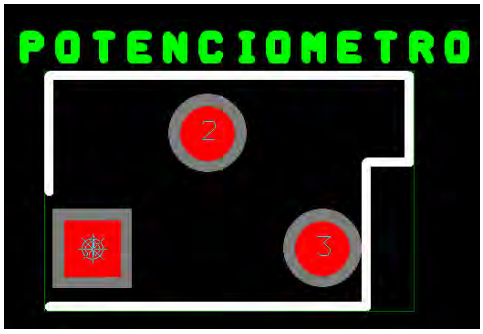


Ilustración 23 Capa Bottom de la huella del potenciómetro

Como se puede ver los tres pines de este potenciómetro son pasantes por lo que hay que poner soldadura tanto en la capa Top como en la Bottom.

En cambio, para el potenciómetro encargado del ajuste de offset usamos uno de montaje superficial y lo colocamos en la capa Bottom ya que solo lo graduaremos una vez y no será necesario tocarlo más.

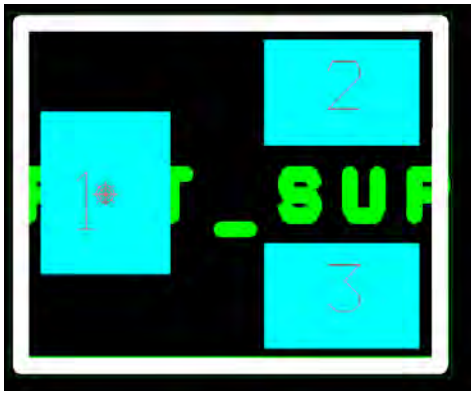


Ilustración 24 Huella del potenciómetro SMD

Inicialmente se hizo la huella para que la soldadura fuese en la capa Top, pero durante el rutado se modificó con un comando que tiene Layout y se colocó directamente el componente en la capa Bottom.

- **Diodo zener**

Por último, también fue necesario crearse la huella para un diodo Zener específico cuya hoja de características está adjunta en el anexo “Hoja de características”.

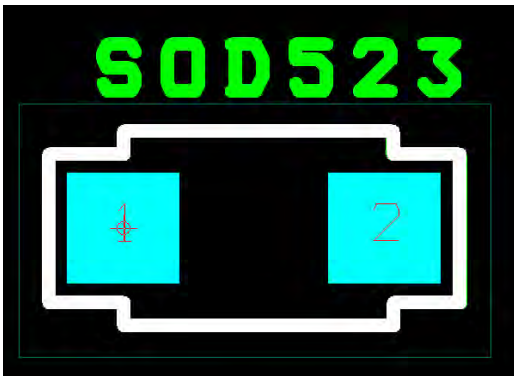


Ilustración 25 Huella del diodo Zener

3.2.2 Rutado de la PCB

Una vez creadas todas las huellas y haberlas asociado a su componente correspondiente podemos rutar la placa. En mi trabajo decidimos hacer un rutado a dos caras por ahorrar costes y por hacerla más visible. Elegimos poner el plano de masa en la capa Bottom, utilizamos un aclarado de 20 mils y el resultado final fue el siguiente:

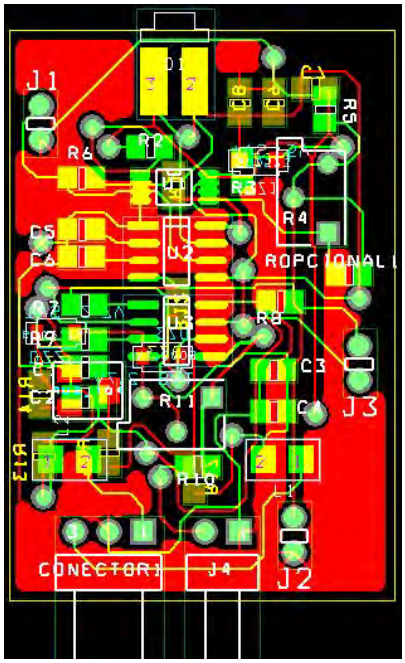


Ilustración 26 Rutado final de la PCB

Lo que más tiempo me ha llevado ha sido el rutado manual en el que se tuvieron que realizar las siguientes operaciones:

- **Se crearon rutas/uniones innecesarias**: Por ejemplo en la Ilustración 26 se puede ver la unión del pin 2 del CONECTOR 1 con masa, anteriormente esta unión estaba conectada a otro elemento unido a su vez con masa y el plano de masa aparecía dividido, la modificación por tanto fue cambiar esa unión y conectar el pin dos directamente con el plano de masa.

- **Algunos componentes no tenían posibilidad de ser unidos en la misma capa:** Tuve que colocar determinados componentes en la capa Bottom para liberar un poco las conexiones de la capa Top y poder unir todo. Un elemento que colocamos por ejemplo en la capa Bottom fue el condensador C_9 que estaba en la capa top y su conexión con el potenciómetro R_{15} resultaba imposible.

- También concluimos que el **potenciómetro R_{15}** cuya función es la de la corrección de offset ya comentada en el apartado 3.1.2 era innecesario que estuviese accesible en la placa ya que no iba a ser necesaria una reconfiguración, por lo que lo cambiamos por un potenciómetro de montaje superficial lo cual cambión un poco el diseño tal y como se puede ver en la Ilustración 26.

3.3 Elección de los componentes optoelectrónicos

Una vez fabricada la PCB, vamos a proceder a elegir los componentes que interactuarán con nuestro driver.
Vamos a emplear láseres comerciales del fabricante Alfa Photonics.

El emisor de referencia, encargado de presenciar agua o hielo, es el modelo **APLD-1310D-S5-A7A**, que trabaja a una longitud de onda de 1310 nm, con una corriente umbral de 6.2 mA y 0.47 mW⁄mA de eficiencia. Su fotodiodo monitor proporciona una corriente de 0.3763 mA cuando recibe una potencia de 5 mW.

El modelo **APLD-1490-cwdm-S5-A7A** se ha elegido para detectar agua, ya que presenta una longitud de onda de 1490 nm, con una eficiencia de 0.31 mW⁄mA, y una corriente umbral de 9.3 mA. La corriente en el fotodiodo monitor de 0.3026 mA para una potencia de 5 mW.

Por otro lado, el **APLD-1550D-S5-A7A** será encargado de detectar el hielo, con una longitud de onda de 1550 nm. Posee una corriente umbral de 7.7 mA, siendo la pendiente de eficiencia de 0.3 mW⁄mA, proporcionando el fotodiodo monitor 0.1662 mA para 5 mW.

En cuando al detector vamos a emplear un fotodiodo de área ancha de la casa *Thorlabs*, modelo **SM05PD6A** de germanio, con una respuesta espectral comprendida entre 800 y 1800 nm, margen que alberga las longitudes de onda de cada emisor.

Ilustración 27 Detector

Este modelo será polarizado en directa, el cátodo del fotodiodo puesto a masa. Entre otras características cabe destacar su área de visión de 7,1 mm^2 .

3.4 Montaje y puesta a punto

La placa ha sido soldada por la Oficina Técnica del departamento de Electrónica. Para ello previamente se tuvo que proporcionar lo siguiente:

- ✓ El diseño de la PCB con la extensión “.max”.
- ✓ El esquemático con la extensión “.opj” y “.dsn”.
- ✓ La lista de materiales y huellas adjunta en el anexo 6.2.
- ✓ Todos los componentes nombrados en la lista anterior.

3.5 Diseño final

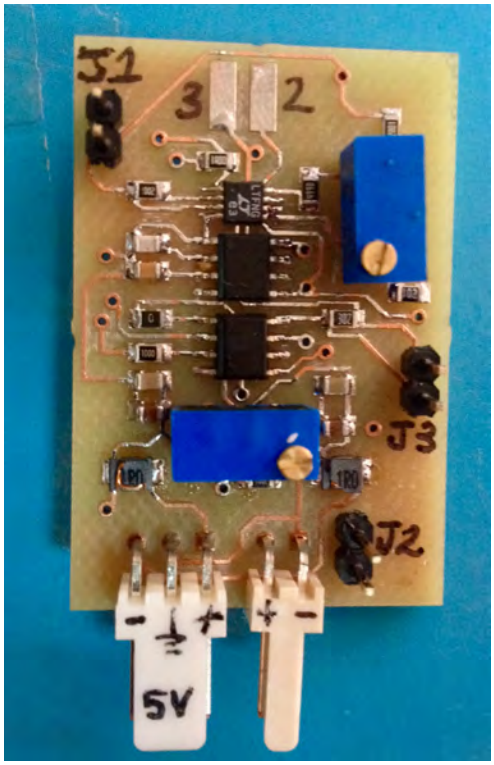


Ilustración 28 Capa Top del montaje final de la PCB

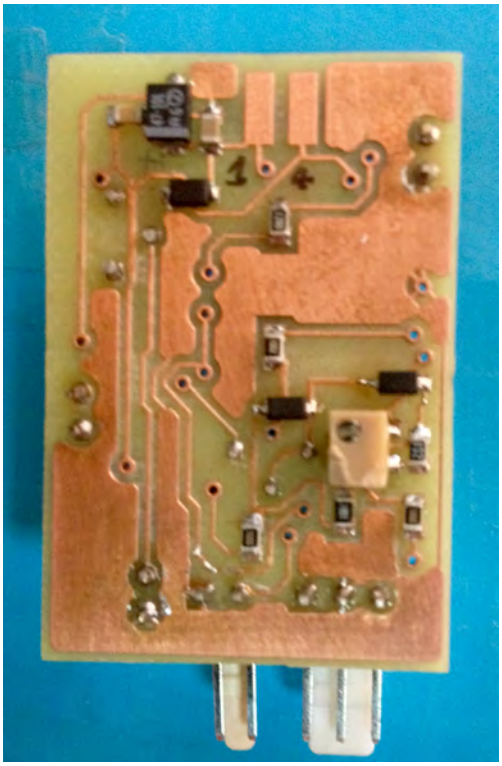


Ilustración 29 Capa Bottom del montaje final de la PCB

Como se puede ver en la Ilustración 28, tenemos dos conectores de alimentación uno a 5 voltios de la fuente y otro en el que irá la tensión de 5 voltios a diferentes puntos del circuito.

Por otro lado hemos marcado cada uno de los conectores Jumper para poderlos tener identificados en el circuito y poder ajustar el driver al laser que introduzcamos.

También se ve en la Ilustración 28 que hemos colocado los dos potenciómetros Trimmer encargados de ajustar la I_{SET} y el que limita la corriente por el láser. En cambio, en la Ilustración 29 se ve que hemos colocado en la capa Bottom el potenciómetro de montaje superficial encargado del ajuste de offset.

Por último me gustaría destacar que se han marcado los pines del láser para saber como soldarlo en el momento en el que se decida sustituirlo por otro.

4. Utilización

Las pruebas de este proyecto están basadas en introducir un láser en el circuito del driver y que este diodo láser sea capaz de emitir luz con la potencia deseada.

Partiendo de la siguiente tabla adjunta en el anexo "hojas de características" que recopila todas las características de uno de los tres diodos láser que vamos a manejar:

Parameter	Value	Dimensions
CW optical power, P_{op}	**5**	mW
Central wavelength at P_{op}, λ	**1310**	nm
Operating current, I_{op}	**16,8**	mA
Threshold current, I_{th}	**6,2**	mA
Monitor current, $I_{m\ op}$	**376,3**	uA
Efficiency	**0,47**	mW/mA
Package type	**TO-18**	
Cap	**Aspherical Lens Cap**	
Pin type	**A**	

Tabla 2 Características del laser de 1310 nm

Para introducir un láser en el circuito es necesario seguir los siguientes pasos:

4.1 Ajuste de los potenciómetros

En el circuito completo tenemos tres potenciómetros, uno de montaje superficial y dos regulables. Analizamos como habría que ajustar cada potenciómetro al introducir este láser en el circuito con el objetivo de que emita una potencia de 3mW p-p:

Potenciómetro 1 [R_{11}]

Partiendo de una tensión V_{mod} = 3,3 V:

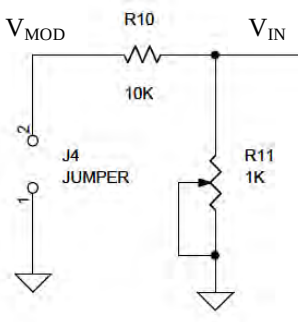


Ilustración 30 Circuito de análisis del potenciómetro R11

Este potenciómetro es el encargado de fijar un valor de tensión V_{IN} que a su vez es la encargada de fijar la corriente de referencia con el OPA860 por medio de la ecuación vista en apartados anteriores:

$$I_{SET} / V_{IN} = \frac{1}{R_{12}} \qquad [ecuación\ 1]$$

Para este láser en concreto, si cogemos los valores de la Tabla [], obtenemos:

$$P_o = 3\ mW \ \text{ y } \ Eficiencia = 0.47\ mW / mA$$

$$I_{SET} = \frac{1}{0.47} \cdot \frac{mA}{mW} \cdot 3\,mW = 6.38\ mA$$

Esto quiere decir que cuando conectemos el láser de 1310 nm a nuestro driver tendremos que girar el potenciómetro R_{11} hasta que tengamos una I_{SET} = 6.38 mA para conseguir una potencia de 3 mW.

Potenciómetro 2 [R_{15}]

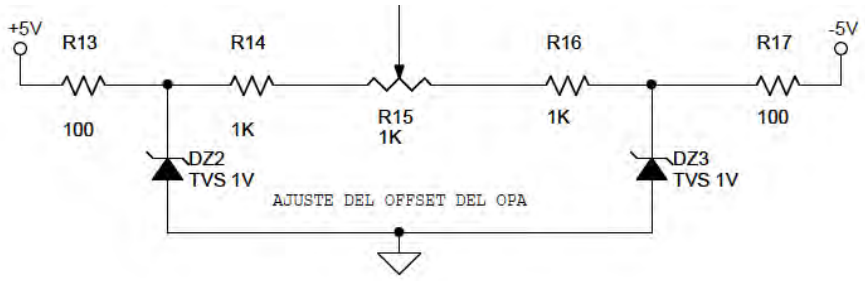


Ilustración 31 Circuito de análisis del potenciómetro R15

Este es el potenciómetro que pertenece al circuito de ajuste de offset del OPA860. Se ha decidido colocar un potenciómetro de montaje superficial, ya que una vez que se ajuste una vez este potenciómetro no va a ser necesario ajustarlo más, por lo que no es necesario que este accesible fuera del driver.

Como ya se ha calculado en otro apartado anterior, el rango de tensión de este potenciómetro oscila entre (-0.33, +0.33) V.

Potenciómetro 3 [R_4]

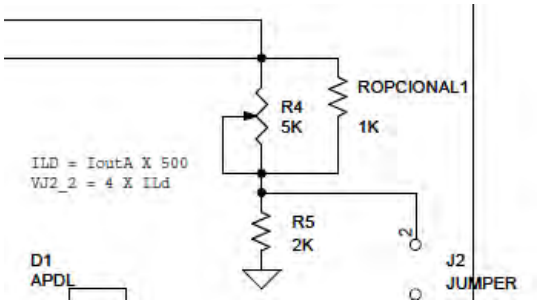


Ilustración 32 Circuito de análisis del potenciómetro R4

Este potenciómetro pertenece a la parte del circuito que se encarga de limitar la corriente que pasa por el láser. Como medida preventiva cada vez que introduzcamos un nuevo láser colocaremos el potenciómetro en la posición $\alpha = 0$ para que la limitación de corriente sea la máxima y apenas llegue corriente al láser y así estropearlo.

4.2 Corrección del offset

Para analizar este apartado vamos a basarnos en esta parte del circuito:

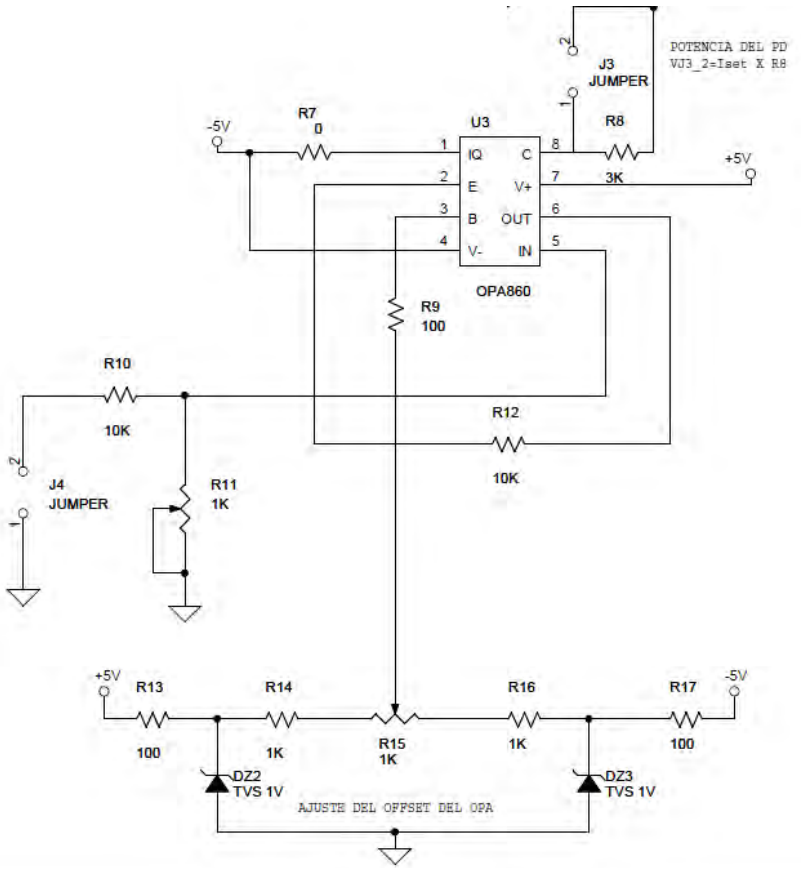


Ilustración 33 Circuito general de corrección de Offset

Como ya hemos comentado en apartados anteriores el potenciómetro encargado de corregir el offset es R_{15}. Lo que se trata de conseguir en la corrección del offset es que cuando yo ponga $V_{IN} = 0$, tengo que tener una $I_{SET} = 0$.

Por tanto lo primero que hacemos es colocar el potenciómetro R_{11} en la posición de arriba de tal manera que midamos la tensión de entrada en el OPA860 = 0 (pin 5).

Una vez conseguido esto necesitamos medir en algún punto de nuestro circuito I_{SET}. Para ello nos ayudamos del Jumper J3 cuya medida de tensión sigue la siguiente ecuación:

$$V_{J3\_Pin2} = I_{SET} \cdot R_8 \rightarrow I_{SET} = \frac{V_{J3\_Pin2}}{R_8} \qquad [ecuación\ 1]$$

Así que lo que tenemos que hacer es medir en V_{J3_Pin2} y regular el potenciómetro R_{15} hasta que veamos el valor 0.

4.3 Sustituir el láser por un circuito equivalente

Este apartado es simplemente un medio de seguridad. Ya que los diodos láser que utilizamos son un componente considerablemente caro, tal y como se puede ver en el anexo “Presupuesto” (apartado 6.1), debemos de ser precavidos y colocar en vez de un láser un circuito equivalente, yo he elegido un cortocircuito:

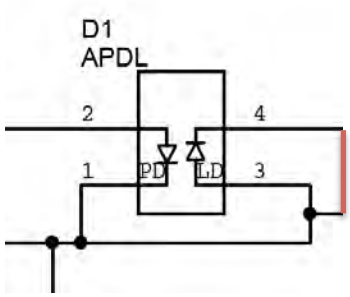


Ilustración 34 Circuito equivalente de un láser en cortocircuito

4.4 Fijar la corriente máxima

Otro medio de prevención antes de colocar el láser es fijar previamente la corriente máxima, como ya se ha explicado en apartados anteriores esto impediría que pasase una sobrecorriente por el láser y lo estropease. Para analizar este apartado nos fijaremos en esta parte del circuito:

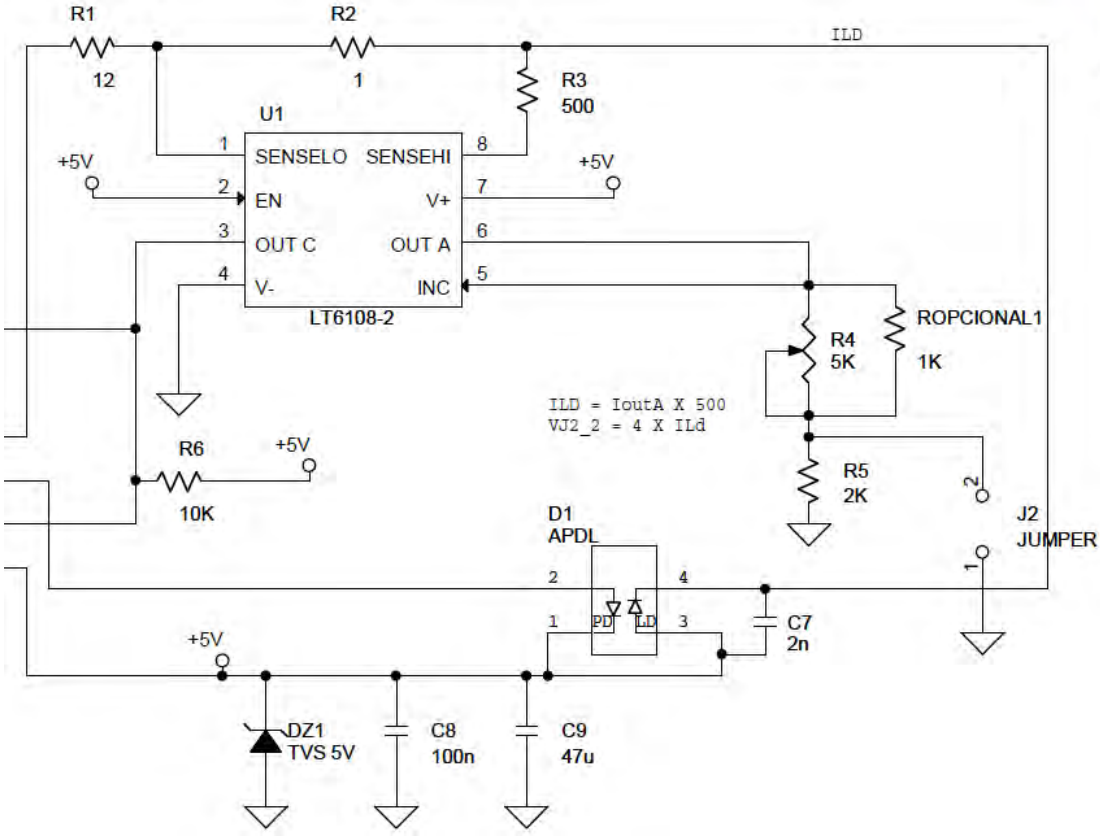


Ilustración 35 Circuito del limitador de corriente

Para medir la corriente que pasa por el láser tenemos que medir en el Jumper J2, dividiendo el valor medido entre 4 nos dará el valor de la corriente que circula por el diodo láser, esta operación proviene del siguiente planteamiento.

Partiendo de la ecuación [6] del apartado 3.1.3, obtenida de un análisis previo tenemos que:

$$I_{OUTA} = \frac{R_{sense} \cdot I_{LD}}{R_{IN}} = \frac{1\Omega \cdot I_{LD}}{500\Omega} \qquad [1]$$

Por tanto:

$$I_{LD} = 500 \cdot I_{OUTA} \qquad [2]$$

Como

$$V_{J2_{pin2}} = I_{OUTA} \cdot R_5 \quad entonces \ \frac{1\Omega \cdot I_{LD}}{500\Omega} \cdot 2K\Omega$$

Así que:

$$V_{J2_{pin2}} = 4 \cdot I_{LD} \qquad [3]$$

Finalmente se puede concluir, que con la ecuación [2] y la ecuación [3] podemos fijar un valor de la corriente que queremos que pasar por el diodo láser, por lo que medimos en el jumper J2 al mismo tiempo que giramos el potenciómetro R_4 hasta conseguir el valor de:

$$I_{LD\_max} = 28.6 \text{ mA}$$

obtenido en el apartado 3.1.3.

5. Conclusiones

El objetivo de partida de este trabajo de final de grado era el diseño y la calibración de un circuito driver para varios diodos láser. Por tanto el resultado fundamental de este proyecto se resume en afirmar la viabilidad técnica del circuito driver, su correcto funcionamiento y la correcta calibración para cualquier láser.

En primer lugar se ha realizado un estudio y análisis del circuito driver explicando cada una de sus partes y sus funciones. Por otro lado se ha fabricado una PCB basada en ese circuito y en la fabricación de determinadas huellas, comprobando en su montaje que el diseño y tamaño de las huellas era el correcto. Por último se han explicado todos los pasos a seguir en la calibración de un láser cuando es soldado al circuito driver.

En la realización de este proyecto fin de carrera se han utilizado y ampliado los conocimientos adquiridos a lo largo de la carrera, en especial las asignaturas fabricación de componentes electrónicos, instrumentación y electrónica analógica.

6. Anexos

6.1 Presupuesto

Coste de personal			
Descripción	**Coste unitario**	**Cantidad**	**Importe total**
Personal de oficina técnica y montaje	$20\ €/_{h}$	5 h	250 €
Coste total del personal			250 €

Tabla 3 Coste de personal

Coste de material			
Descripción	**Coste unitario**	**Cantidad**	**Importe total**
APLD-1310D-S5-A7A	275 €	1	275 €
APLD-1490-cwdm-S5-A7A	275 €	1	275 €
APLD-1550D-S5-A7A	275 €	1	275 €
IC-WJZ	1 €	1	1 €
LT6108-2	3,85 €	1	3,85 €
OPA860	5,80 €	1	5,80 €
Diodo ZENER	0,84 €	3	2,52 €
Resistencias	0,07 €	15	1,54 €
Potenciómetro SMD (R_{11})	5,65 €	1	5,65 €
Potenciómetro R_{15} y R_4	1,48 €	2	1,48 €
Condensador	0,08 €	9	0,72 €
Bobina	1,01 €	2	2,02 €
Conector 2 pines	0,173 €	1	0,173 €
Conector 3 pines	0,567 €	1	0,567 €
Conectores Jumper	0,496 €	3	1,488 €
Coste total de componentes			**851.808€**

Tabla 4 Coste de material

Resumen del presupuesto

Descripción	Importe total
Coste de personal	250 €
Coste de material	851.808 €
Total presupuesto	**1101.808** €

Tabla 5 Resumen del presupuesto

6.2 Lista de materiales

UNIT	QUANTITY	COMPONENT	VALUE	FOOTPRINT	FARNELL
1	1	CONECTOR1	CONN TRBLK 3	BLKCON.100/RH/TM1SQ/W.425/3	1462932
2	2	C1,C3	100n	SM/0805	644160
3	2	C2,C4	2.2u	SM/0805	1833811
4	1	C5	10p	SM/0805	1855771
5	1	C6	22n	SM/0805	1288269
6	1	C7	2n	SM/0805	1740501
7	1	C8	100n	SM/0805	644160
8	1	C9	47u	SM/0805	1754168
9	1	DZ1	TVS 5V	SOD523	1829265
10	2	DZ2,DZ3	TVS 2.7V	SOD27V	1459115
11	1	D1	APLD	LASER_R	LASER
12	3	J1,J2,J3	JUMPER	JUMPER100	9728953
13	1	J4	JUMPER	BLKCON.100/RH/TM1SQ/W.425/2	1756797
14	1	L1, L2	1uH	SM/L1	1800375
15	1	R11	1k	POTENCIOMETRO	9352643
16	1	R15	1k	POT_SUP	514871
17	3	ROPCIONAL1,R14,R16	1k	SM/0805	1360934
18	1	R1	12	SM/0805	1697404
19	1	R2	1	SM/0805	1717799
20	1	R3	500	SM/0805	1160132
21	1	R4	5K	POTENCIOMETRO	9352643
22	1	R5	2K	SM/0805	1469764
23	3	R6,R10,R12	10K	SM/0805	1697445
24	1	R7	0	SM/0805	1652903
25	1	R8	3K	SM/0805	1653032
26	3	R9,R13,R17	100	SM/0805	1652907
27	1	U1	LT6108-2	SM/MSOP/.025/08/WB.260/L.120	2097861
28	1	U2	IC-WJZ	SOG.050/8/WG.244/L.200	-
29	1	U3	OPA860	SOG.050/8/WG.244/L.200	-

Tabla 6 Lista de materiales

6.3 Hojas de características

iC-WJ, iC-WJZ
LASER DIODE DRIVER

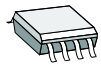
FEATURES

- Laser diode driver for continuous and pulsed operation (CW to 300 kHz) up to 250 mA
- Averaging control of laser power
- Simple adjustment of the laser power via external resistor
- Adjustable watchdog at the switching input to protect the laser diode
- Soft-start after power-on
- Driver shutdown with overtemperature and undervoltage
- Single 5 V supply
- Simple circuitry
- **iC-WJ** for laser diodes with 50 to 500 µA monitor current
- **iC-WJZ** for laser diodes with 0.15 to 1.5 mA monitor current

APPLICATIONS

- General purpose laser diode driver

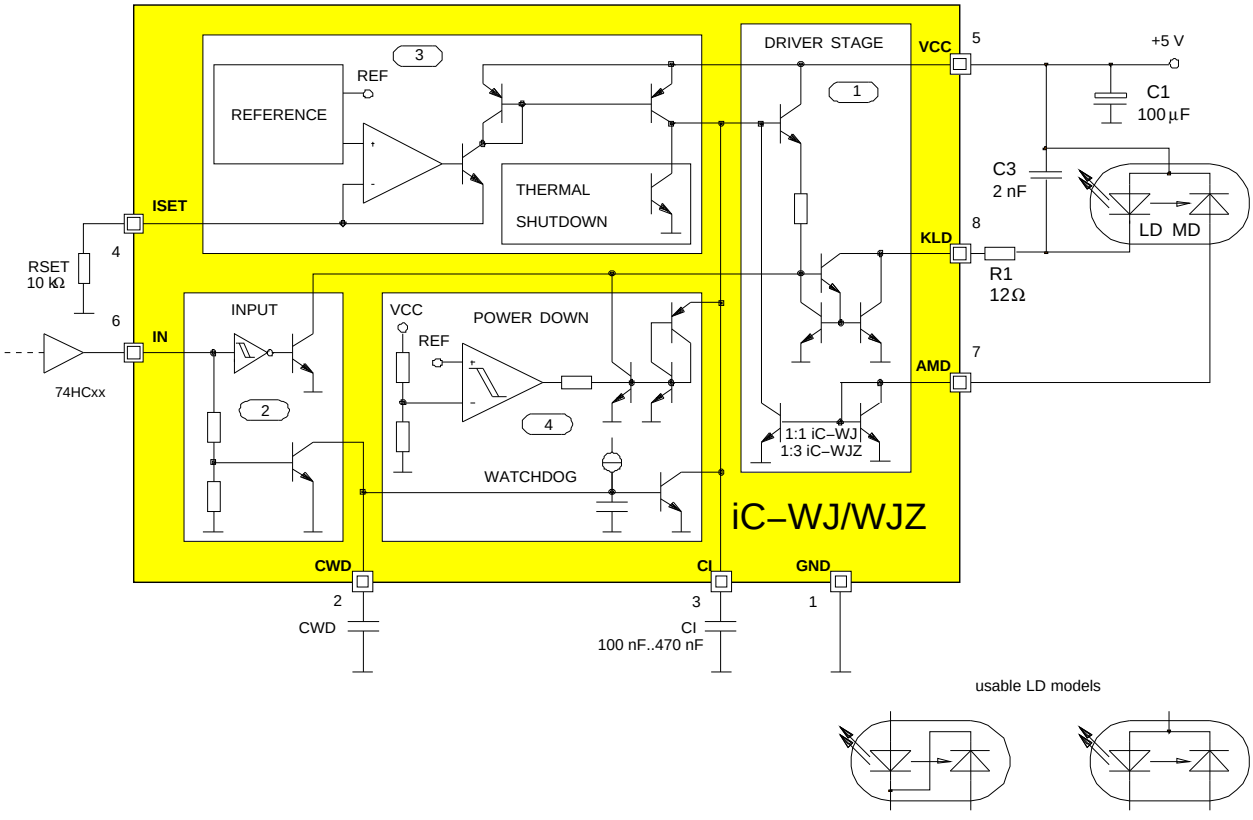
PACKAGES



SO8

MSOP8

BLOCK DIAGRAM



DESCRIPTION

The iC-WJ and iC-WJZ devices are driver ICs for laser diodes in continuous and pulsed operation up to 300 kHz. The laser diode is activated via switching input IN. A control to the mean value of the optical laser power and integrated protective functions ensure nondestructive operation of the sensitive semiconductor laser.

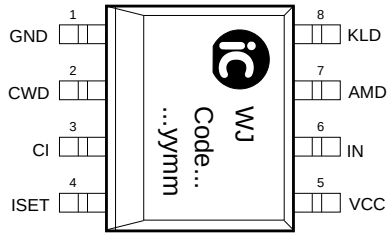
The IC contains protective diodes to prevent destruction due to ESD, a protective circuit to guard against overtemperature and undervoltage and a soft-start for the laser diode driver to protect the laser diode when switching on the supply voltage.

An external resistor at ISET is utilised to adapt the power control to the laser diode being used. The capacitor at CI determines the recovery time constants and the start-up time.

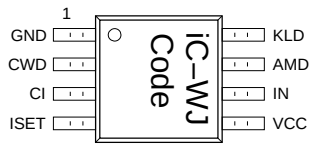
A watchdog circuit monitors the switching input IN. If IN remains low longer than preset by the capacitor at CWD, the capacitor of the power control is discharged at pin CI. This ensures that the current through the laser diode during the next high pulse at input IN is not impermissibly high.

PACKAGES SO8, MSOP8 to JEDEC Standard

PIN CONFIGURATION SO8
(top view)



PIN CONFIGURATION MSOP8
(top view)



PIN FUNCTIONS

No.	Name	Function
1	GND	Ground
2	CWD	Capacitor for Watchdog
3	CI	Capacitor for Power Control
4	ISET	Attachment for RSET
5	VCC	5 V Supply Voltage
6	IN	Input
7	AMD	Anode Monitor Diode
8	KLD	Cathode Laser Diode

ABSOLUTE MAXIMUM RATINGS

Beyond these values damage may occur; device operation is not guaranteed.

Item No.	Symbol	Parameter	Conditions	Fig.	Min.	Max.	Unit
G001	VCC	Supply Voltage			0	6	V
G002	I(CI)	Current in CI			-4	4	mA
G003	V(KLD)	Voltage at KLD	IN = lo		0	6	V
G004	I(KLD)	Current in KLD	IN = hi		-4	600	mA
G005	I(AMD)	Current in AMD	**iC-WJ** **iC-WJZ**		-4 -6	4 6	mA mA
G006	I(IN)	Current in IN			-10	2	mA
G007	I(ISET)	Current in ISET			-2	2	mA
G008	I(CWD)	Current in CWD	IN = lo		-2	2	mA
G009	Vd()	ESD Susceptibility at CWD, CI, ISET, IN, AMD, KLD	MIL-STD-883, HBM 100 pF discharged through 1.5 kΩ			1.5	kV
G010	Tj	Junction Temperature			-40	150	°C
G011	Ts	Storage Temperature			-40	150	°C

THERMAL DATA

Operating Conditions: VCC = 5 V ±10 %

Item No.	Symbol	Parameter	Conditions	Fig.	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range (extended temperature range on request)			-25		90	°C
T02	Rthja	Thermal Resistance Chip to Ambient	surface mounted on PCB, without special cooling				140	K/W

All voltages are referenced to ground unless otherwise stated.
All currents into the device pins are positive; all currents out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating Conditions: VCC = 5 V ±10 %, RSET = 2.7...27 kΩ,
iC-WJ: I(AMD) = 50...500 µA, **iC-WJZ**: I(AMD) = 0.15...1.5 mA, Tj = -25...125 °C, unless otherwise noted.

Item No.	Symbol	Parameter	Conditions	Tj °C	Fig.	Min.	Typ.	Max.	Unit
Total Device									
001	VCC	Permissible Supply Voltage Range				4.5		5.5	V
002	Iav(VCC)	Supply Current in VCC (average value)	Iav(KLD) = 100 mA, f(IN) = 200 kHz ±20 %					15	mA
003	tp(IN-KLD)	Delay Time Pulse Edge V(IN) to I(KLD)	IN(hi ↔ lo), V(50 %) : I(50 %)					135	ns
004	Vc()lo	Clamp Voltage lo at VCC, IN, AMD, KLD, CI, CWD, ISET	I() = -2 mA, other pins open			-1.5		-0.3	V
005	Vc()hi	Clamp Voltage hi at IN, AMD, KLD, GND, CI, CWD, ISET	Vc()hi = V() − VCC; I() = 2 mA, other pins open			0.3		1.5	V
Driver									
101	Vs(KLD)	Saturation Voltage at KLD	IN = hi, I(KLD) = 200 mA					1.3	V
102	I0(KLD)	Leakage Current in KLD	IN = lo, V(KLD) = VCC					10	µA
103	I(KLD)	Current in KLD	IN = hi, I(AMD) = 0	-25 27 70 125		225 250 250 250	250		mA mA mA mA
104	V(AMD)	Voltage at AMD	**iC-WJ:** I(AMD) = 500 µA **iC-WJZ:** I(AMD) = 1.5 mA			0.5 0.4		1.5 1.5	V V
105	tr	Current Rise Time in KLD	Imax(KLD) = 20...250 mA, Ip(): 10 → 90 %					100	ns
106	tf	Current Fall Time in KLD	Imax(KLD) = 20...250 mA, Ip(): 90 % → 10 %					100	ns
107	CR1()	Current Ratio I(AMD) / I(ISET)	I(CI) = 0, closed control loop; **iC-WJ** **iC-WJZ**			 0.8 2.4	 1 3	 1.2 3.6	
108	CR2()	Current Ratio I(AMD) / I(CI)	V(CI) = 1...3.5 V, ISET open; **iC-WJ** **iC-WJZ**			 0.9 2.7	 1 3	 1.1 3.3	
Input IN									
201	Vt()hi	Threshold hi		 -25 27 70 125		1.60	 1.84 1.87 1.88 1.91	2.40	V V V V V
202	Vt()lo	Threshold lo		 -25 27 70 125		1.50	 1.76 1.78 1.79 1.81	2.20	V V V V V
203	Vt()hys	Hysteresis		 -25 27 70 125		10	 80 90 90 100	190	mV mV mV mV mV
204	Rin	Pull-Down Resistor	V(IN) = -0.3...VCC + 0.3 V			4		16	kΩ
205	V0()	Open-loop Voltage	I(IN) = 0					0.1	V
206	Vtwd()	Threshold for Watchdog		-25 27 70 125		2.4 2.0 1.5 1.0		3.2 2.8 2.3 1.8	V V V V
Reference und Thermal Shutdown									
301	V(ISET)	Voltage at ISET		 27		1.17	 1.22	1.28	V V
302	CR()	Current Ratio I(CI) / I(ISET)	V(CI) = 1...3.5 V, I(AMD) = 0			0.9	1	1.1	

ELECTRICAL CHARACTERISTICS

Operating Conditions: VCC = 5 V ±10 %, RSET = 2.7...27 kΩ,
iC-WJ: I(AMD) = 50...500 µA, **iC-WJZ**: I(AMD) = 0.15...1.5 mA, Tj = -25...125 °C, unless otherwise noted.

Item No.	Symbol	Parameter	Conditions	Tj °C	Fig.	Min.	Typ.	Max.	Unit
303	RSET	Permissible Resistor at ISET (Control Set-up Range)				2.7		50	kΩ
304	Toff	Thermal Shutdown Threshold				125		150	°C
305	Thys	Thermal Shutdown Hysteresis				10		40	°C
Power-Down and Watchdog									
401	VCCon	Turn-on Threshold VCC		27		3.5	3.8	4.3	V V
402	VCCoff	Undervoltage Threshold at VCC				3.2		3.8	V
403	VCChys	Hysteresis	VCChys = VCCon − VCCoff	27		300	400	450	mV mV
404	Vs(CI)off	Saturation Voltage at CI with undervoltage	I(CI) = 300 µA, VCC < VCCoff					1.6	V
405	Vs(CI)wd	Saturation Voltage at CI with IN = lo	I(CI) = 300 µA, t(IN = lo) > tp (*)					1.5	V
406	Ipu(CWD)	Pull-Up Current at CWD	V(CWD) = 0, IN = lo			-15		-3	µA
407	tpmin	Min. Activation Time for Watchdog	IN = lo, CWD open			10		45	µs
408	Kwd (*)	Constant for Calculating the Watchdog Activation Time	IN = lo			0.19	0.38	0.57	µs/pF

(*) tp = (C(CWD) ∗ Kwd) + tpmin (see Applications Information)

APPLICATIONS INFORMATION

Laser Power Adjustment
The iC-WJ and iC-WJZ devices can be adapted to CW laser diodes from approximately 2 to 40 mW. N- and M-type models can be used.

The pin ISET is used for the adjustment to the sensitivity of the monitor diode and to set the desired optical laser power. The setpoint for the averaging control of the monitor diode current is preset at this pin.

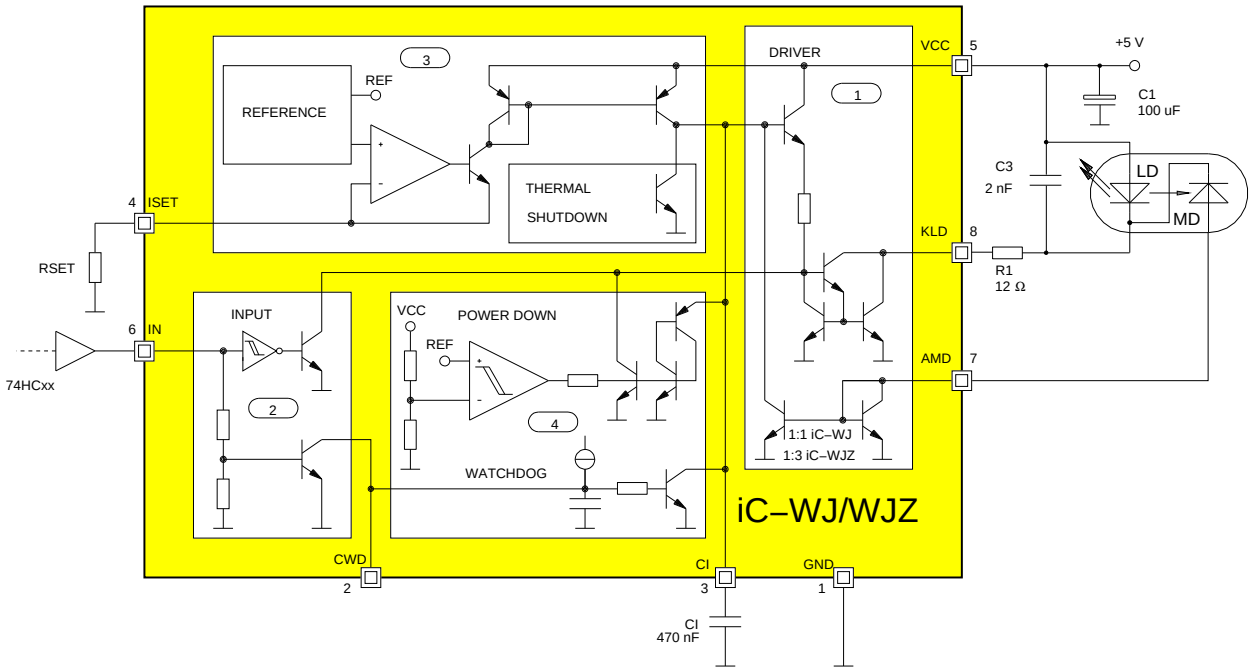


Figure 1: Operation of a laser diode according to the example

To calculate the current required at ISET, the average optical laser power is to determine:

$$P_{av} = P_{peak} * \frac{t_{whi}}{T}$$

with peak value P_{peak} and pulse/period duration t_{whi}/T.

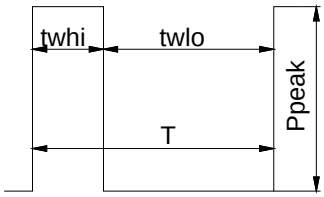


Figure 2: Duty cycle

Example iC-WJ
Laser diode with 5 mW maximum optical output, monitor diode with 0.13 mA/mW, pulse duty factor set to 20 % with P_{peak} = 5 mW:

The resulting average optical power is 1 mW and the average monitor diode current is 0.13 mA. The resistor RSET is calculated as:

$$RSET = \frac{CR1 * V(ISET)}{I_{av}(AMD)} = \frac{1 * 1.22\,V}{0.13\,mA} = 9.4\,k\Omega$$

with the Electrical Characteristics No. 301 for V(ISET) and No. 108 for current ratio CR1.

Example iC-WJZ
Laser diode with 5 mW maximum optical output, monitor diode with 0.75 mA at 3 mW, CW operation (pulse duty factor 100 %) with P_{cw} = 1 mW:

For the monitor diode current of 0.25 mA the resistor RSET is calculated as:

$$RSET = \frac{CR1 * V(ISET)}{I_{av}(AMD)} = \frac{3 * 1.22\,V}{0.25\,mA} = 14.6\,k\Omega$$

with Electrical Characteristics No. 301 for V(ISET) and No. 108 (iC-WJZ) for current ratio CR1.

Averaging control
The control of the average optical laser power requires a capacitor at pin CI. This capacitor is used for averaging and must be adjusted to the selected pulse repetition frequency and the charging current preset with RSET. The ratios are linear in both cases, i.e. the capacitor CI must be increased in size proportionally as the pulse repetition frequency slows or the current from ISET increases:

$$CI \geq \frac{440 * I(ISET)}{f * V(ISET)} = \frac{440}{f * RSET}$$

Example
Pulse repetition frequency 100 kHz, RSET = 10 kΩ:
CI = 440 nF, chosen 470 nF.

Otherwise the charging of the capacitor CI during the pulse pauses (with I(ISET) = 1.22 V / RSET) will create an excessive mean value potential and may destroy the laser diode during the next pulse. The capacitor CI is correctly dimensioned when the current through the laser diode and the optical output signal do not show any overshots following the rising edge.

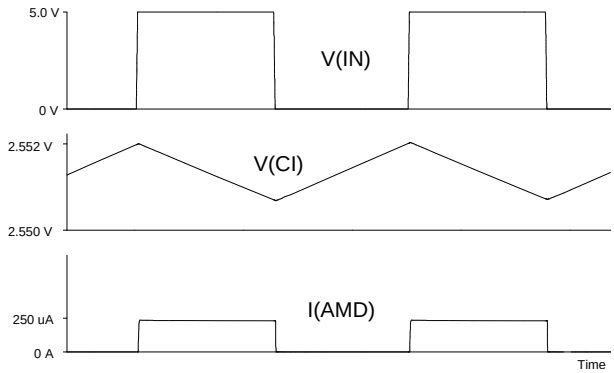


Figure 3: Steady-state averaging control, f(IN) = 100 kHz (1:1), CI = 470 nF, RSET = 10 kΩ

In steady-state condition and for a pulse duty factor of 50 % (pulse/pause 1:1), signals as shown in Figure 3 are present at the IC pins.

Figure 4 shows the corresponding signals for a pulse duty factor of 20 %. The influence of the pulse duty factor on the peak value of the monitor current proportional to the laser current is apparent. The average kept constant by the control (RSET unchanged) means a peak value increased by the factor 2.5. The pulse duty factor for which RSET was dimensioned should therefore be kept constant if possible.

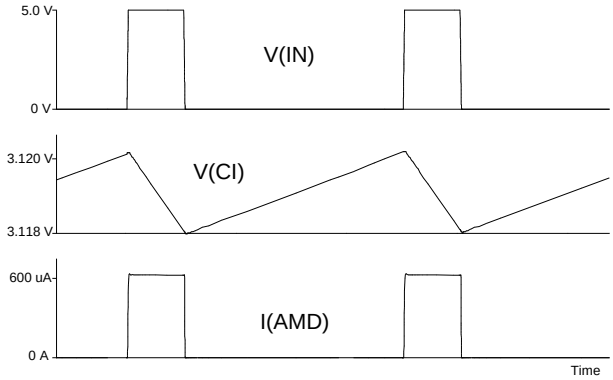


Figure 4: Steady-state averaging, f(IN) = 100 kHz (1:4), CI = 470 nF, RSET = 10 kΩ

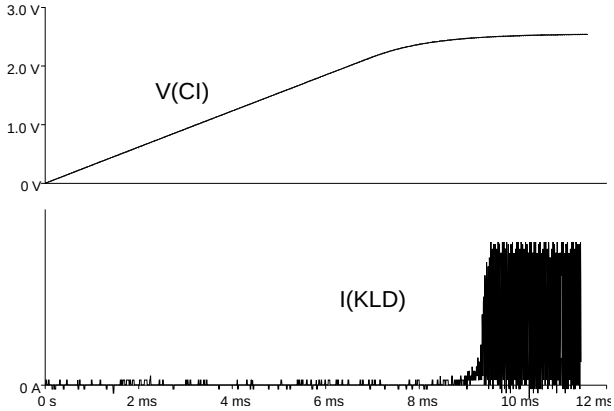


Figure 5: Turn-on behavior, f(IN) = 100 kHz (1:1), CI = 470 nF, RSET = 10 kΩ

Turn-on and turn-off behavior
Capacitor CI also determines the starting time from switching on the supply voltage VCC to steady-state laser pulse operation or after a discharge of CI by the watchdog. The following applies to estimating the starting time (Figure 5):

$$T_{on} = \frac{2.5\,V * CI}{I(ISET)} = \frac{2.5\,V * CI * RSET}{1.22\,V}$$

Example
CI = 470 nF, RSET = 10 kΩ: T_{on} = 9.6 ms

Figure 6 shows a detailed view of the start of laser operation; Figure 7 shows the shut-down behavior. The decline in the voltage at CI and the absence of the laser pulses are signs that the undervoltage detector is active.

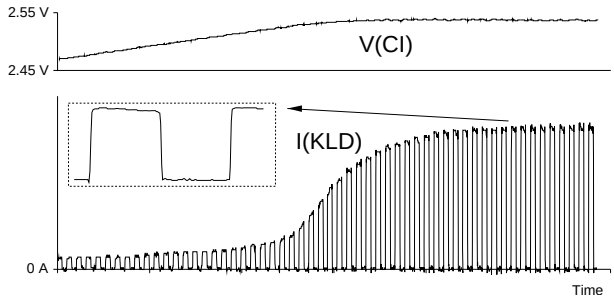


Figure 6: Turn-on behavior, detailed view f(IN) = 100 kHz (1:1), CI = 470 nF, RSET = 10 kΩ

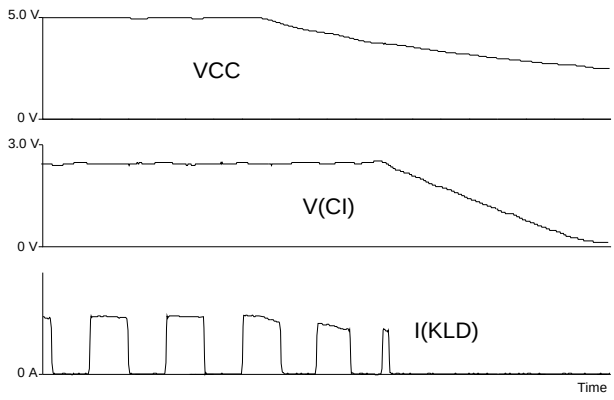


Figure 7: Turn-off behavior, f(IN) = 100 kHz (1:1), CI = 470 nF, RSET = 10 kΩ

Watchdog
In order for the watchdog to function correctly, the input IN must be activated with a CMOS output (e.g. with an HCMOS gate: see Figure 1).

The watchdog ensures that the capacitor CI is discharged during protracted pulse pulses at IN. During the pulse pauses the potential at CI increases by ΔV (Figure 3):

$$\Delta V = \frac{I(ISET) * t_{wlo}}{CI}$$

The discharge of capacitor CI by the watchdog protects the laser diode from being destroyed by an excessive turn-on current during the next pulse.

The capacitor CWD should be dimensioned such that the response time t_p of the watchdog is slightly longer than the pulse pause t_{wlo} of the input signal. As a result, the watchdog is just short of being activated.

For response times t_p longer than t_{pmin} applies:

$$CWD = \frac{t_p - t_{pmin}}{K_{wd}}$$

with t_{pmin} and K_{wd} from Electrical Characteristics No. 407, 408.

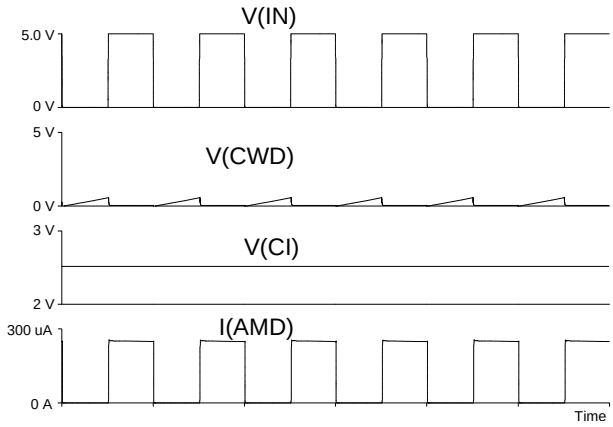


Figure 8: Watchdog, CWD open, f(IN) = 100 kHz (1:1), CI = 470 nF, RSET = 10 kΩ

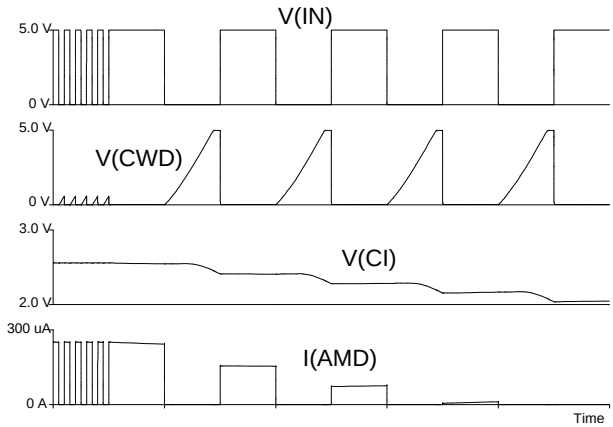


Figure 9: Watchdog, CWD open, f(IN) = 100 kHz → 10 kHz (1:1), CI = 470 nF, RSET = 10 kΩ

Figure 8 shows the signals during normal operation, without the watchdog being activated. The potential at CWD rises during pulse pauses but does not reach the watchdog activation threshold.

Figure 9 shows the watchdog behavior when the input frequency is reduced from 100 kHz to 10 kHz. The pulse pauses are longer than the watchdog's response

time. The watchdog begins to discharge the capacitor CI current limited. The remaining charge time during the pulse pauses before further watchdog intervention is not sufficient to maintain the initial potential at CI. The potential is thus gradually reduced until it reaches the saturation voltage $Vs(CI)_{wd}$ (Electrical Characteristics No. 405).

The watchdog therefore protects the laser diode from destruction when the input signal change in such a manner that the capacitor CI is not longer adequate for averaging.

Furthermore, the introduction of the watchdog permits long pulse pauses and activation of the laser diode with pulse packets.

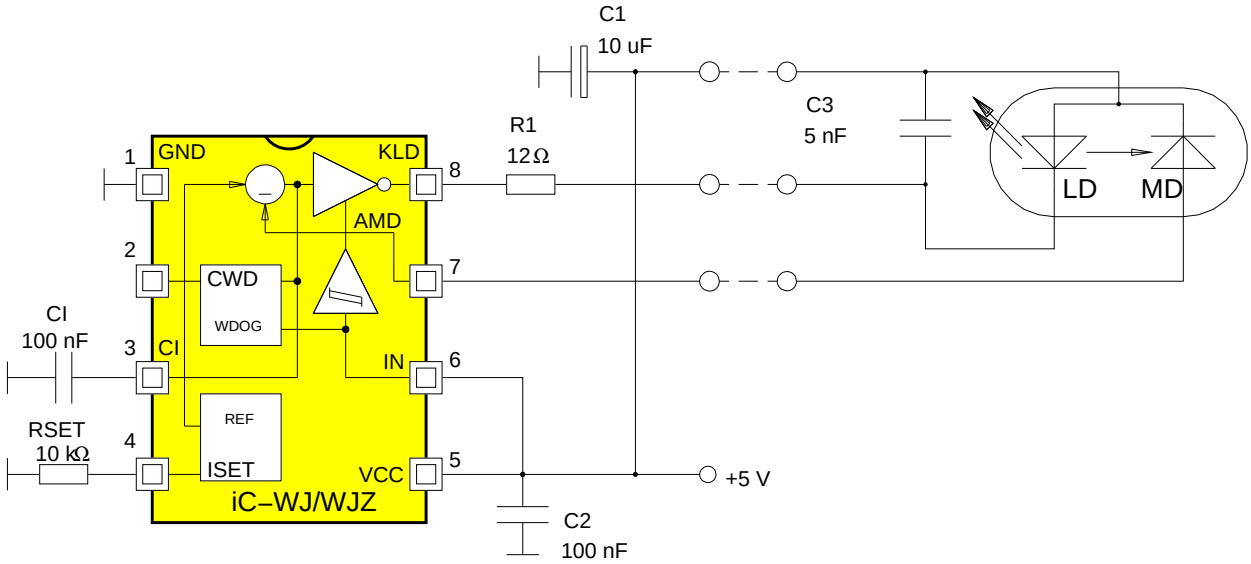


Figure 10: CW operation via cable

CW Operation
In case of CW operation, the input IN can be connected to the power supply VCC. The pin CWD may be left open, because the capacitor for the watchdog is not necessary. The capacitor CI for the averaging control can be reduced to 100 nF.

Operation of laser diode via cable
It is recommended to connect a capacitor of 1 to 10 nF across the laser diode in order to protect the laser diode against destruction due to ESD or transients. This capacitor should be placed close to the laser diode and not at the beginning of the LD supply line.

An approx. 12 Ω series resistor at pin KLD reduces the IC power consumption and damps possible resonances of the load circuit caused by the inductive LD supply line. This resistor is useful for many applications, also for those which do not operate via cable.

On a PCB the forward path VCC to the laser diode should be arranged in parallel with the return path to KLD even when the line is only a few centimeters in length.

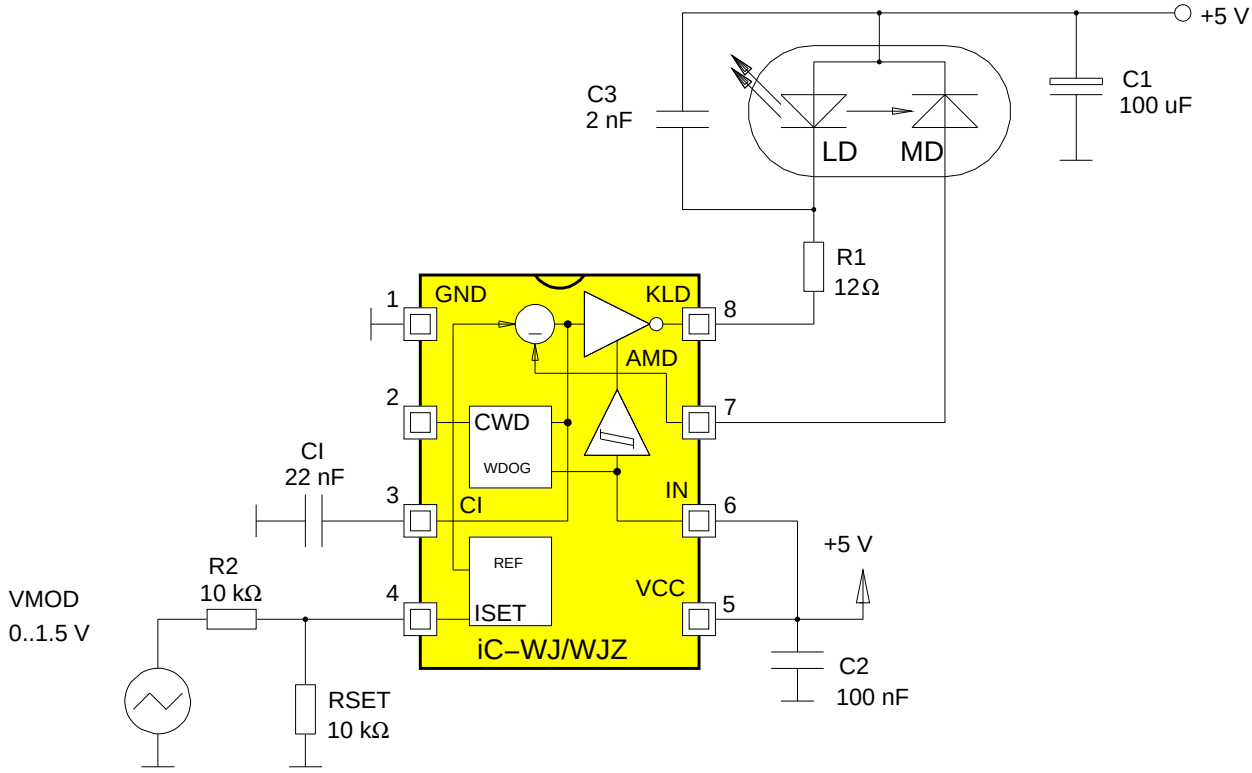


Figure 11: Analogue modulation during CW operation

Analogue modulation during CW operation
The modulation cut-off frequency is determined by the capacitor CI as well as by the operating point set with the resistor RSET. With CI = 100 nF and RSET = R2 = 10 kΩ the cut-off frequency is approx. 40 kHz, with CI = 22 nF and the same resitor value of about 230 kHz.

The laser power can also be modulated by adapting a current source, e.g. by using an operational amplifier with a current output (OTA). To limit the current at pin ISET while turning on the power supply for the OTA circuitry, however, RSET should be connected to the OTA output (instead of to GND). The maximum current possible at ISET must be taken into consideration when dimensioning the capacitor CI.

PC board layout
The ground connections of the external components CI, CWD and RSET have to be directly connected at the IC with the GND terminal.

DEMO BOARD

For the devices iC-WJ/WJZ/WJB a Demo Board is available for test purposes. The following figures show the schematic diagram and the component side of the test PCB.

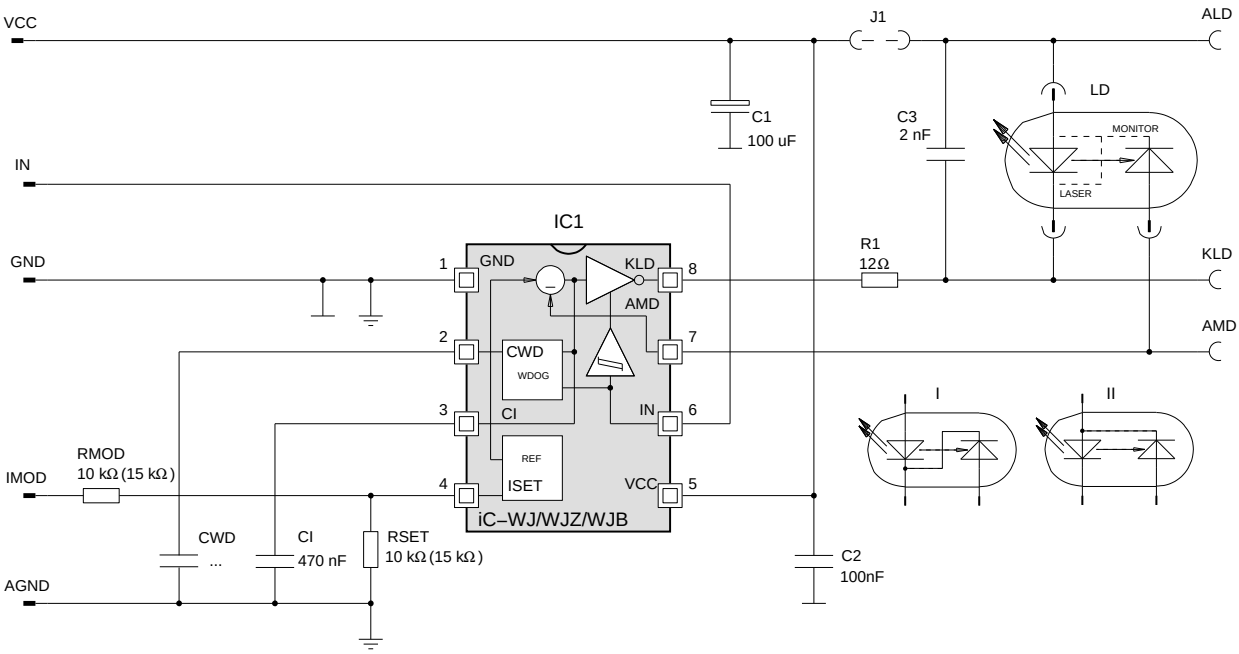


Figure 12: Schematic diagram of the Demo Board

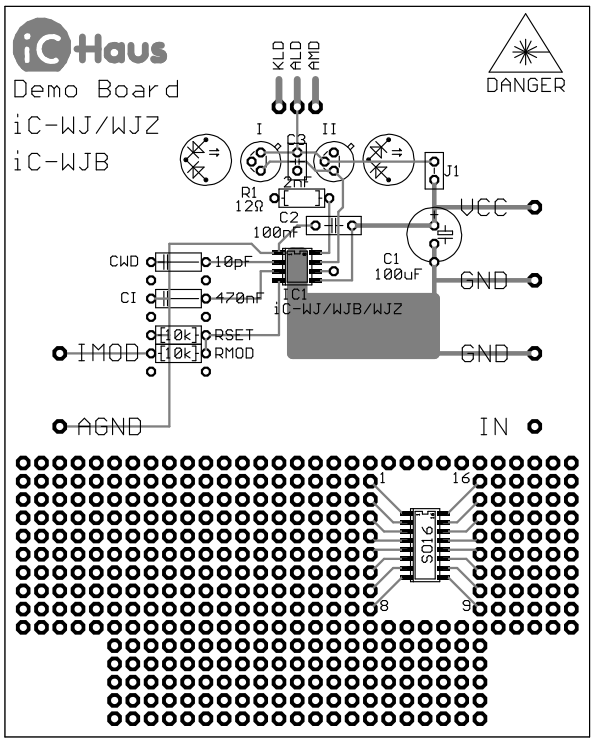


Figure 13: Demo Board (components side)

ORDERING INFORMATION

Type	Package	Order Designation
iC-WJ	SO8	iC-WJ SO8
	MSOP8	iC-WJ MSOP8
WJ Evaluation Board		iC-WJ EVAL WJ1D
iC-WJZ	SO8	iC-WJZ SO8
	MSOP8	iC-WJZ MSOP8
WJZ Evaluation Board		iC-WJZ EVAL WJ1D

For information about prices, terms of delivery, other packaging options etc. please contact:

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Am Kuemmerling 18
D-55294 Bodenheim
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Fax: +49 (61 35) 92 92-192
Web: http://www.ichaus.com
E-Mail: sales@ichaus.com

Wide Bandwidth OPERATIONAL TRANSCONDUCTANCE AMPLIFIER (OTA) and BUFFER

OTA FEATURES

- **Wide Bandwidth (80MHz, Open-Loop, G = +5)**
- **High Slew Rate (900V/µs)**
- **High Transconductance (95mA/V)**
- **External I_Q-Control**

BUFFER FEATURES

- **Closed-Loop Buffer**
- **Wide Bandwidth (1600MHz, V_O = 1V_{PP})**
- **High Slew Rate (4000V/µs)**
- **60mA Output Current**

OPA860 FEATURES

- **Low Quiescent Current (11.2mA)**
- **Versatile Circuit Function**

APPLICATIONS

- **Baseline Restore Circuits**
- **Video/Broadcast Equipment**
- **Communications Equipment**
- **High-Speed Data Acquisition**
- **Wideband LED Driver**
- **AGC-Multiplier**
- **ns-Pulse Integrator**
- **Control Loop Amplifier**
- **OPA660 Upgrade**

DESCRIPTION

The OPA860 is a versatile monolithic component designed for wide-bandwidth systems, including high performance video, RF and IF circuitry. It includes a wideband, bipolar operational transconductance amplifier (OTA), and voltage buffer amplifier.

The OTA or voltage-controlled current source can be viewed as an *ideal transistor*. Like a transistor, it has three terminals—a high impedance input (base), a low-impedance input/output (emitter), and the current output (collector). The OTA, however, is self-biased and bipolar. The output collector current is zero for a zero base-emitter voltage. AC inputs centered about zero produce an output current, which is bipolar and centered about zero. The transconductance of the OTA can be adjusted with an external resistor, allowing bandwidth, quiescent current, and gain trade-offs to be optimized.

Also included in the OPA860 is an uncommited closed-loop, unity-gain buffer. This provides 1600MHz bandwidth and 4000V/µs slew rate.

Used as a basic building block, the OPA860 simplifies the design of AGC amplifiers, LED driver circuits for fiber optic transmission, integrators for fast pulses, fast control loop amplifiers and control amplifiers for capacitive sensors and active filters. The OPA860 is available in an SO-8 surface-mount package.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA860	SO-8	D	–45°C to +85°C	OPA860	OPA860ID	Rails, 75
					OPA860IDR	Tape and Reel, 2500

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

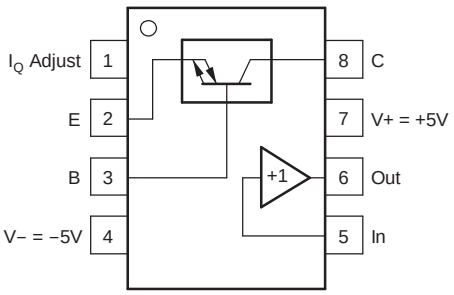
ABSOLUTE MAXIMUM RATINGS(1)

Power Supply	±6.5V_{DC}
Internal Power Dissipation	See Thermal Information
Differential Input Voltage	±1.2V
Input Common-Mode Voltage Range	±V_S
Storage Temperature Range: D	–65°C to +125°C
Lead Temperature (soldering, 10s)	+300°C
Junction Temperature (T_J)	+150°C
ESD Rating:	
Human Body Model (HBM)(2)	1500V
Charge Device Model (CDM)	1000V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress Ratings only, and functional operations of the device at these and any other conditions beyond those specified is not supported.
(2) Pin 2 > 500V HBM.

PIN CONFIGURATION

Top View **SO**



ELECTRICAL CHARACTERISTICS: V_S = ±5V

R_L = 500Ω and R_{ADJ} = 250Ω, unless otherwise noted.

PARAMETER	CONDITIONS	OPA860ID				UNITS	MIN/ MAX	TEST LEVEL(1)
		TYP	MIN/MAX OVER TEMPERATURE					
		+25°C	+25°C(2)	0°C to 70°C(3)	–40°C to +85°C(3)			
Closed Loop OTA + BUFFER (see Figure 53)								
AC PERFORMANCE	G = +2, See Figure 53							
Bandwidth	V_O = 200mV$_{PP}$	470	380	375	370	MHz	min	B
	V_O = 1V$_{PP}$	470				MHz	typ	C
	V_O = 5V$_{PP}$	350				MHz	typ	C
Bandwidth for 0.1dB Gain Flatness	V_O = 200mV$_{PP}$	42				MHz	typ	C
Slew Rate	V_O = 5V Step	3500	3000	2800	2700	V/µs	typ	C
Rise Time and Fall Time	V_O = 1V Step	0.7				ns	typ	C
Harmonic Distortion	G = +2, V_O = 2V$_{PP}$, 5MHz							
2nd-Harmonic	R_L = 100Ω	–54				dBc	typ	C
	R_L = 500Ω	–77				dBc	typ	C
3rd-Harmonic	R_L = 100Ω	–66				dBc	typ	C
	R_L = 500Ω	–79				dBc	typ	C
OTA - Open-Loop (see Figure 48)								
AC PERFORMANCE								
Bandwidth	G = +5, V_O = 200mV$_{PP}$, R_L = 500Ω	80	77	75	74	MHz	min	B
	G = +5, V_O = 1V$_{PP}$	80				MHz	typ	C
	G = +5, V_O = 5V$_{PP}$	80				MHz	typ	C
Slew Rate	G = +5, V_O = 5V Step	900	860	850	840	V/µs	min	B
Rise Time and Fall Time	V_O = 1V Step	4.4				ns	typ	C
Harmonic Distortion	G = +5, V_O = 2V$_{PP}$, 5MHz							
2nd-Harmonic	R_L = 500Ω	–68	–55	–54	–53	dB	max	B
3rd-Harmonic	R_L = 500Ω	–57	–52	–51	–49	dB	max	B
Base Input Voltage Noise	f > 100kHz	2.4	3.0	3.3	3.4	nV/√Hz	max	B
Base Input Current Noise	f > 100kHz	1.65	2.4	2.45	2.5	pA/√Hz	max	B
Emitter Input Current Noise	f > 100kHz	5.2	15.3	16.6	17.5	pA/√Hz	max	B
OTA DC PERFORMANCE(4) (see Figure 48)								
Min OTA Transconductance	V_O = ±10mV, R_C = 0Ω, R_E = 0Ω	95	**80**	77	75	mA/V	min	A
Max OTA Transconductance	V_O = ±10mV, R_C = 0Ω, R_E = 0Ω	95	**150**	155	160	mA/V	min	A
B-Input Offset Voltage	V_B = 0V, R_C = 0Ω, R_E = 100Ω	±3	**±12**	±15	±20	mV	max	A
Average B-Input Offset Voltage Drift	V_B = 0V, R_C = 0Ω, R_E = 100Ω	±3		±67	±120	µV/°C	max	B
B-Input Bias Current	V_B = 0V, R_C = 0Ω, R_E = 100Ω	±1	**±5**	±6	±6.6	µA	max	A
Average B-Input Bias Current Drift	V_B = 0V, R_C = 0Ω, R_E = 100Ω			±20	±25	nA/°C	max	B
E-Input Bias Current	V_B = 0V, V_C = 0V	±30	**±100**	±125	±140	µA	max	A
Average E-Input Bias Current Drift	V_B = 0V, V_C = 0V			±500	±600	nA/°C	max	B
C-Output Bias Current	V_B = 0V, V_C = 0V	±5	**±18**	±30	±38	µA	max	A
Average C-Output Bias Current Drift	V_B = 0V, V_C = 0V			±250	±300	nA/°C	max	B
OTA INPUT (see Figure 48)								
B-Input Voltage Range		±4.2	±3.7	±3.6	±3.6	V	min	B
B-Input Impedance		455 || 2.1				kΩ || pF	typ	C
Min E-Input Input Resistance		10.5	12.5	13.0	13.3	Ω	min	B
Max E-Input Input Resistance		10.5	6.7	6.5	6.3	Ω	max	B

(1) Test levels: (A) 100% tested at +25°C. Over temperature limits set by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(2) Junction temperature = ambient for +25°C specifications.
(3) Junction temperature = ambient at low temperature limit; junction temperature = ambient + 8°C at high temperature limit for over temperature specifications.
(4) Current is considered positive out of node. V_{CM} is the input common-mode voltage.

ELECTRICAL CHARACTERISTICS: V_S = ±5V (continued)

R_L = 500Ω and R_{ADJ} = 250Ω, unless otherwise noted.

PARAMETER	CONDITIONS	OPA860ID TYP +25°C	OPA860ID MIN/MAX OVER TEMPERATURE +25°C[2]	0°C to 70°C[3]	–40°C to +85°C[3]	UNITS	MIN/ MAX	TEST LEVEL[1]
OTA OUTPUT								
E-Output Voltage Compliance	I_E = ±1mA	±4.2	**±3.7**	±3.6	±3.6	V	min	A
E-Output Current, Sinking/Sourcing	V_E = 0	±15	**±10**	±9	±9	mA	min	A
C-Output Voltage Compliance	I_C = ±1mA	±4.7	**±4.0**	±3.9	±3.9	V	min	A
C-Output Current, Sinking/Sourcing	V_C = 0	±15	**±10**	±9	±9	mA	min	A
C-Output Impedance		54 || 2				kΩ || pF	typ	C
BUFFER (see Figure 45)								
AC PERFORMANCE								
Bandwidth	V_O = 200mV$_{PP}$	1200	750	720	700	MHz	min	B
	V_O = 1V$_{PP}$	1600				MHz	typ	C
	V_O = 5V$_{PP}$	1000				MHz	typ	C
Slew Rate	V_O = 5V Step	4000	3500	3200	3000	V/µs	min	B
Rise Time and Fall Time	V_O = 1V Step	0.4				ns	typ	C
Settling Time to 0.05%	V_O = 1V Step	6				ns	typ	C
Harmonic Distortion	V_O = 2V$_{PP}$, 5MHz							
2nd-Harmonic	R_L = 100Ω	–52	–47	–46	–44	dBc	max	B
	R_L ≥ 500Ω	–72	–65	–63	–61	dBc	max	B
3rd-Harmonic	R_L = 100Ω	–67	–63	–63	–62	dBc	max	B
	R_L ≥ 500Ω	–96	–86	–85	–83	dBc	max	B
Input Voltage Noise	f > 100kHz	4.8	5.1	5.6	6.0	nV/√Hz	max	B
Input Current Noise	f > 100kHz	2.1	2.6	2.7	2.8	pA/√Hz	max	B
Differential Gain	NTSC, PAL	0.06				%	typ	C
Differential Phase	NTSC, PAL	0.02				Degrees	typ	C
BUFFER DC PERFORMANCE								
Gain	R_L = 500Ω	1	**0.98**	0.98	0.98	V/V	min	A
	R_L = 500Ω	1	**1**	1	1	V/V	max	A
Input Offset Voltage		±16	**±30**	±36	±38	mV	max	A
Average Input Offset Voltage Drift				±125	±125	µV/°C	max	B
Input Bias Current		±3	**±7**	±8	±8.5	µA	max	A
Average Input Bias Current Drift				±20	±20	nA/°C	max	B
BUFFER INPUT								
Input Impedance		1.0 || 2.1				MΩ || pF	typ	C
BUFFER OUTPUT								
Output Voltage Swing	R_L = 500Ω	±4.0	**±3.8**	±3.8	±3.8	V	min	A
Output Current	V_O = 0	±60	**±50**	±49	±48	mA	min	A
Closed-Loop Output Impedance	f ≤ 100kHz	1.4				Ω	typ	C
POWER SUPPLY (OTA + BUFFER)								
Specified Operating Voltage		±5				V	typ	C
Maximum Operating Voltage			**±6.5**	±6.5	±6.5	V	max	A
Minimum Operating Voltage			**±2.5**	±2.5	±2.5	V	min	B
Maximum Quiescent Current	R_{ADJ} = 250Ω	11.2	**12**	13.5	14.5	mA	max	A
Minimum Quiescent Current	R_{ADJ} = 250Ω	11.2	**10.5**	9.5	7.9	mA	min	A
OTA Power-Supply Rejection Ratio (+PSRR)	$\Delta I_C/\Delta V_S$	±20	**±50**	±60	±65	µA/V	max	A
Buffer Power-Supply Rejection Ratio (–PSRR)	$\Delta V_O/\Delta V_S$	54	**48**	46	45	dB	min	A
THERMAL CHARACTERISTICS								
Specification: ID		–40 to +85				°C	typ	C
Thermal Resistance θ_{JA}								
D SO-8	Junction-to-Ambient	125				°C/W	typ	C

TYPICAL CHARACTERISTICS: V_S = ±5V

At T_A = +25°C, I_Q = 11.2mA, and R_L = 500Ω, unless otherwise noted. (See Figure 53.)

OTA + BUF Performance

SMALL-SIGNAL FREQUENCY RESPONSE

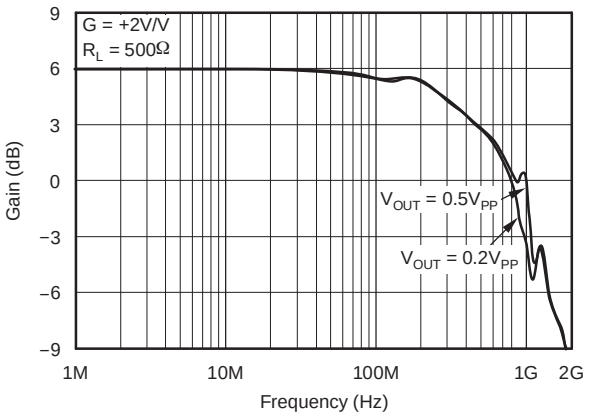


Figure 1.

LARGE-SIGNAL FREQUENCY RESPONSE

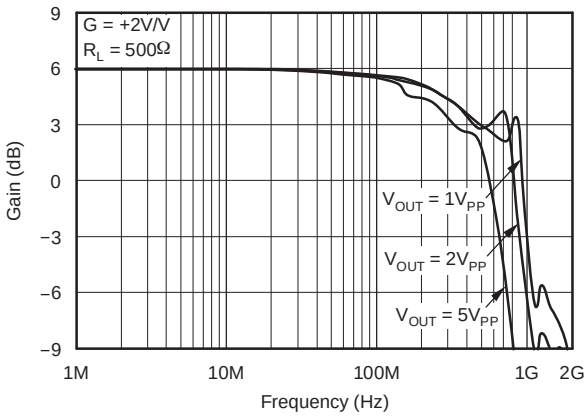


Figure 2.

SMALL-SIGNAL FREQUENCY RESPONSE vs QUIESCENT CURRENT

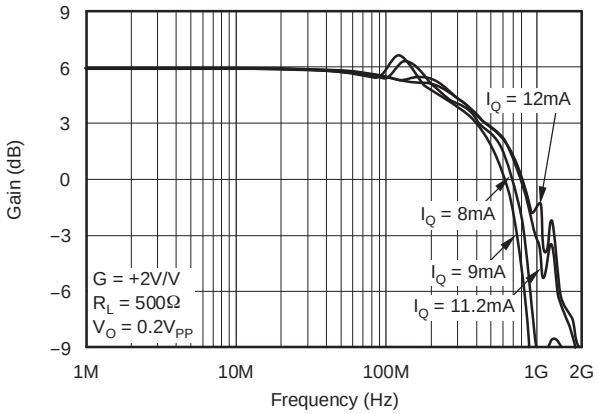


Figure 3.

GAIN FLATNESS vs QUIESCENT CURRENT

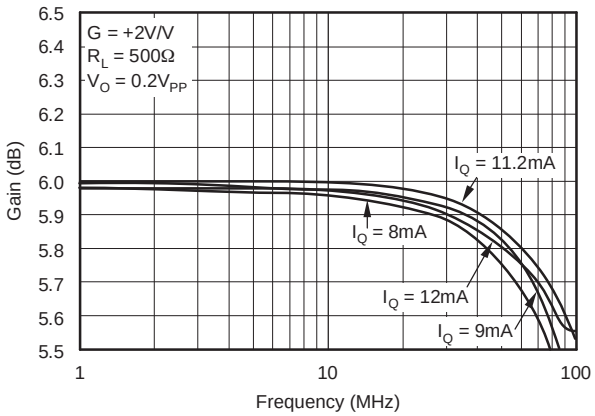


Figure 4.

SMALL-SIGNAL PULSE RESPONSE

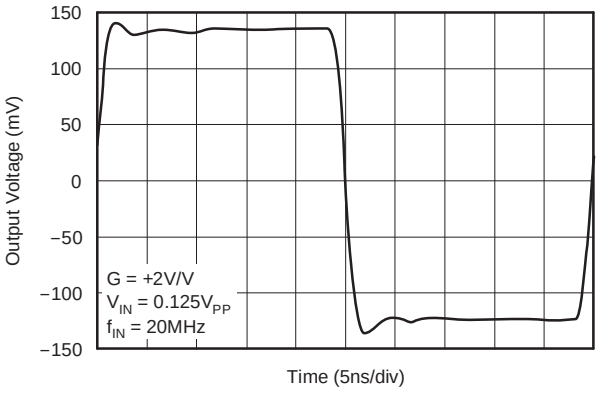


Figure 5.

LARGE-SIGNAL PULSE RESPONSE

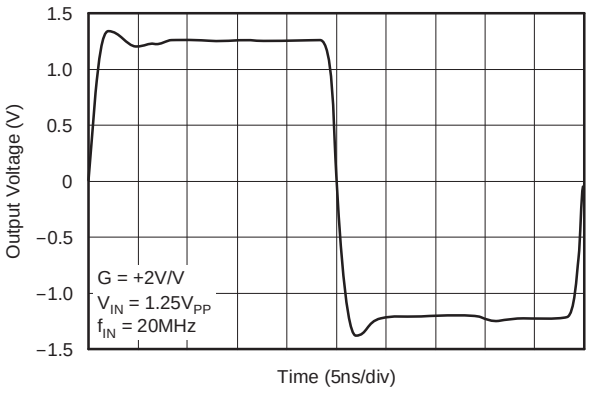


Figure 6.

TYPICAL CHARACTERISTICS: V_S = ±5V (continued)

At T_A = +25°C, I_Q = 11.2mA, and R_L = 500Ω, unless otherwise noted. (See Figure 53.)

HARMONIC DISTORTION vs FREQUENCY

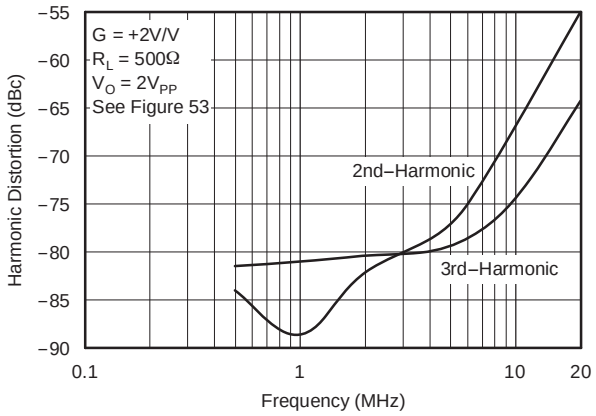


Figure 7.

HARMONIC DISTORTION vs OUTPUT RESISTANCE

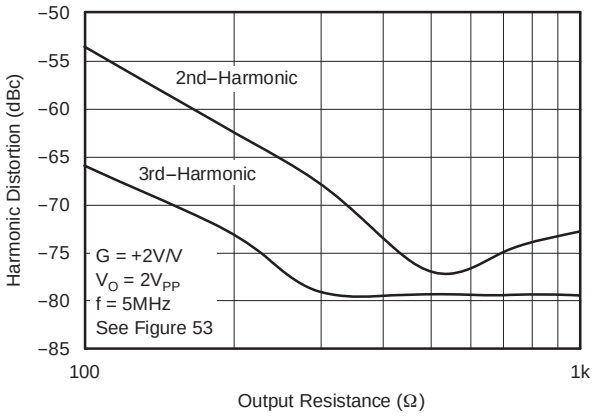


Figure 8.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

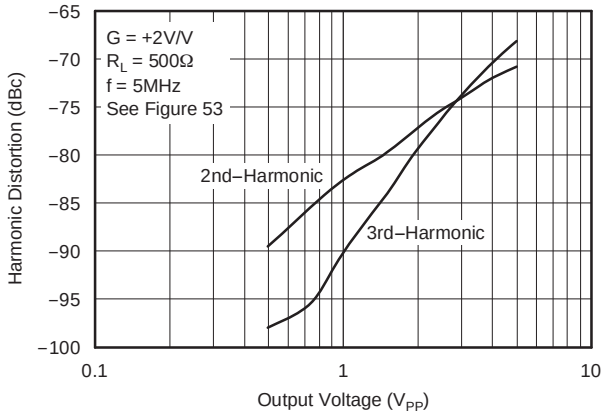


Figure 9.

HARMONIC DISTORTION vs SUPPLY VOLTAGE

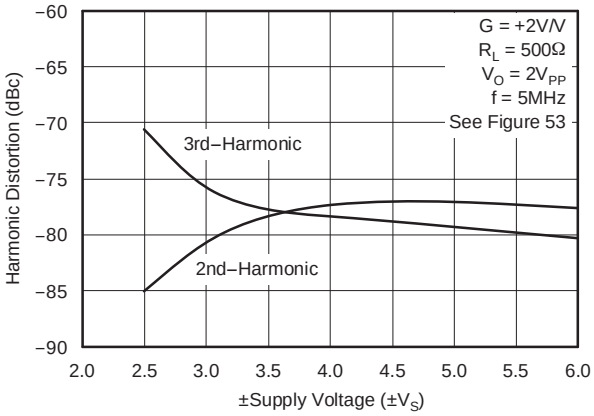


Figure 10.

HARMONIC DISTORTION vs QUIESCENT CURRENT

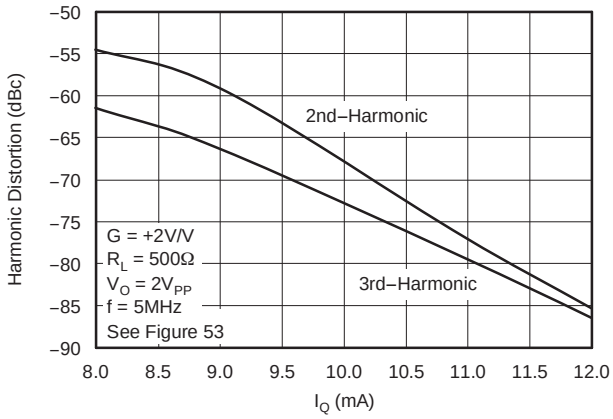


Figure 11.

QUIESCENT CURRENT vs R_{ADJ}

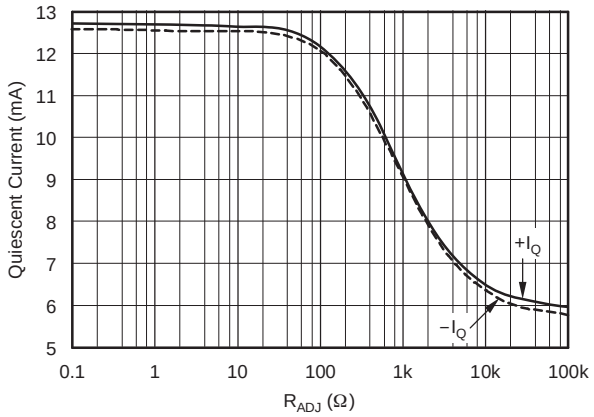


Figure 12.

TYPICAL CHARACTERISTICS: V_S = ±5V

At T_A = +25°C, I_Q = 11.2mA, and R_L = 500Ω, unless otherwise noted.

OTA Performance

OTA TRANSCONDUCTANCE vs FREQUENCY

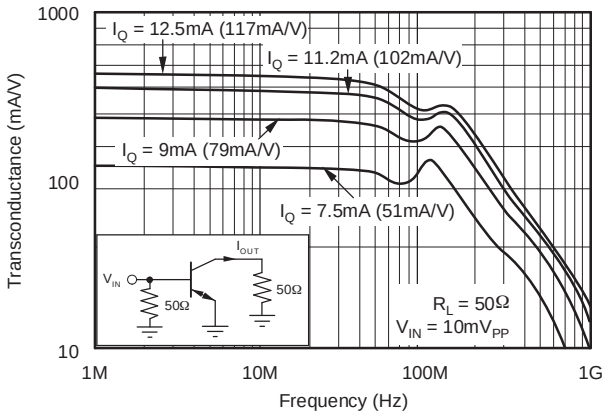


Figure 13.

OTA TRANSCONDUCTANCE vs QUIESCENT CURRENT

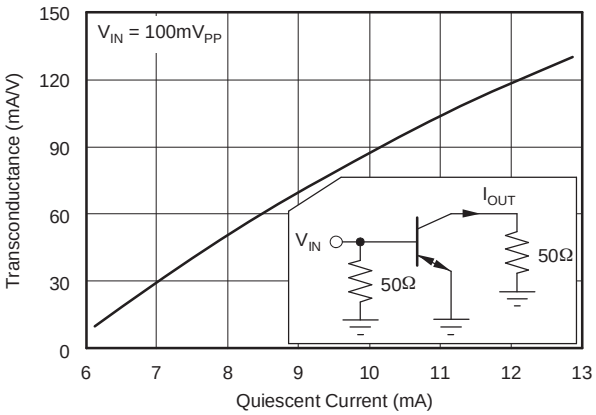


Figure 14.

OTA TRANSCONDUCTANCE vs INPUT VOLTAGE

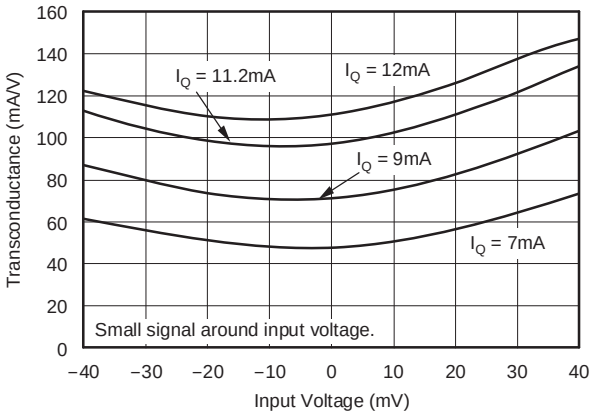


Figure 15.

OTA TRANSFER CHARACTERISTICS

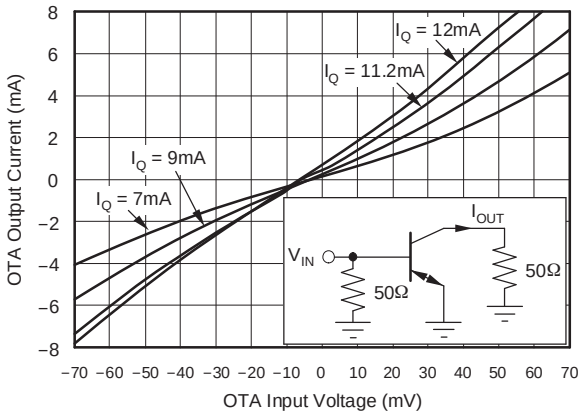


Figure 16.

OTA SMALL-SIGNAL PULSE RESPONSE

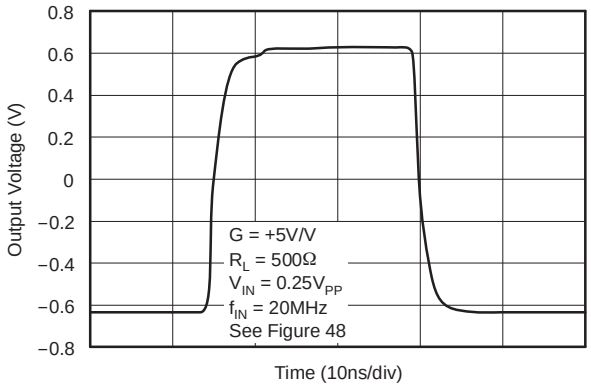


Figure 17.

OTA LARGE-SIGNAL PULSE RESPONSE

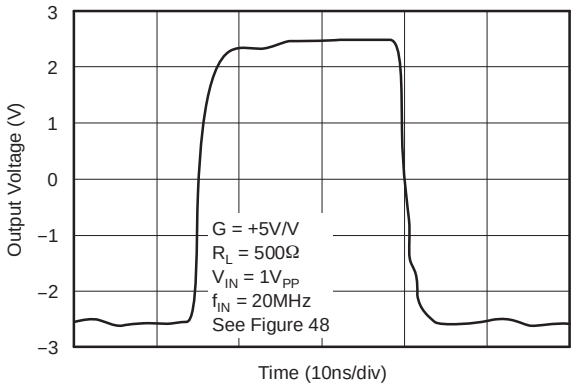


Figure 18.

TYPICAL CHARACTERISTICS: V_S = ±5V (continued)

At T_A = +25°C, I_Q = 11.2mA, and R_L = 500Ω, unless otherwise noted.

B-INPUT RESISTANCE vs QUIESCENT CURRENT

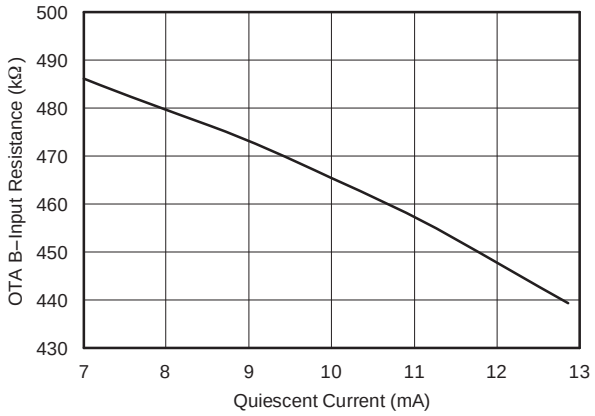


Figure 19.

C-OUTPUT RESISTANCE vs QUIESCENT CURRENT

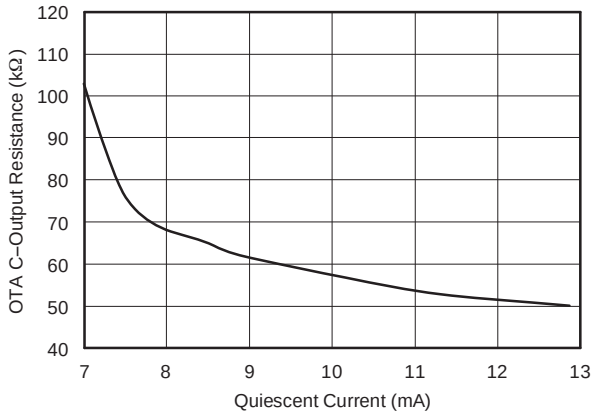


Figure 20.

E-OUTPUT RESISTANCE vs QUIESCENT CURRENT

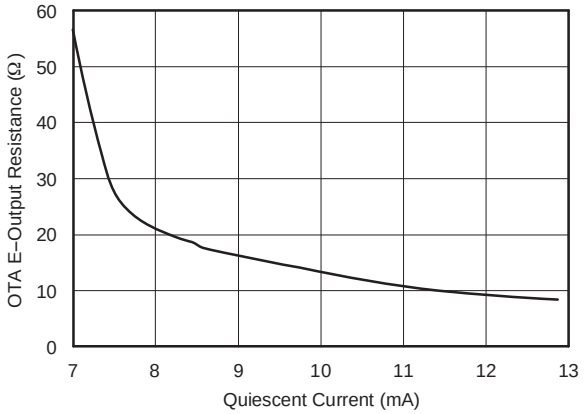


Figure 21.

INPUT VOLTAGE AND CURRENT NOISE DENSITY

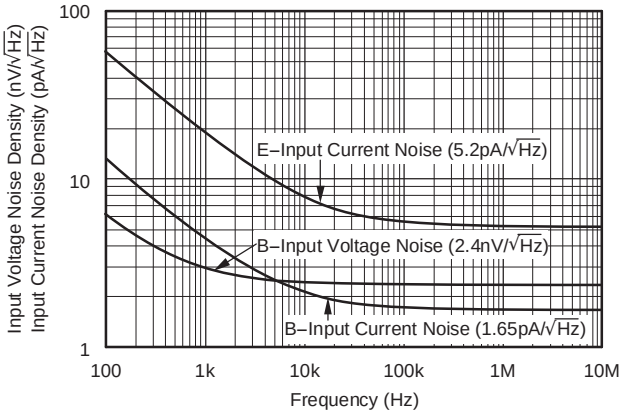


Figure 22.

1MHz OTA VOLTAGE AND CURRENT NOISE DENSITY vs QUIESCENT CURRENT ADJUST RESISTOR

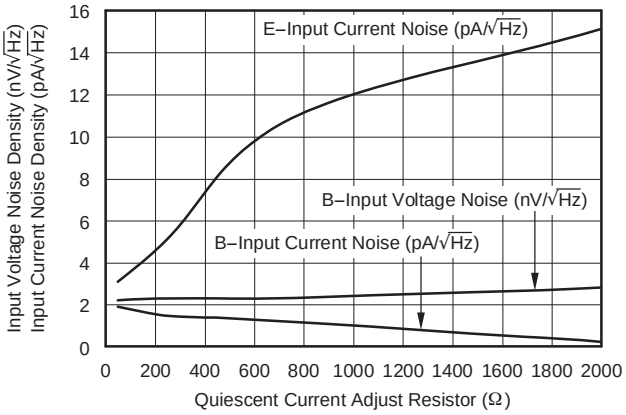


Figure 23.

TYPICAL CHARACTERISTICS: V_S = ±5V

At T_A = +25°C, I_Q = 11.2mA, and R_L = 500Ω, unless otherwise noted.

BUF Performance

BUFFER BANDWIDTH vs OUTPUT VOLTAGE

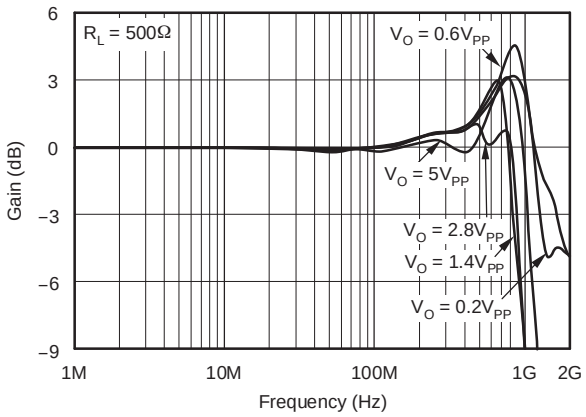


Figure 24.

BUFFER BANDWIDTH vs LOAD RESISTANCE

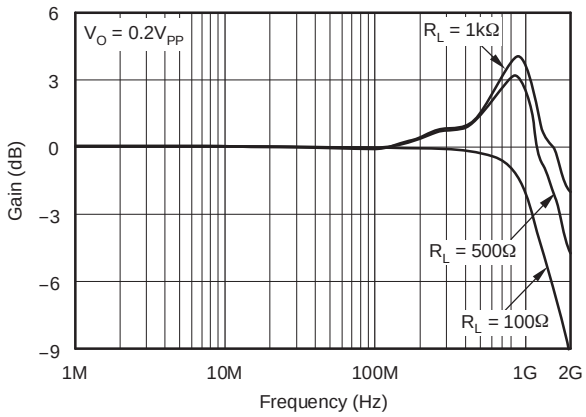


Figure 25.

BUFFER GAIN FLATNESS

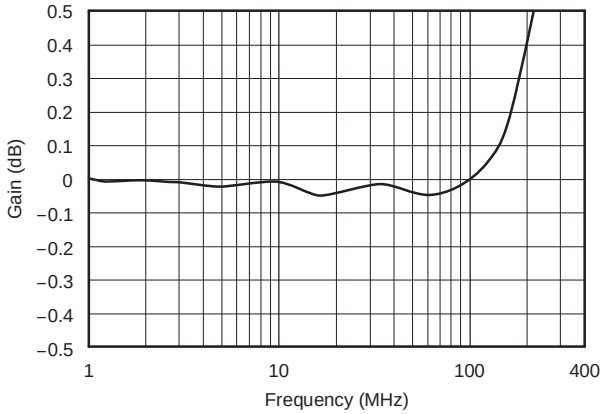


Figure 26.

BUFFER SMALL-SIGNAL PULSE RESPONSE

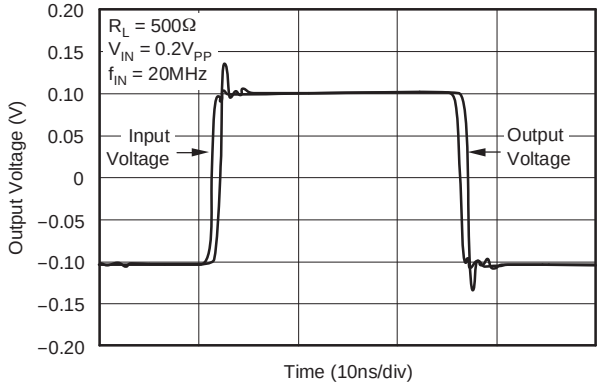


Figure 27.

BUFFER LARGE-SIGNAL PULSE RESPONSE

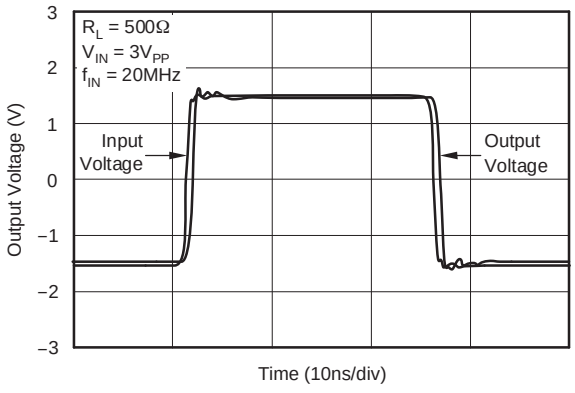


Figure 28.

HARMONIC DISTORTION vs FREQUENCY

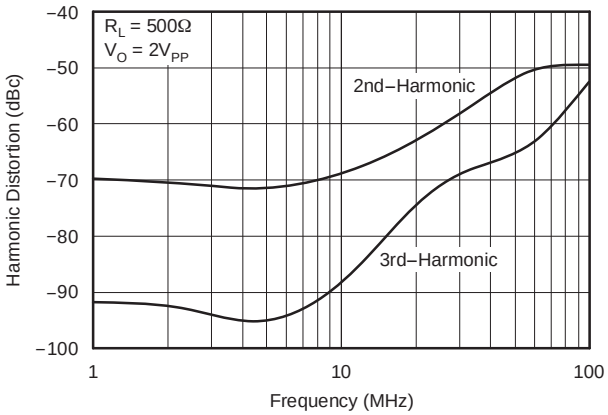


Figure 29.

TYPICAL CHARACTERISTICS: V_S = ±5V (continued)

At T_A = +25°C, I_Q = 11.2mA, and R_L = 500Ω, unless otherwise noted.

5MHz HARMONIC DISTORTION vs LOAD RESISTANCE

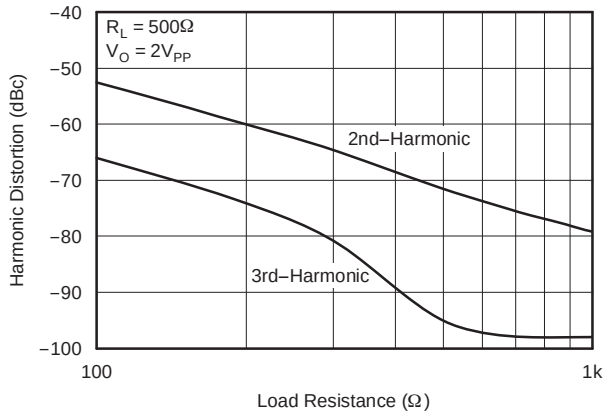


Figure 30.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

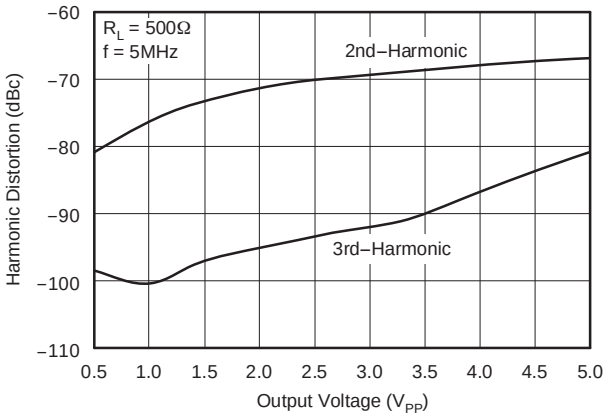


Figure 31.

5MHz HARMONIC DISTORTION vs SUPPLY VOLTAGE

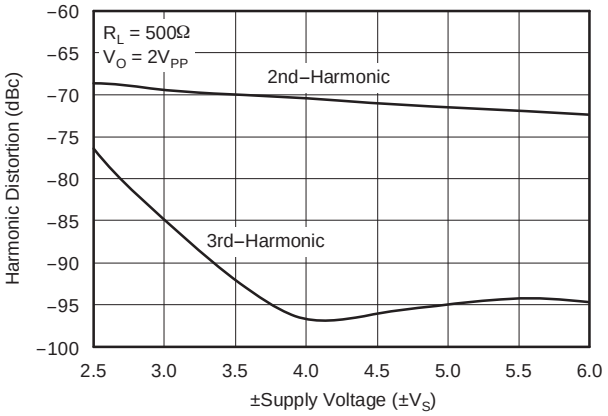


Figure 32.

BUFFER TRANSFER FUNCTION

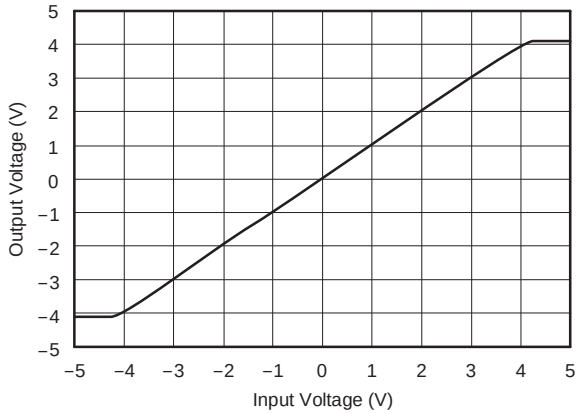


Figure 33.

INPUT VOLTAGE AND CURRENT NOISE DENSITY

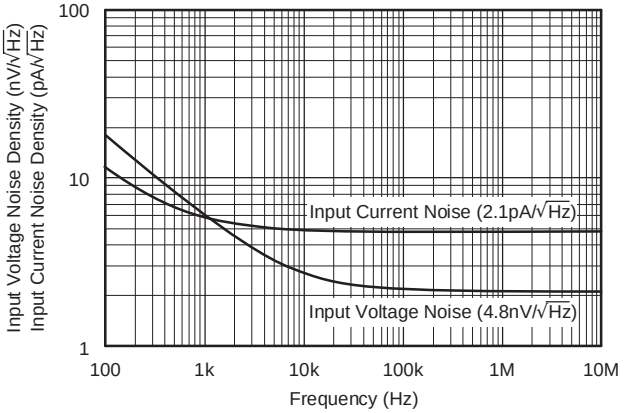


Figure 34.

BUFFER OUTPUT IMPEDANCE

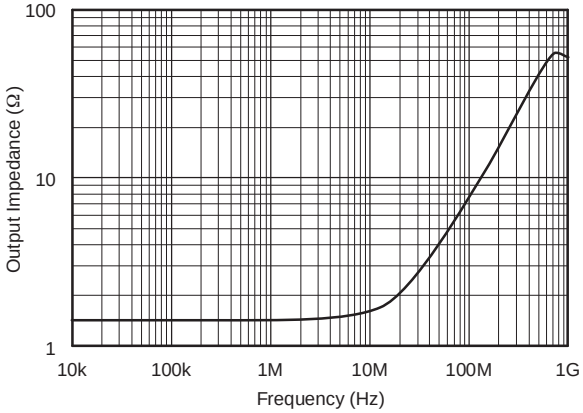


Figure 35.

TYPICAL CHARACTERISTICS: V_S = ±5V (continued)

At T_A = +25°C, I_Q = 11.2mA, and R_L = 500Ω, unless otherwise noted.

BUFFER GROUP DELAY TIME vs FREQUENCY

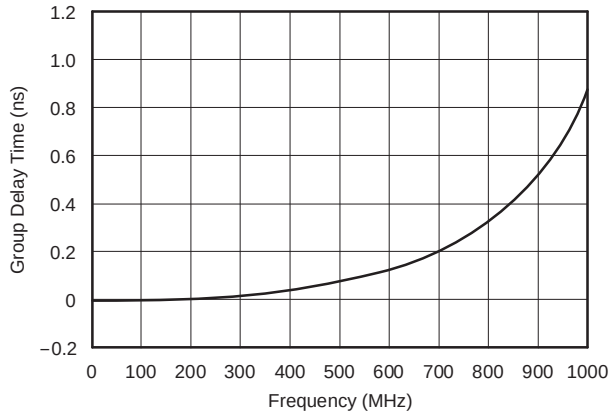


Figure 36.

BUFFER OUTPUT VOLTAGE AND CURRENT LIMITATIONS

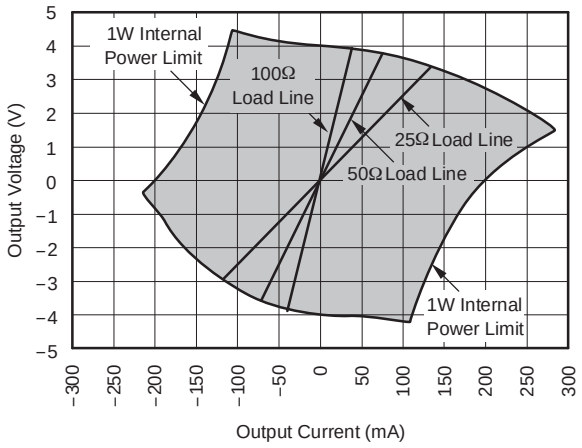


Figure 37.

QUIESCENT CURRENT vs TEMPERATURE

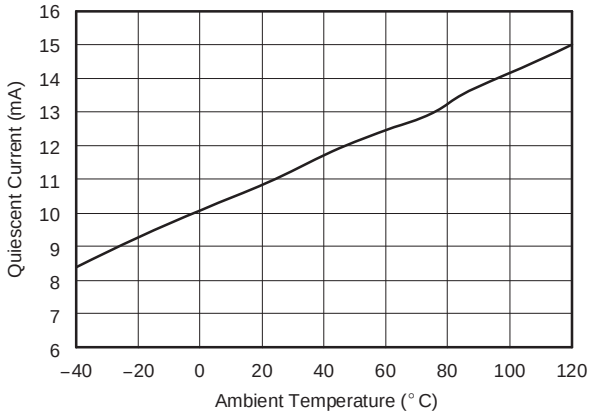


Figure 38.

POWER-SUPPLY REJECTION RATIO vs FREQUENCY

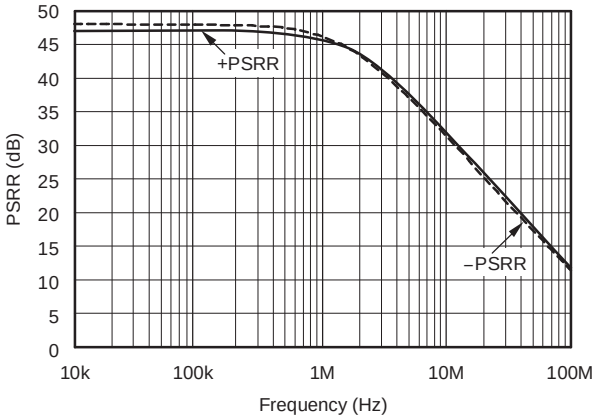


Figure 39.

VOLTAGE RANGE vs TEMPERATURE

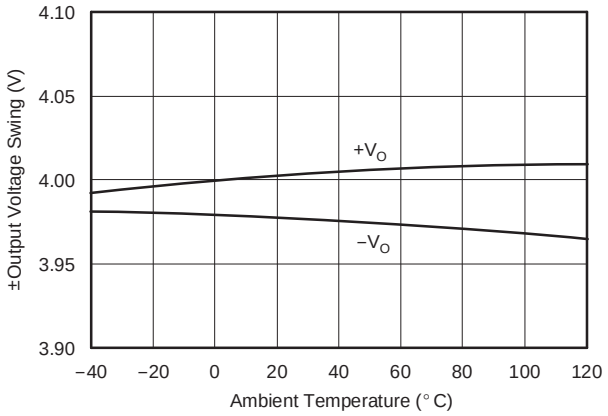


Figure 40.

OUTPUT CURRENT vs TEMPERATURE

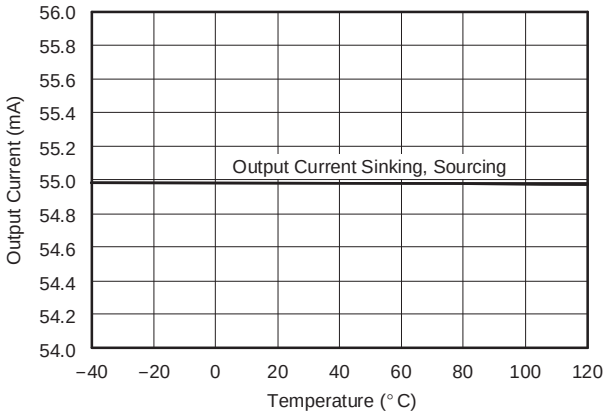


Figure 41.

TYPICAL CHARACTERISTICS: V_S = ±5V (continued)

At T_A = +25°C, I_Q = 11.2mA, and R_L = 500Ω, unless otherwise noted.

DC DRIFT vs TEMPERATURE

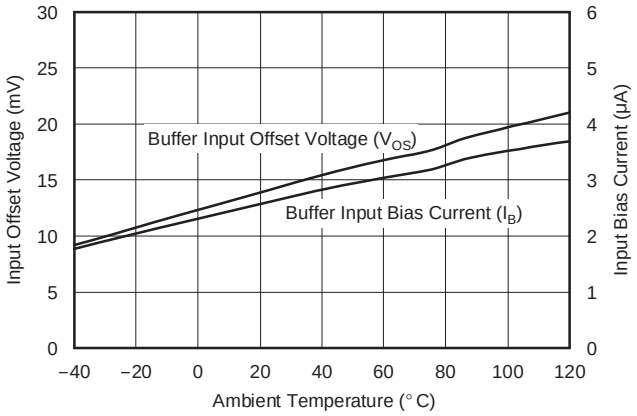


Figure 42.

C-OUTPUT BIAS CURRENT vs TEMPERATURE

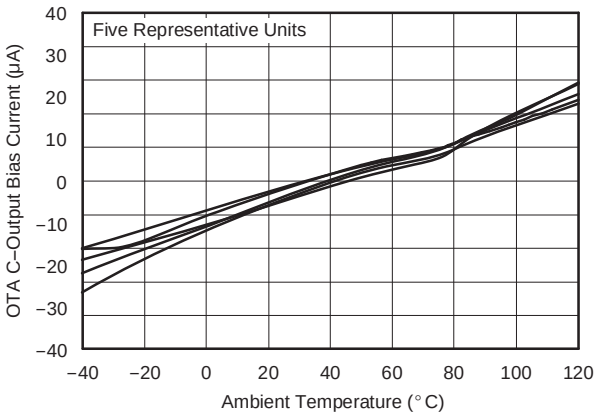


Figure 43.

APPLICATION INFORMATION

The OPA860 combines a high-performance buffer with a transconductance section. This transconductance section is discussed in the *OTA (Operational Transconductance Amplifier)* section of this data sheet. Over the years and depending on the writer, the OTA section of an op amp has been referred to as a Diamond Transistor, Voltage-Controlled Current source, Transconductor, Macro Transistor, or positive second-generation current conveyor (CCII+). Corresponding symbols for these terms are shown in Figure 44.

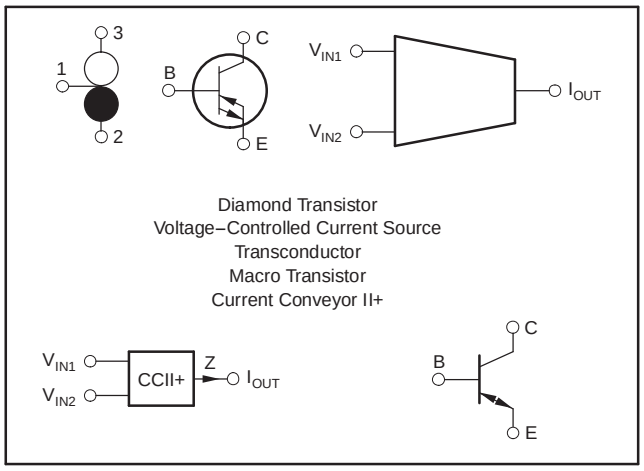


Figure 44. Symbols and Terms

Regardless of its depiction, the OTA section has a high-input impedance (B input), a low-input/output impedance (E input), and a high impedance current source output (C output).

BUFFER SECTION—AN OVERVIEW

The buffer section of the OPA860 is an 1600MHz, 4000V/µs closed-loop buffer that can be used as a building block for AGC amplifiers, LED driver circuit, integrator for fast pulse, fast control loop amplifiers, and control amplifiers for capacitive sensors and active filters. The Buffer section does not share the bias circuit of the OTA section; thus, it is not affected by changes in the I_Q adjust resistor (R_{ADJ}).

TRANSCONDUCTANCE (OTA) SECTION—AN OVERVIEW

The symbol for the OTA section is similar to a transistor (see Figure 44). Applications circuits for the OTA look and operate much like transistor circuits—the transistor is also a voltage-controlled current source. Not only does this characteristic simplify the understanding of application circuits, it aids the circuit optimization process as well. Many of the same intuitive techniques used with transistor designs apply to OTA circuits. The three terminals of the OTA are labeled B, E, and C. This labeling calls attention to its similarity to a transistor, yet draws distinction for clarity. While the OTA is similar to a transistor, one essential difference is the sense of the C-output current: it flows out the C terminal for positive B-to-E input voltage and in the C terminal for negative B-to-E input voltage. The OTA offers many advantages over a discrete transistor. The OTA is self-biased, simplifying the design process and reducing component count. In addition, the OTA is far more linear than a transistor. Transconductance of the OTA is constant over a wide range of collector currents—this feature implies a fundamental improvement of linearity.

BASIC CONNECTIONS

Figure 46 shows basic connections required for operation. These connections are not shown in subsequent circuit diagrams. Power-supply bypass capacitors should be located as close as possible to the device pins. Solid tantalum capacitors are generally best.

QUIESCENT CURRENT CONTROL PIN

The quiescent current of the transconductance portion of the OPA860 is set with a resistor, R_{ADJ}, connected from pin 1 to $-V_S$. It affects only the operating currents of OTA sections. The bias circuitry of the Buffer section is independent of the bias circuitry for the OTA section; therefore, the quiescent current cannot go below 5.8mA. The maximum quiescent current is 12.7mA. R_{ADJ} should be set between 50Ω and 1kΩ for optimal performance of the OTA section. This range corresponds to the 12.5mA quiescent current for R_{ADJ} = 50Ω, and 9mA for R_{ADJ} = 1kΩ. If the I_Q adjust pin is connected to the negative supply, the quiescent current will be set by the 250Ω internal resistor.

Reducing or increasing the quiescent current for the OTA section controls the bandwidth and AC behavior as well as the transconductance. With R_{ADJ} = 250Ω, this sets approximately 11.2mA total quiescent current at 25°C. It may be appropriate in some applications to trim this resistor to achieve the desired quiescent current or AC performance.

Applications circuits generally do not show the resistor R_Q, but it is required for proper operation.

With a fixed R_{ADJ} resistor, quiescent current increases with temperature (see Figure 43 in the *Typical Characteristics* section). This variation of current with temperature holds the transconductance, g_m, of the OTA relatively constant with temperature (another advantage over a transistor).

It is also possible to vary the quiescent current with a control signal. The control loop in Figure 45 shows 1/2 of a REF200 current source used to develop 100mV on R_1. The loop forces 125mV to appear on R_2. Total quiescent current of the OPA860 is approximately 37 × I_1, where I_1 is the current made to flow out of pin 1.

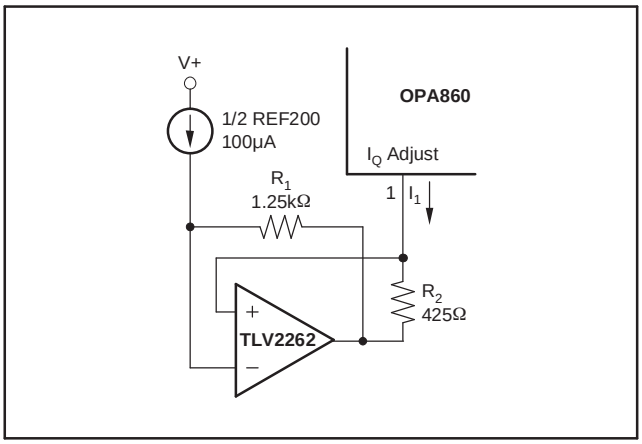


Figure 45. Optional Control Loop for Setting Quiescent Current

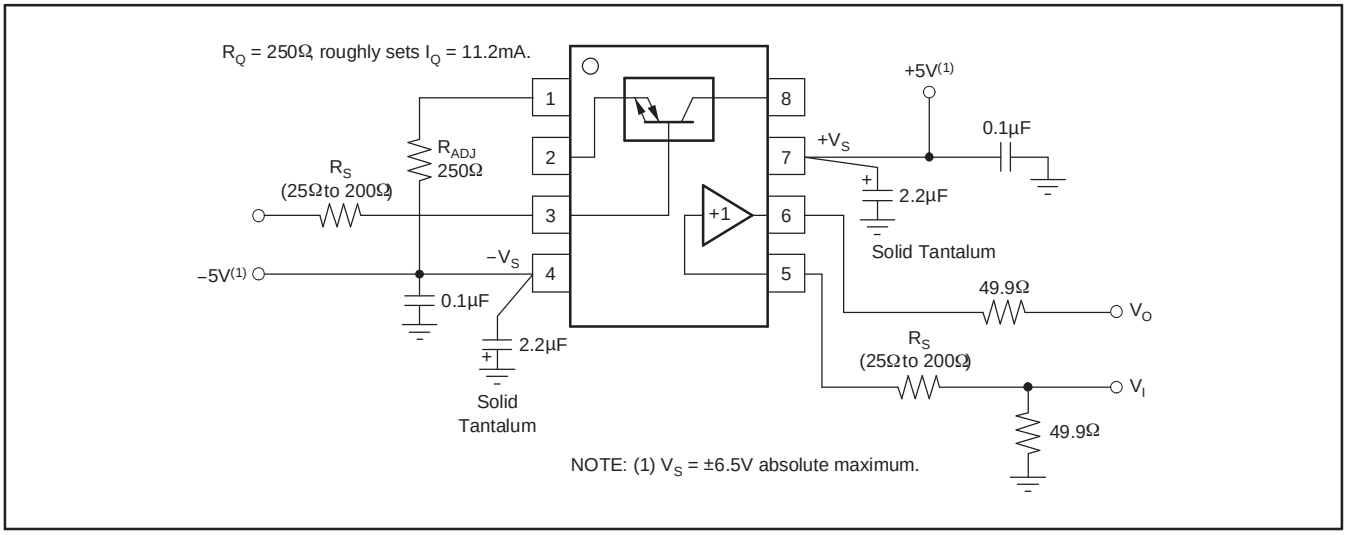


Figure 46. Basic Connections

With this control loop, quiescent current will be nearly constant with temperature. Since this differs from the temperature-dependent behavior of the internal current source, other temperature-dependent behavior may differ from that shown in the Typical Characteristics. The circuit of Figure 45 will control the I_Q of the OTA section of the OPA860 somewhat more accurately than with a fixed external resistor, R_Q. Otherwise, there is no fundamental advantage to using this more complex biasing circuitry. It does, however, demonstrate the possibility of signal-controlled quiescent current. This capability may suggest other possibilities such as AGC, dynamic control of AC behavior, or VCO.

BASIC APPLICATIONS CIRCUITS

Most applications circuits for the OTA section consist of a few basic types, which are best understood by analogy to a transistor. Used in voltage-mode, the OTA section can operate in three basic operating states—common emitter, common base, and common collector. In the current-mode, the OTA can be useful for analog computation such as current amplifier, current differentiator, current integrator, and current summer.

Common-E Amplifier or Forward Amplifier

Figure 47 compares the common-emitter configuration for a BJT with the common-E amplifier for the OTA section. There are several advantages in using the OTA section in place of a BJT in this configuration. Notably, the OTA does not require any biasing, and the transconductance gain remains constant over temperature. The output offset voltage is close to 0, compared with several volts for the common-emitter amplifier.

The gain is set in a similar manner as for the BJT equivalent with Equation 1:

$$G = \frac{R_L}{\frac{1}{g_m} + R_E} \quad (1)$$

Just as transistor circuits often use emitter degeneration, OTA circuits may also use degeneration. This option can be used to reduce the effects that offset voltage and offset current might otherwise have on the DC operating point of the OTA. The E-degeneration resistor may be bypassed with a large capacitor to maintain high AC gain. Other circumstances may suggest a smaller value capacitor used to extend or optimize high-frequency performance.

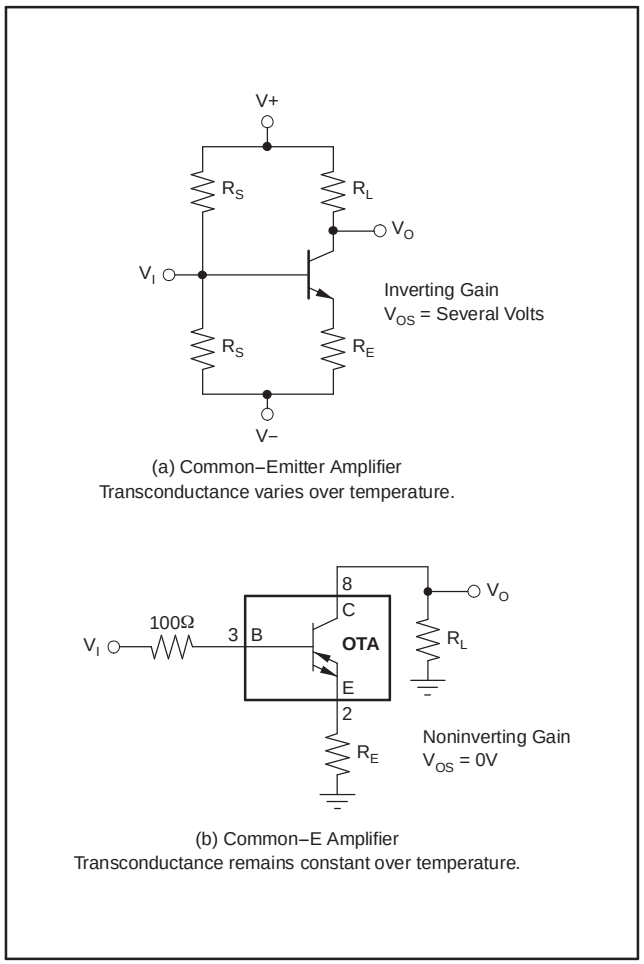


Figure 47. Common-Emitter vs Common-E Amplifier

The transconductance of the OTA with degeneration can be calculated by Equation 2:

$$g_{m\_deg} = \frac{1}{\frac{1}{g_m} + R_E} \quad (2)$$

A positive voltage at the B-input, pin 3, causes a positive current to flow out of the C-input, pin 8. Figure 47b shows an amplifier connection of the OTA, the equivalent of a common-emitter transistor amplifier. Input and output can be ground-referenced without any biasing. The amplifier is noninverting because of the sense of the output current.

The forward amplifier shown in Figure 48 and Figure 49 corresponds to one of the basic circuits used to characterize the OPA860. Extended characterization of this topology appears in the *Typical Characteristics* section of this data sheet.

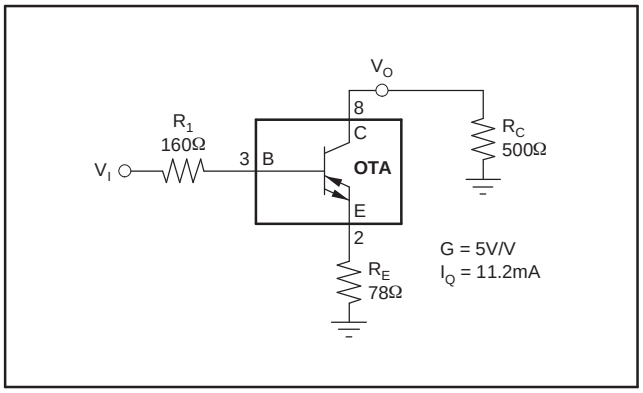


Figure 48. Forward Amplifier Configuration and Test Circuit

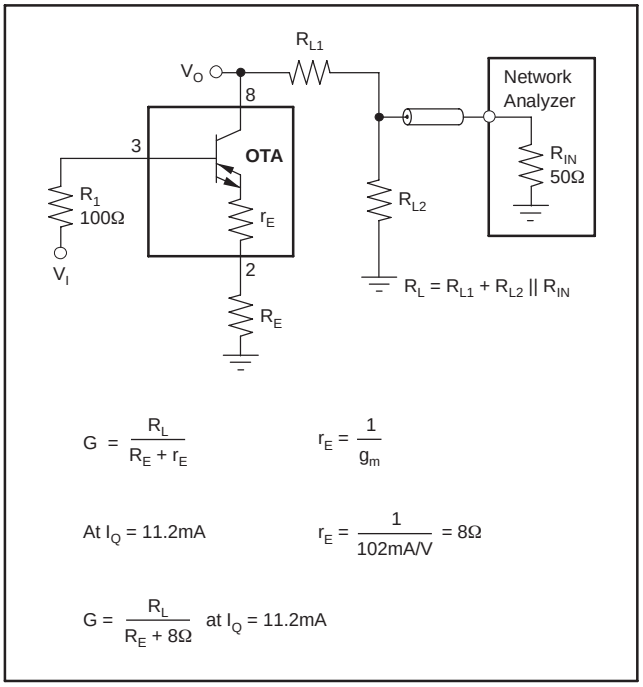


Figure 49. Forward Amplifier Design Equations

Common-C Amplifier

Figure 50b shows the OTA connected as an E-follower—a voltage buffer. It is interesting to notice that the larger the R_E resistor, the closer to unity gain the buffer will be. If the OTA section is to be used as a buffer, use $R_E \geq 500\Omega$ for best results. For the OTA section used as a buffer, the gain is given by Equation 3:

$$G = \frac{1}{1 + \frac{1}{g_m \times R_E}} \approx 1 \quad (3)$$

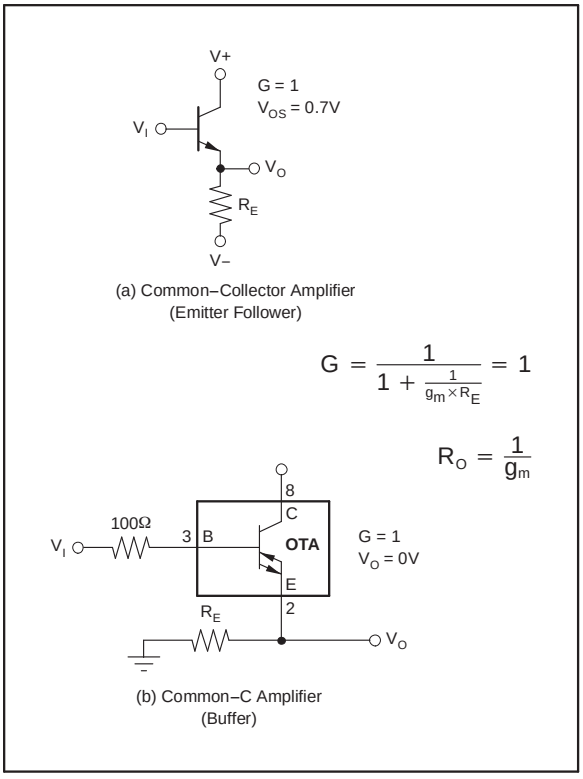


Figure 50. Common-Collector vs Common-C Amplifier

A low value resistor in series with the B OTA and buffer inputs is recommended. This resistor helps isolate trace parasitic from the inputs, reduces any tendency to oscillate, and controls frequency response peaking. Typical resistor values are from 25Ω to 200Ω.

Common-B Amplifier

Figure 51 shows the Common-B amplifier. This configuration produces an inverting gain and a low impedance input. Equation 4 shows the gain for this configuration.

$$G = \frac{R_L}{R_E + \frac{1}{g_m}} \approx -\frac{R_L}{R_E} \quad (4)$$

This low impedance can be converted to a high impedance by inserting the buffer amplifier in series.

Current-Mode Analog Computations

As mentioned earlier, the OTA section of the OPA860 can be used advantageously for analog computation. Among the application possibilities are functionality as a current amplifier, current differentiator, current integrator, current summer, and weighted current summer. Table 1 lists these different uses with the associated transfer functions.

These functions can easily be combined to form active filters. Some examples using these current-mode functions are shown later in this document.

OPA860 APPLICATIONS

The OPA860 is comprised of both the OTA section and the Buffer section. This applications information focuses more on using both sections together to form various useful amplifiers. A more thorough description of the OTA section in filter applications can be found in the OPA861 data sheet, available for download at www.ti.com.

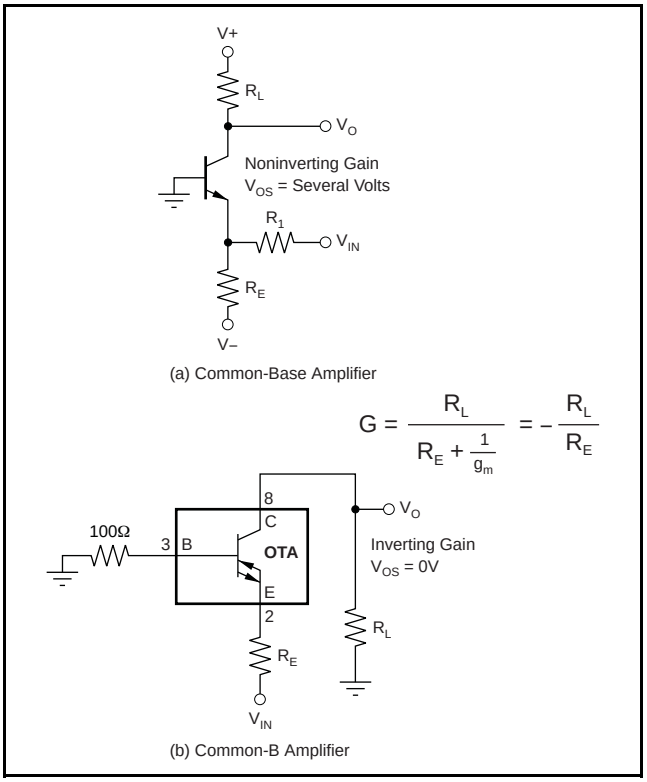


Figure 51. Common-Base Transistor vs Common-B OTA

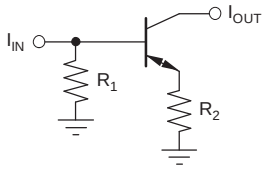
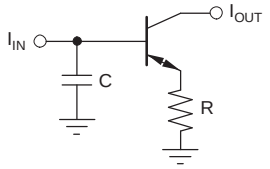
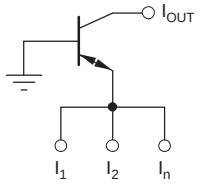
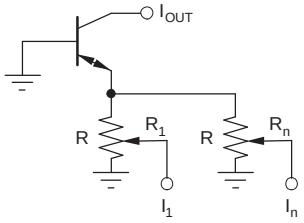
Direct Feedback Amplifier

The direct feedback amplifier (shown in Figure 53) topology has been used to characterize the OPA860. Extended characterization of this topology appears in the *Typical Characteristics* section of this data sheet. This topology is obtained by closing the loop between the C-output and the E-input of the common-E topology, and then buffered.

The gain for this topology is given by Equation 5:

$$G = \frac{\frac{R_3}{2} + R_5}{R_5 + \frac{1}{2 \times g_m}} \approx 1 + \frac{R_3}{2R_5} \quad (5)$$

Table 1. Current-Mode Analog Computation Using the OTA Section

FUNCTIONAL ELEMENT	TRANSFER FUNCTION	IMPLEMENTATION WITH THE OTA SECTION
Current Amplifier	$I_{OUT} = \frac{R_1}{R_2} \times I_{IN}$	
Current Integrator	$I_{OUT} = \frac{1}{C \times R \times \int I_{IN} dt}$	
Current Summer	$I_{OUT} = -\sum_{j=1}^{n} I_j$	
Weighted Current Summer	$I_{OUT} = -\sum_{j=1}^{n} I_j \times \frac{R_j}{R}$	

Current-Feedback Amplifier

Building a current-feedback amplifier with the OPA860 is extremely simple. One advantage of building a current-feedback amplifier with the OPA860 instead of getting an off-the-shelf current-feedback amplifier is the control gained on the bandwidth though the use of external capacitors. Figure 54 shows a typical circuit for the OPA860 in a noninverting current-feedback amplifier configuration. Input and output parasitic capacitances are shown. R_1 is the output impedance of the C-output of the OTA section. C_1 is the output parasitic capacitance on the C-output pin of the OTA-section. C_2 is the input parasitic capacitance for the input of the Buffer section. As shown in Equation 6, the poles formed by R_1, C_1, R_2, and C_2 control the frequency response. The frequency response in this configuration is shown in Figure 52. Setting an external capacitor on the C-output to ground allows adjusting the bandwidth.

$$\frac{V_{OUT}}{V_{IN}} = \frac{\alpha\left(1 + \frac{R_F}{R_G}\right)}{1 + \left(1 + \frac{R_F}{R_G}\right) \times \frac{1}{g_m \times R_1} \times [1 + s(R_1C_1 + R_1C_2 + R_2C_2) + s^2R_1C_1C_2]} \quad (6)$$

Note that both peaking and bandwidth can be adjusted by changing the feedback resistance, R_F.

Control-Loop Amplifier

A new type of control loop amplifier for fast and precise control circuits can be designed with the OPA860. The circuit of Figure 55 shows a series connection of two voltage control current sources that have an integral (and at higher frequencies, a proportional) behavior versus frequency. The control loop amplifiers show an integrator behavior from DC to the frequency, represented by the RC time constant of the network from the C-output to GND. Above this frequency, they operate as an amp with constant gain. The series connection increases the overall gain to about 110dB and thus minimizes the control loop deviation. The differential configuration at the inputs enables one to apply the measured output signal and the reference voltage to two identical high-impedance inputs. The output buffer decouples the C-output of the second OTA in order to insure the AC performance and to drive subsequent output stages.

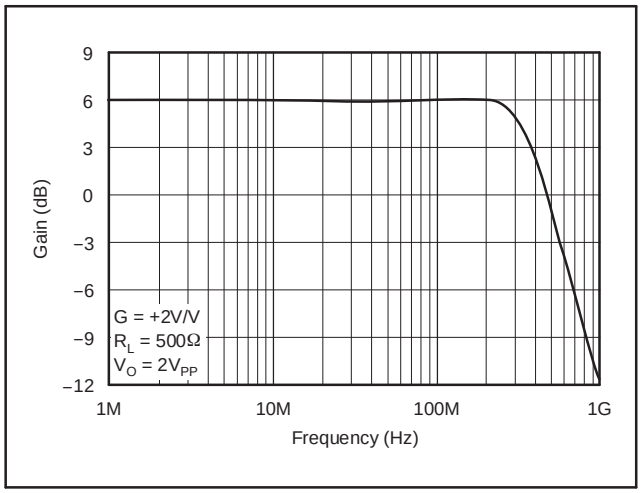


Figure 52. Current-Feedback Architecture Frequency Response

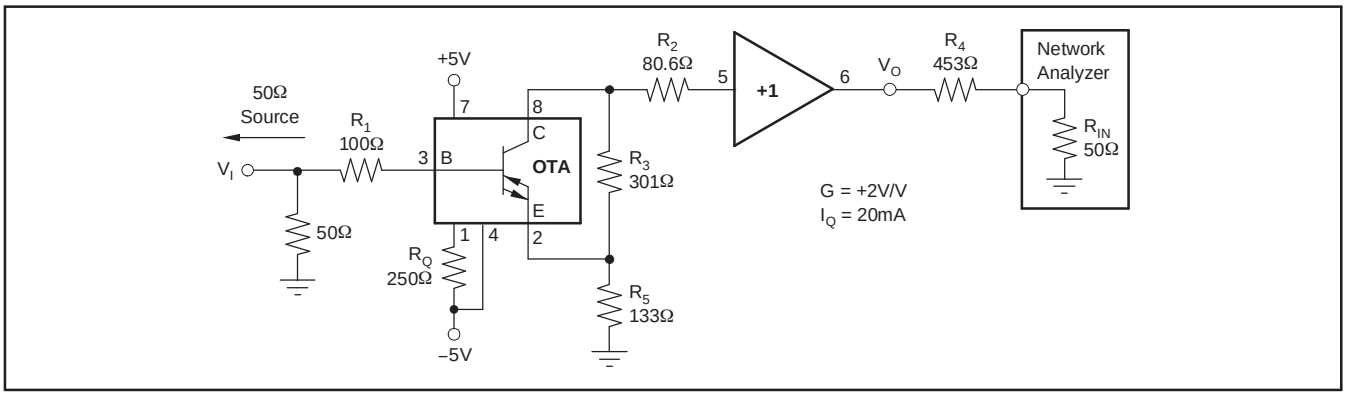


Figure 53. Direct Feedback Amplifier Specification and Test Circuit

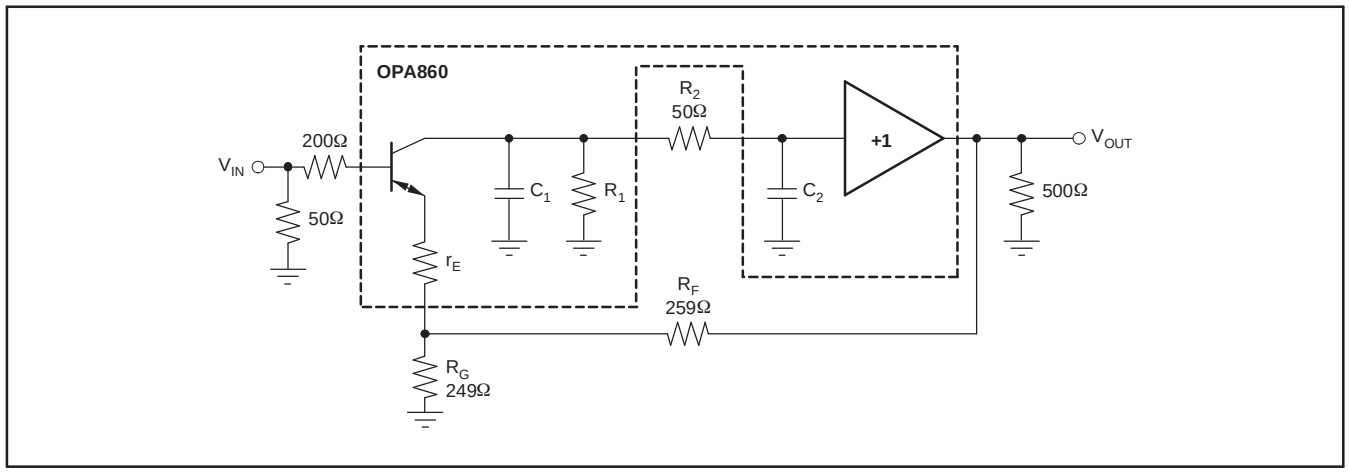


Figure 54. OPA860 Used in a Noninverting Current-Feedback Architecture

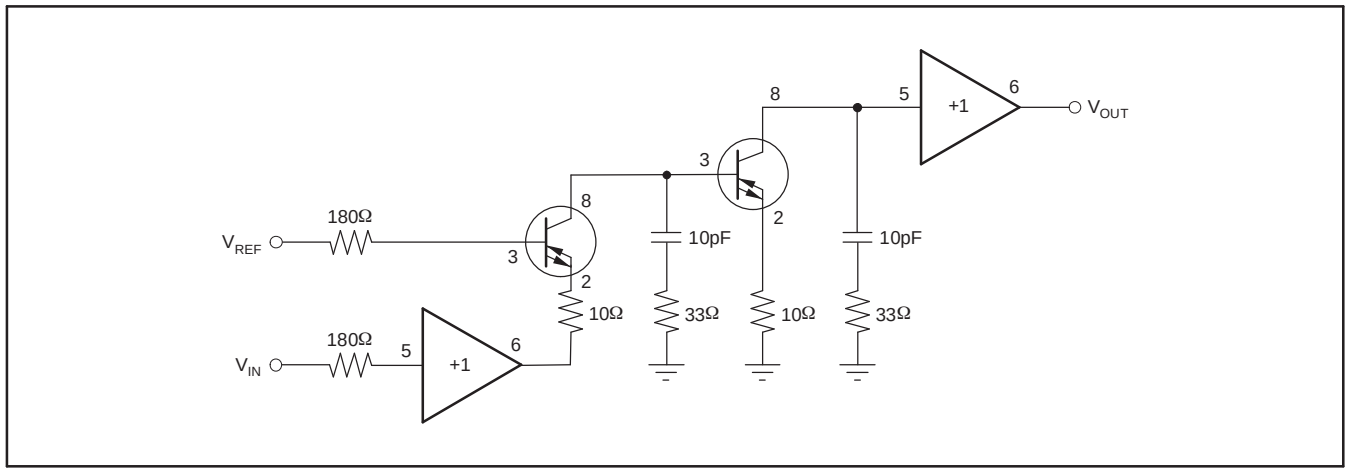


Figure 55. Control-Loop Amplifier Using Two OPA860s

DC-Restore Circuit

The OPA860 can be used advantageously with an operational amplifier, here the OPA820, as a DC-restore circuit. Figure 56 illustrates this design. Depending on the collector current of the transconductance amplifier (OTA) of the OPA860, a switching function is realized with the diodes D_1 and D_2.

When the C-output is sourcing current, the capacitor C_1 is being charged. When the C-output is sinking current, D_1 is turned off and D_2 is turned on, letting the voltage across C_1 be discharged through R_2.

The condition to charge C_1 is set by the voltage difference between V_{REF} and V_{OUT}. For the OTA C-output to source current, V_{REF} has to be greater than V_{OUT}. The rate of charge of C_1 is set by both R_1 and C_1. The discharge rate is given by R_2 and C_1.

Comparator

An interesting and also cost-effective circuit solution using the OPA860 as a low-jitter comparator is shown in Figure 57. At the same time, this circuit uses a positive and negative feedback. The input is connected to the inverting E-input. The output signal is applied in a direct feedback over the two antiparallel, connected gallium-arsenide diodes back to the emitter. A second feedback path over the RC combination to the base, which is a positive feedback, accelerates the output voltage change when the input voltage crosses the threshold voltage. The output voltage is limited to the threshold voltage of the back-to-back diodes.

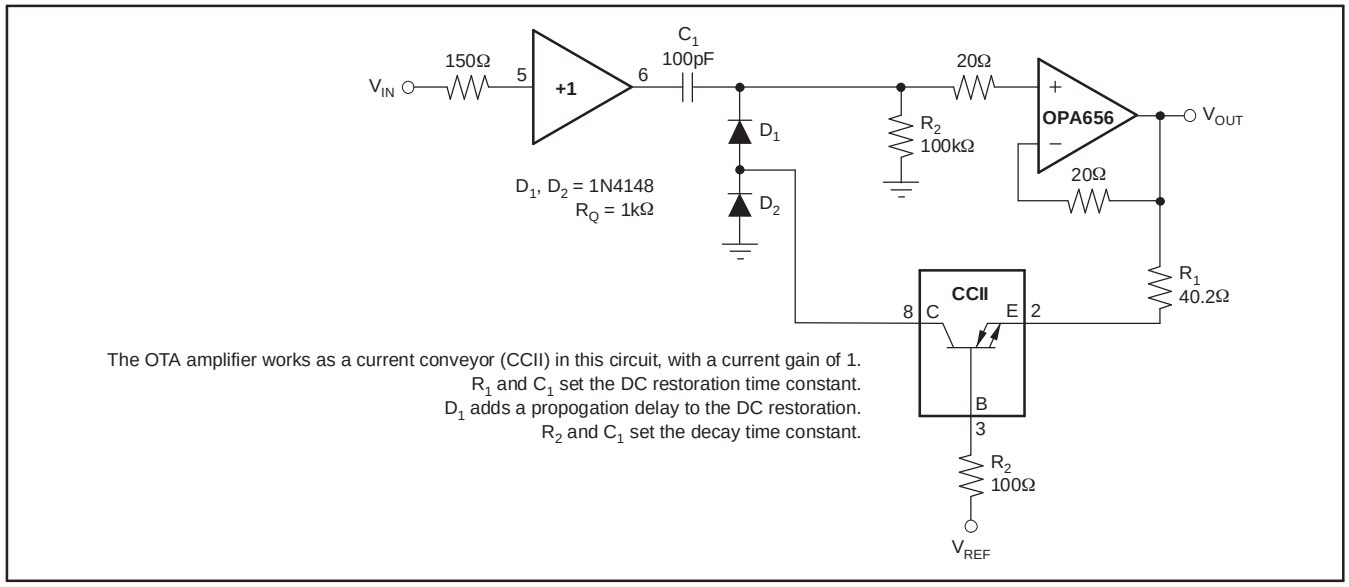


Figure 56. DC Restorer Circuit

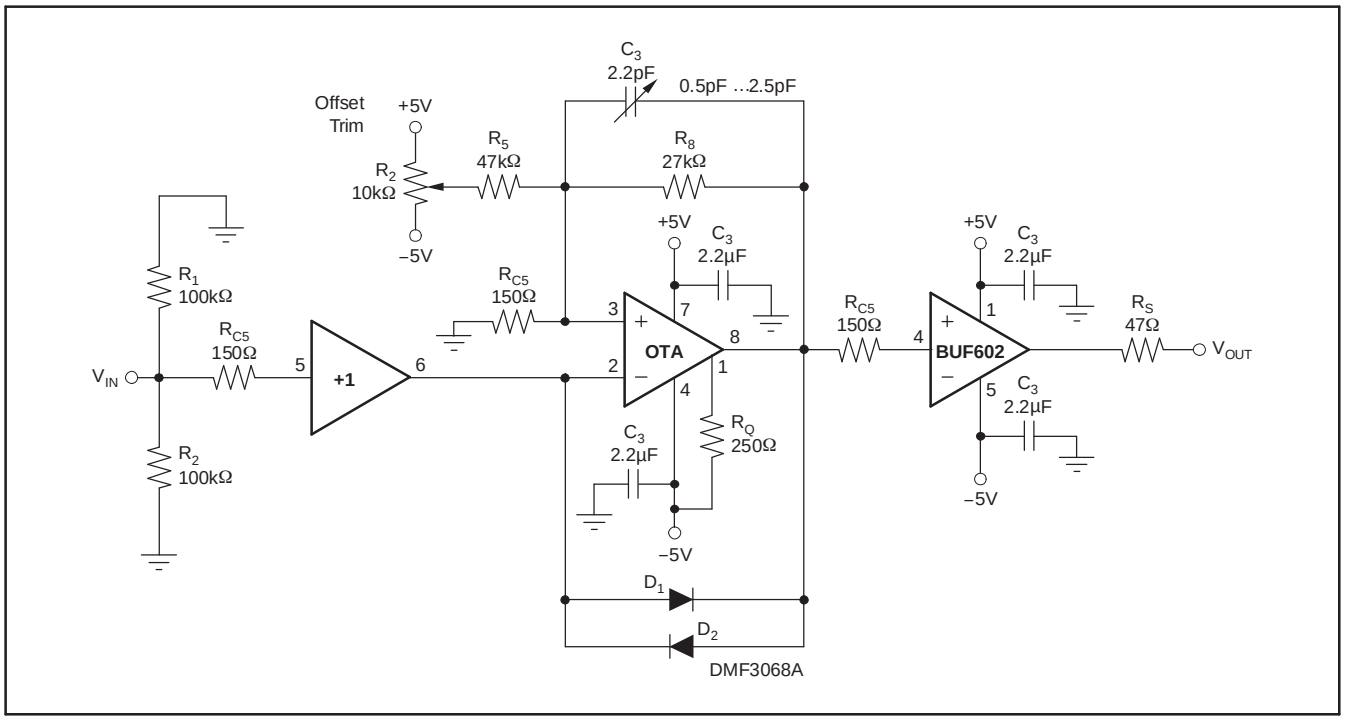


Figure 57. Comparator (Low Jitter)

Integrator for ns-Pulse

One very interesting application using the OPA860 in physical measurement technology is an open-loop ns-integrator (shown in Figure 58) which can process pulses with an amplitude of ±2.5V, have a rise/fall time of as little as 2ns, and also have a pulse width of more than 8ns. The voltage-controlled current source charges the integration capacitor linearly according to Equation 7:

$$V_C = V_{BE} \times g_m \times \frac{t}{C} \quad (7)$$

Where:

- V_C = Voltage At Pin 8
- V_{BE} = Base-Emitter Voltage
- g_m = Transconductance
- t = Time
- C = Integration Capacitance

The output voltage is the time integral of the input voltage. It can be calculated from Equation 8:

$$V_O = \frac{g_m}{C} \int_O^T V_{BE}\ dt \quad (8)$$

Where:

- V_O = Output Voltage
- T = Integration Time
- C = Integration Capacitance

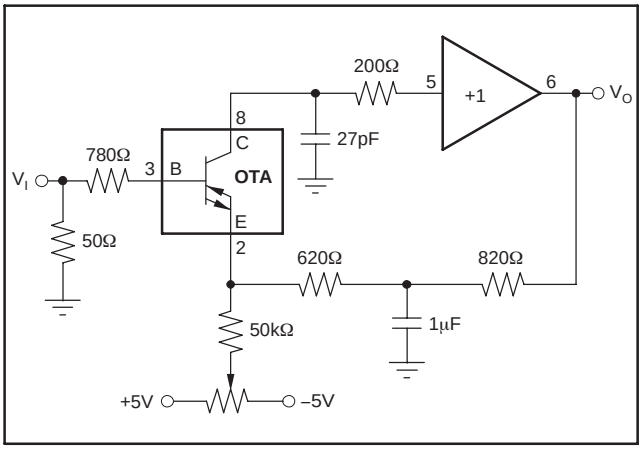


Figure 58. Integrator for ns-Pulses

Video Luminance Matrix

The inverting amplifier in Figure 59 amplifies the three input voltages that correspond to the luminance section of the RGB color signal. Different feedback resistances weight the voltages differently, resulting in an output voltage consisting of 30% of the red, 59% of the green, and 11% of the blue section of the input voltage. The way in which the signal is weighted corresponds to the transformation equation for converting RGB pictures into B/W pictures. The output signal is the black/white replay. It might drive a monochrome control monitor or an analog printer (hardcopy output).

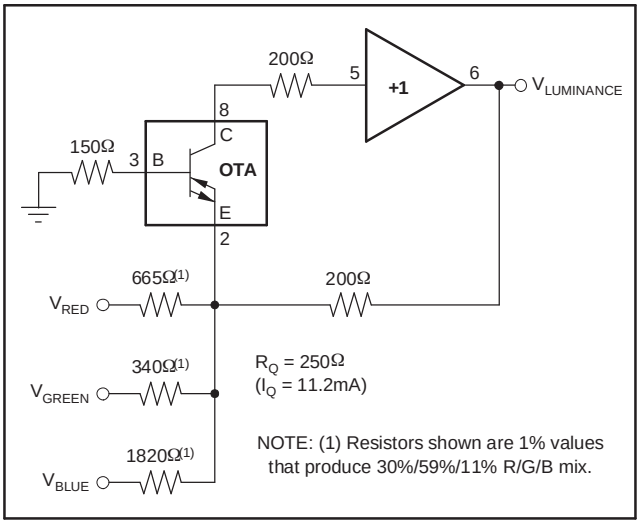


Figure 59. Video Luminance Matrix

State-Variable Filters

The ability of the OPA860 to easily drive a capacitor can be put to good use in implementing state-variable filters. A state-variable filter, or KHN filter, can be represented with integrators and coefficients. For example, the filter represented in the block diagram of Figure 60 can easily be implemented with two OPA860s, as shown in Figure 61.

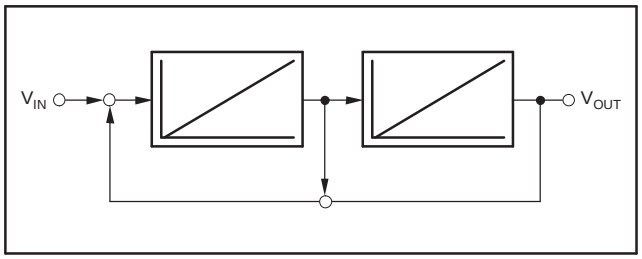


Figure 60. State Variable Filter Block Diagram

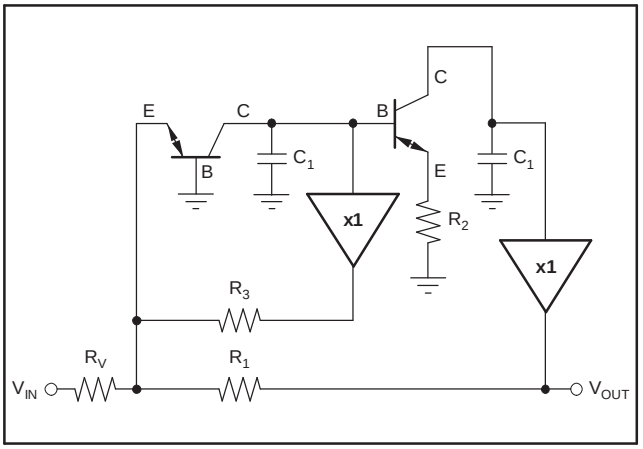


Figure 61. State Variable Filter Using the OPA860

The transfer function is then:

$$H(s) = \frac{a_0}{s^2 + C_1 s + C_0} = -\frac{R_1}{R_V} \times \frac{1}{1 + sC_2\frac{R_1 \times R_2}{R_3} + s^2 C_1 C_2 R_1 R_2} \quad (9)$$

$$\omega_0 = \frac{1}{\sqrt{C_1 C_2 R_1 R_2}} \quad (10)$$

$$Q = \sqrt{\frac{C_1}{C_2}} \times \frac{R_3}{\sqrt{R_1 R_2}} \quad (11)$$

DESIGN-IN TOOLS

DEMONSTRATION BOARDS

A printed circuit board (PCB) is available to assist in the initial evaluation of circuit performance using the OPA860. This module is available free, as an unpopulated PCB delivered with descriptive documentation. The summary information for the board is shown below:

PRODUCT	PACKAGE	BOARD PART NUMBER	LITERATURE REQUEST NUMBER
OPA860ID	SO-8	DEM-OTA-SO-1A	SBOU035A

The board can be requested on Texas Instruments web site (www.ti.com).

MACROMODELS AND APPLICATIONS SUPPORT

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. This principle is particularly true for Video and RF amplifier circuits where parasitic capacitance and inductance can have a major effect on circuit performance. A SPICE model for the OPA860 is available through the Texas Instruments web page (www.ti.com). These models do a good job of predicting small-signal AC and transient performance under a wide variety of operating conditions. They do not do as well in predicting the harmonic distortion. These models do not attempt to distinguish between the package types in their small-signal AC performance.

NOISE PERFORMANCE

The OTA noise model consists of three elements: a voltage noise on the B-input; a current noise on the B-input; and a current noise on the E-input. Figure 62 shows the OTA noise analysis model with all the noise terms included. In this model, all noise terms are taken to be noise voltage or current density terms in either nV/√Hz or pA/√Hz.

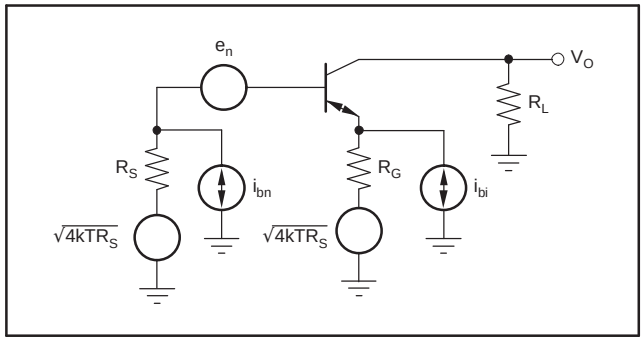


Figure 62. OTA Noise Analysis Model

The total output spot noise voltage can be computed as the square root of the sum of all squared output noise voltage contributors. Equation 12 shows the general form for the output noise voltage using the terms shown in Figure 62.

$$e_O = \sqrt{\left[e_n^2 + (R_S i_{bn})^2 + 4kTR_S\right]\left[\frac{R_L}{R_G + \frac{1}{g_m}}\right]^2 + \left[(R_G i_{bi})^2 + 4kTR_G\right]\frac{R_L}{\frac{1}{g_m}}} \quad (12)$$

For the buffer, the noise model is shown in Figure 63. Equation 13 shows the general form for the output noise voltage using the terms shown in Figure 63.

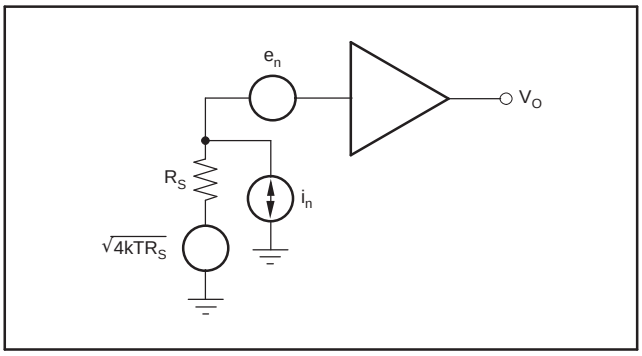


Figure 63. Buffer Noise Analysis Model

$$e_O = \sqrt{e_n^2 + (i_n R_S)^2 + 4kTR_S} \quad (13)$$

THERMAL ANALYSIS

Due to the high output power capability of the OPA860, heatsinking or forced airflow may be required under extreme operating conditions. Maximum desired junction temperature will set the maximum allowed internal power dissipation as described below. In no case should the maximum junction temperature be allowed to exceed +150°C.

Operating junction temperature (T_J) is given by $T_A + P_D \times \theta_{JA}$. The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} will depend on the required output signal and load but would, for a grounded resistive load, be at a maximum when the output is fixed at a voltage equal to 1/2 of either supply voltage (for equal bipolar supplies). Under this condition, $P_{DL} = V_S^2/(4 \times R_L)$ where R_L includes feedback network loading.

Note that it is the power in the output stage and not into the load that determines internal power dissipation.

As a worst-case example, compute the maximum T_J using an OPA860ID in the circuit of Figure 53 operating at the maximum specified ambient temperature of +85°C and driving a grounded 20Ω load.

$P_D = 10V \times 11.2mA + 5^2/(4 \times 20\Omega) = 424mW$

Maximum $T_J = +85°C + (0.43W \times 125°C/W) = 139°C$.

Although this is still well below the specified maximum junction temperature, system reliability considerations may require lower tested junction temperatures. The highest possible internal dissipation will occur if the load requires current to be forced into the output for positive output voltages or sourced from the output for negative output voltages. This puts a high current through a large internal voltage drop in the output transistors. The output V-I plot shown in the Typical Characteristics includes a boundary for 1W maximum internal power dissipation under these conditions.

BOARD LAYOUT GUIDELINES

Achieving optimum performance with a high-frequency amplifier like the OPA860 requires careful attention to board layout parasitics and external component types. Recommendations that will optimize performance include:

a) Minimize parasitic capacitance to any AC ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability: on the noninverting input, it can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.

b) Minimize the distance (< 0.25") from the power-supply pins to high-frequency 0.1µF decoupling capacitors. At the device pins, the ground and power-plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections should always be decoupled with these capacitors. An optional supply decoupling capacitor (0.1µF) across the two power supplies (for bipolar operation) will improve 2nd-harmonic distortion performance. Larger (2.2µF to 6.8µF) decoupling capacitors, effective at lower frequency, should also be used on the main supply pins. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PC board.

c) Careful selection and placement of external components will preserve the high-frequency performance of the OPA860. Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal film or carbon composition, axially-leaded resistors can also provide good high-frequency performance. Again, keep their leads and PC board traces as short as possible. Never use wirewound type resistors in a high-frequency application.

d) Connections to other wideband devices on the board may be made with short, direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50mils to 100mils) should be used, preferably with ground and power planes opened up around them. If a long trace is required at the buffer output, and the 6dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is normally not necessary on board, and in fact, a higher impedance environment will improve distortion as shown in the distortion versus load plots.

e) Socketing a high-speed part like the OPA860 is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network that makes it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the OPA860 onto the board.

INPUT AND ESD PROTECTION

The OPA860 is built using a very high-speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the *Absolute Maximum Ratings* table. All device pins are protected with internal ESD protection diodes to the power supplies as shown in Figure 64.

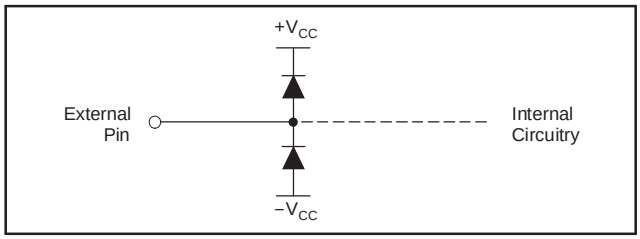


Figure 64. Internal ESD Protection

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes can typically support 30mA continuous current. Where higher currents are possible (for example, in systems with ±15V supply parts driving into the OPA860), current-limiting series resistors should be added into the two inputs. Keep these resistor values as low as possible since high values degrade both noise performance and frequency response.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (June 2006) to Revision C **Page**

- Changed storage temperature range rating in Absolute Maximum Ratings table from –40°C to +125°C to –65°C to +125°C 2

Changes from Revision A (January 2006) to Revision B **Page**

- Changed Figure 49—corrected equations 16
- Changed Figure 58—corrected resistor value 22

PACKAGING INFORMATION

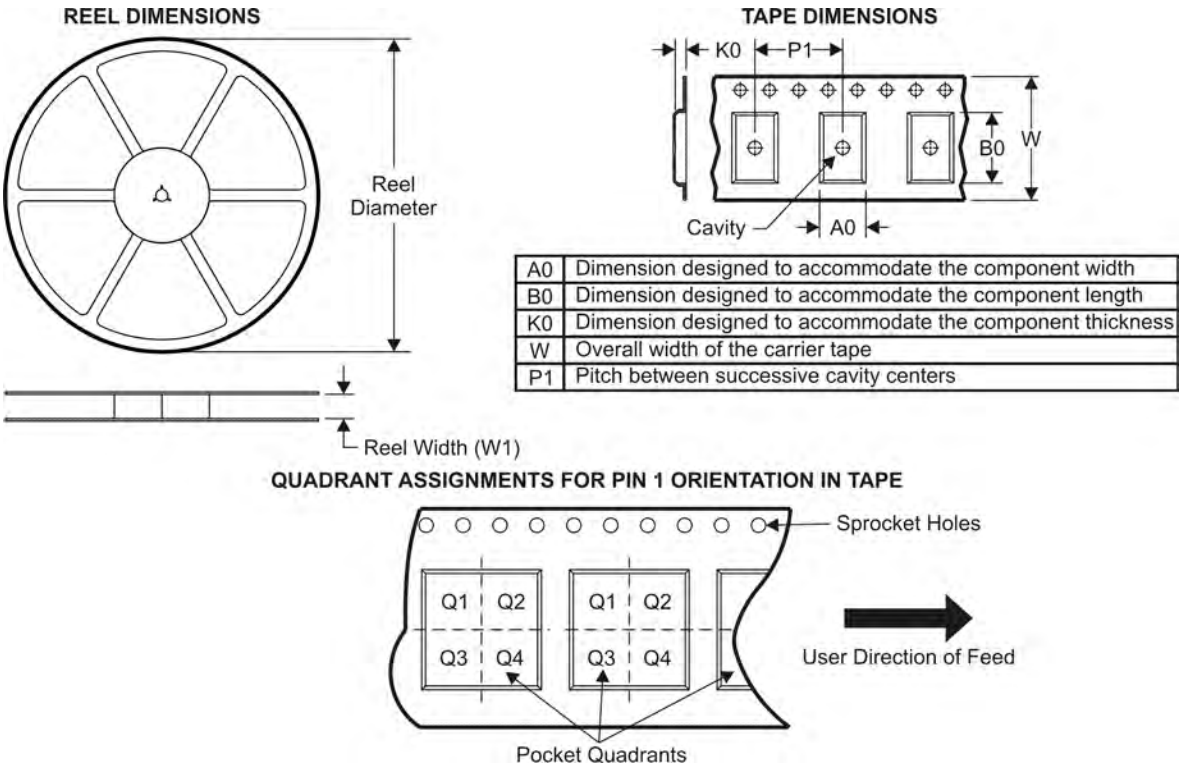
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
OPA860ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA860IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA860IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
OPA860IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

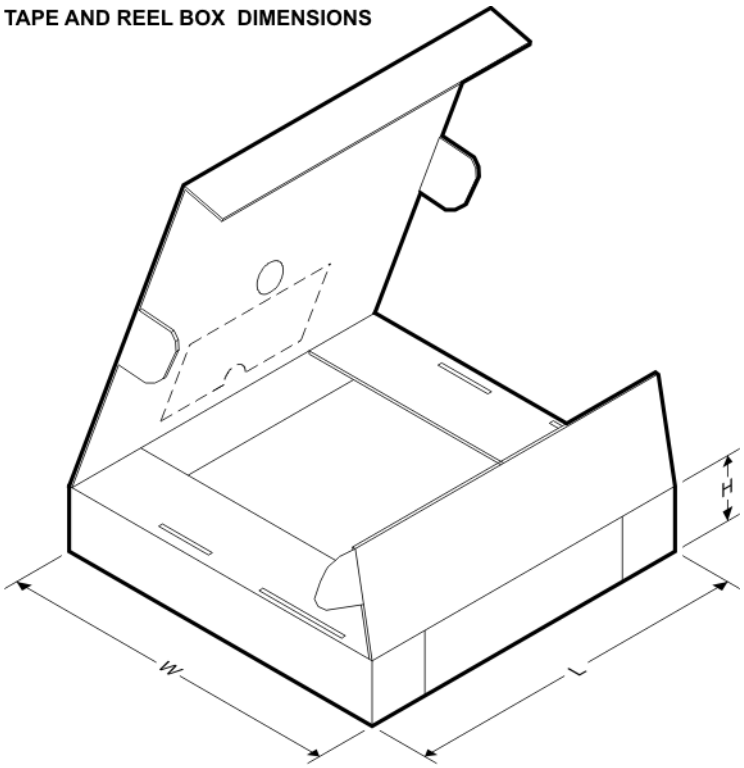


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA860IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

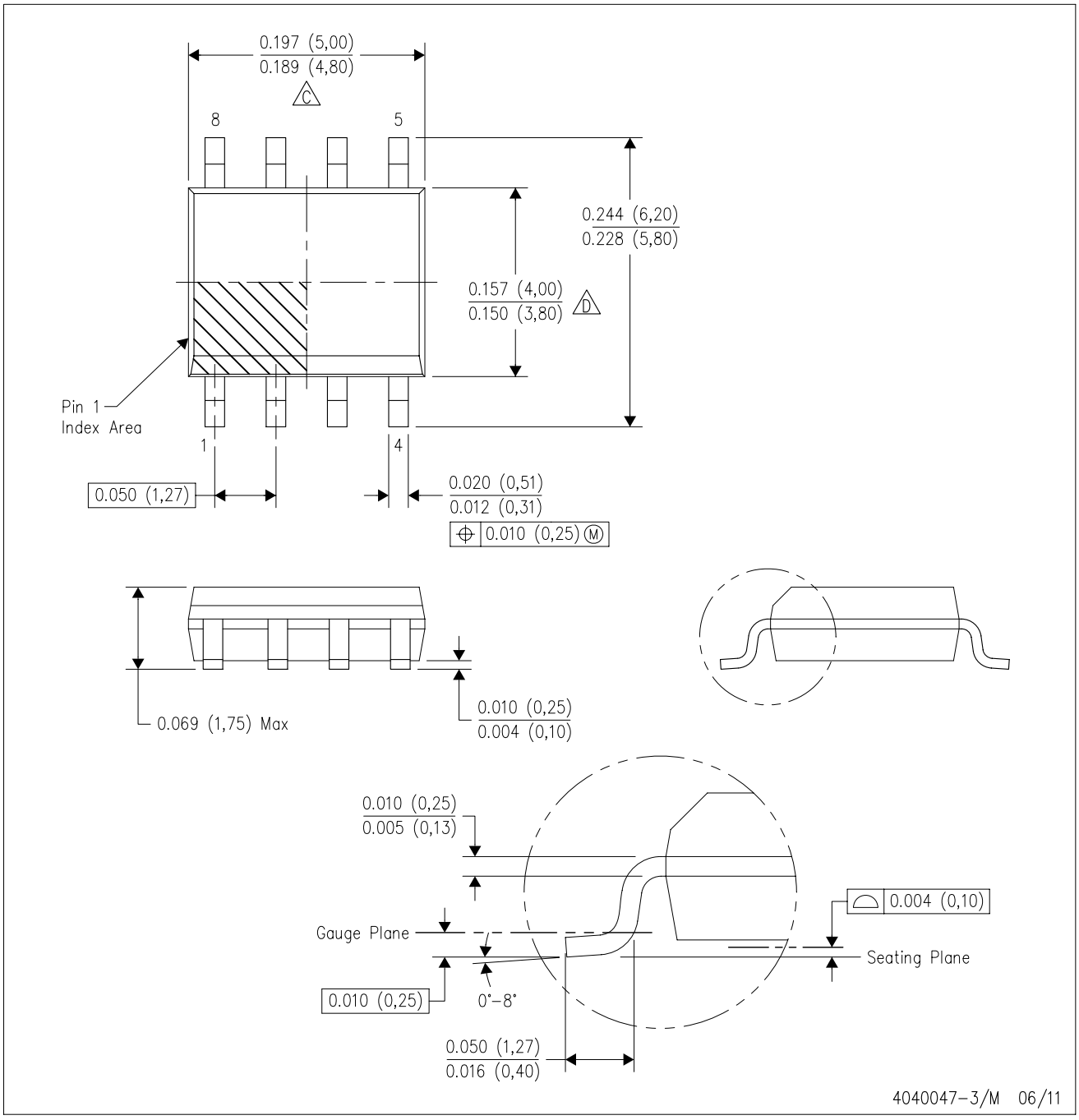
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

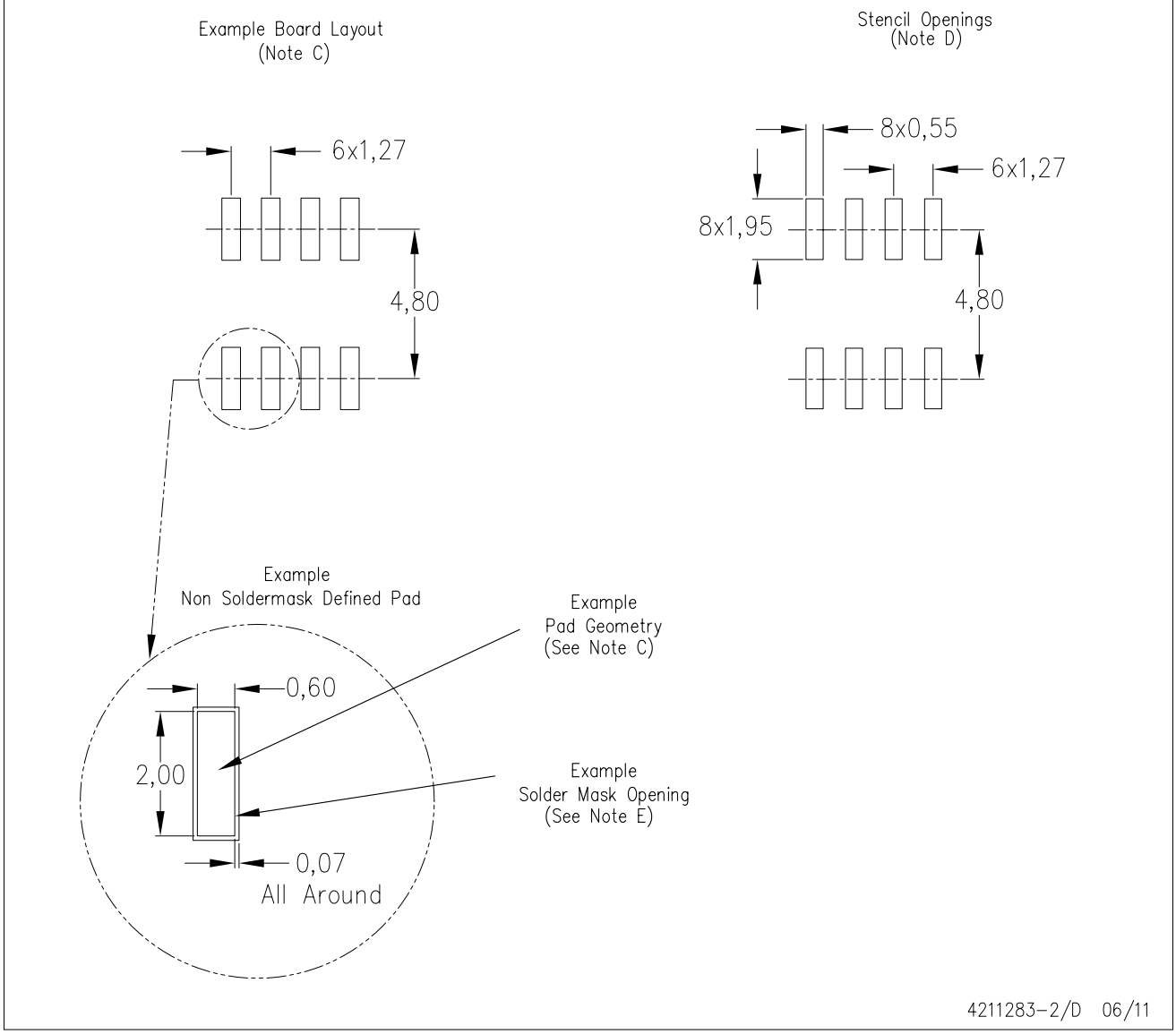
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA860IDR	SOIC	D	8	2500	346.0	346.0	29.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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DLP® Products	www.dlp.com	Energy and Lighting	www.ti.com/energy
DSP	dsp.ti.com	Industrial	www.ti.com/industrial
Clocks and Timers	www.ti.com/clocks	Medical	www.ti.com/medical
Interface	interface.ti.com	Security	www.ti.com/security
Logic	logic.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
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RFID	www.ti-rfid.com	Wireless	www.ti.com/wireless-apps
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High Side Current Sense Amplifier with Reference and Comparator

FEATURES

- Current Sense Amplifier
  - Fast Step Response: 500ns
  - Low Offset Voltage: 125µV Maximum
  - Low Gain Error: 0.2% Maximum
- Internal 400mV Precision Reference
- Internal Comparator
  - Fast Response Time: 500ns
  - Total Threshold Error: ±1.25% Maximum
  - Latching or Non-Latching Comparator Option
- Wide Supply Range: 2.7V to 60V
- Supply Current: 450µA
- Low Shutdown Current: 5µA Maximum
- Specified for –40°C to 125°C Temperature Range
- Available in 8-Lead MSOP and 8-Lead (2mm × 3mm) DFN Packages

APPLICATIONS

- Overcurrent and Fault Detection
- Current Shunt Measurement
- Battery Monitoring
- Motor Control
- Automotive Monitoring and Control
- Remote Sensing
- Industrial Control

DESCRIPTION

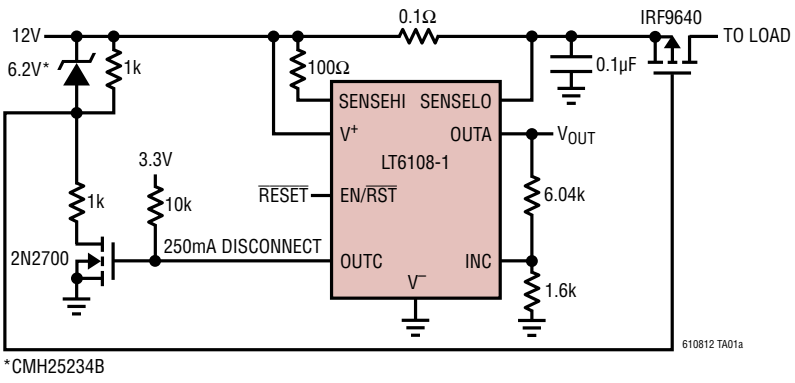
The LT®6108 is a complete high side current sense device that incorporates a precision current sense amplifier, an integrated voltage reference and a comparator. Two versions of the LT6108 are available. The LT6108-1 has a latching comparator and the LT6108-2 has a non-latching comparator. In addition, the current sense amplifier and comparator inputs and outputs are directly accessible. The amplifier gain and comparator trip point are configured by external resistors. The open-drain comparator output allows for easy interface to other system components.

The overall propagation delay of the LT6108 is typically only 1.4µs, allowing for quick reaction to overcurrent conditions. The 1MHz bandwidth allows the LT6108 to be used for error detection in critical applications such as motor control. The high threshold accuracy of the comparator, combined with the ability to latch the comparator, ensures the LT6108 can capture high speed events.

The LT6108 is fully specified for operation from –40°C to 125°C, making it suitable for industrial and automotive applications. The LT6108 is available in the small 8-lead MSOP and 8-lead DFN packages.

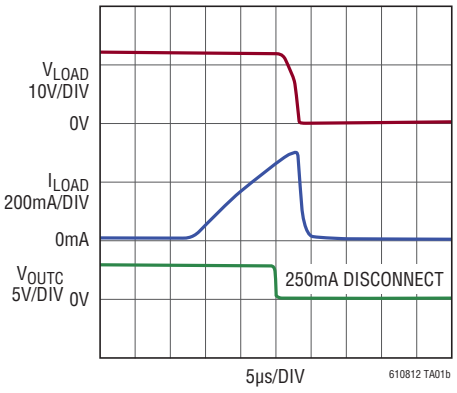
TYPICAL APPLICATION

Circuit Fault Protection with Very Fast Latching Load Disconnect



*CMH25234B

Response to Overcurrent Event

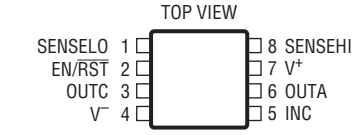


ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V^+ to V^-) 60V
Maximum Voltage
(SENSELO, SENSEHI, OUTA) ..... V^+ + 1V
Maximum V^+ – (SENSELO or SENSEHI) 33V
Maximum EN, EN/$\overline{RST}$ Voltage 60V
Maximum Comparator Input Voltage 60V
Maximum Comparator Output Voltage 60V
Input Current (Note 2) ..... –10mA
SENSEHI, SENSELO Input Current ..... ±10mA
Differential SENSEHI or SENSELO Input Current .. ±2.5mA
Amplifier Output Short-Circuit Duration (to V^-) .. Indefinite
Operating Temperature Range (Note 3)
LT6108I ..... –40°C to 85°C
LT6108H ..... –40°C to 125°C
Specified Temperature Range (Note 3)
LT6108I ..... –40°C to 85°C
LT6108H ..... –40°C to 125°C
Maximum Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
MSOP Lead Temperature (Soldering, 10 sec) ..... 300°C

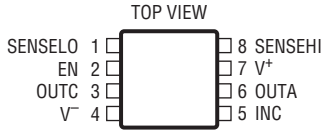
PIN CONFIGURATION

LT6108-1

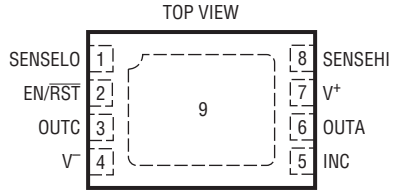


MS8 PACKAGE
8-LEAD PLASTIC MSOP
θ_{JA} = 163°C/W, θ_{JC} = 45°C/W

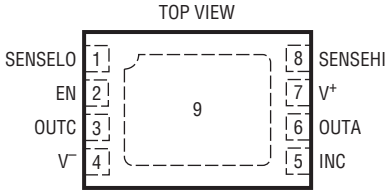
LT6108-2



MS8 PACKAGE
8-LEAD PLASTIC MSOP
θ_{JA} = 163°C/W, θ_{JC} = 45°C/W



DCB PACKAGE
8-LEAD (2mm × 3mm) PLASTIC DFN
θ_{JA} = 64°C/W, θ_{JC} = 10°C/W
EXPOSED PAD (PIN 9) IS V^-, PCB CONNECTION OPTIONAL



DCB PACKAGE
8-LEAD (2mm × 3mm) PLASTIC DFN
θ_{JA} = 64°C/W, θ_{JC} = 10°C/W
EXPOSED PAD (PIN 9) IS V^-, PCB CONNECTION OPTIONAL

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LT6108AIMS8-1#PBF	LT6108AIMS8-1#TRPBF	LTFND	8-Lead Plastic MSOP	–40°C to 85°C
LT6108IMS8-1#PBF	LT6108IMS8-1#TRPBF	LTFND	8-Lead Plastic MSOP	–40°C to 85°C
LT6108AHMS8-1#PBF	LT6108AHMS8-1#TRPBF	LTFND	8-Lead Plastic MSOP	–40°C to 125°C
LT6108HMS8-1#PBF	LT6108HMS8-1#TRPBF	LTFND	8-Lead Plastic MSOP	–40°C to 125°C
LT6108AIMS8-2#PBF	LT6108AIMS8-2#TRPBF	LTFNG	8-Lead Plastic MSOP	–40°C to 85°C
LT6108IMS8-2#PBF	LT6108IMS8-2#TRPBF	LTFNG	8-Lead Plastic MSOP	–40°C to 85°C
LT6108AHMS8-2#PBF	LT6108AHMS8-2#TRPBF	LTFNG	8-Lead Plastic MSOP	–40°C to 125°C
LT6108HMS8-2#PBF	LT6108HMS8-2#TRPBF	LTFNG	8-Lead Plastic MSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

Lead Free Finish

TAPE AND REEL (MINI)	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LT6108IDCB-1#TRMPBF	LT6108IDCB-1#TRPBF	LFNF	8-Lead (2mm × 3mm) Plastic DFN	–40°C to 85°C
LT6108HDCB-1#TRMPBF	LT6108HDCB-1#TRPBF	LFNF	8-Lead (2mm × 3mm) Plastic DFN	–40°C to 125°C
LT6108IDCB-2#TRMPBF	LT6108IDCB-2#TRPBF	LFNH	8-Lead (2mm × 3mm) Plastic DFN	–40°C to 85°C
LT6108HDCB-2#TRMPBF	LT6108HDCB-2#TRPBF	LFNH	8-Lead (2mm × 3mm) Plastic DFN	–40°C to 125°C

TRM = 500 pieces. *Temperature grades are identified by a label on the shipping container.

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 12V, V_{PULLUP} = V^+, V_{EN} = $V_{EN/\overline{RST}}$ = 2.7V, R_{IN} = 100Ω, R_{OUT} = R1 + R2 = 10k, gain = 100, R_C = 25.5k, C_L = C_{LC} = 2pF, unless otherwise noted. (See Figure 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V^+	Supply Voltage Range		●	2.7		60	V
I_S	Supply Current (Note 4)	V^+ = 2.7V, R_{IN} = 1k, V_{SENSE} = 5mV			450		µA
		V^+ = 60V, R_{IN} = 1k, V_{SENSE} = 5mV	 ●		550	650 950	µA µA
	Supply Current in Shutdown	V^+ = 2.7V, $V_{EN/\overline{RST}}$ = 0V, R_{IN} = 1k, V_{SENSE} = 0.5V	 ●		3	5 7	µA µA
		V^+ = 60V, $V_{EN/\overline{RST}}$ = 0V, R_{IN} = 1k, V_{SENSE} = 0.5V	 ●		7	11 13	µA µA
	EN/$\overline{RST}$ Pin Current	$V_{EN/\overline{RST}}$ = 0V, V^+ = 60V (LT6108-1 Only)			–200		nA
	EN Pin Current	V_{EN} = 0V, V^+ = 60V (LT6108-2 Only)			–100		nA
V_{IH}	EN/$\overline{RST}$ Pin Input High	V^+ = 2.7V to 60V (LT6108-1 Only)	●	1.9			V
V_{IL}	EN/$\overline{RST}$ Pin Input Low	V^+ = 2.7V to 60V (LT6108-1 Only)	●			0.8	V
V_{IH}	EN Pin Input High	V^+ = 2.7V to 60V (LT6108-2 Only)	●	1.9			V
V_{IL}	EN Pin Input Low	V^+ = 2.7V to 60V (LT6108-2 Only)	●			0.8	V
Current Sense Amplifier							
V_{OS}	Input Offset Voltage	V_{SENSE} = 5mV, LT6108A V_{SENSE} = 5mV, LT6108 V_{SENSE} = 5mV, LT6108A V_{SENSE} = 5mV, LT6108	 ● ●	–125 –350 –250 –450		125 350 250 450	µV µV µV µV
$\Delta V_{OS}/\Delta T$	Input Offset Voltage Drift	V_{SENSE} = 5mV	●		±0.8		µV/°C
I_B	Input Bias Current (SENSELO, SENSEHI)	V^+ = 2.7V to 60V	 ●		60	300 350	nA nA
I_{OS}	Input Offset Current	V^+ = 2.7V to 60V			±5		nA
I_{OUTA}	Output Current (Note 5)		●	1			mA
PSRR	Power Supply Rejection Ratio (Note 6)	V^+ = 2.7V to 60V	 ●	120 114	127		dB dB
CMRR	Common Mode Rejection Ratio	V^+ = 36V, V_{SENSE} = 5mV, V_{ICM} = 2.7V to 36V			125		dB
		V^+ = 60V, V_{SENSE} = 5mV, V_{ICM} = 27V to 60V	 ●	110 103	125		dB dB
$V_{SENSE(MAX)}$	Full-Scale Input Sense Voltage (Note 5)	R_{IN} = 500Ω	●	500			mV
	Gain Error (Note 7)	V^+ = 2.7V to 12V V^+ = 12V to 60V, V_{SENSE} = 5mV to 100mV, MS8 Package V^+ = 12V to 60V, V_{SENSE} = 5mV to 100mV, DFN Package	 ● ●	 –0.2 –0.3	–0.08	 0 0	% % %
	SENSELO Voltage (Note 8)	V^+ = 2.7V, V_{SENSE} = 100mV, R_{OUT} = 2k V^+ = 60V, V_{SENSE} = 100mV	● ●	2.5 27			V V
	Output Swing High (V^+ to V_{OUTA})	V^+ = 2.7V, V_{SENSE} = 27mV	●			0.2	V
		V^+ = 12V, V_{SENSE} = 120mV	●			0.5	V
BW	Signal Bandwidth	I_{OUT} = 1mA I_{OUT} = 100µA			1 140		MHz kHz
t_r	Input Step Response (to 50% of Final Output Voltage)	V^+ = 2.7V, V_{SENSE} = 24mV Step, Output Rising Edge V^+ = 12V to 60V, V_{SENSE} = 100mV Step, Output Rising Edge			500 500		ns ns
t_{SETTLE}	Settling Time to 1%	V_{SENSE} = 10mV to 100mV, R_{OUT} = 2k			2		µs

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 12V, V_{PULLUP} = V^+, V_{EN} = $V_{EN/\overline{RST}}$ = 2.7V, R_{IN} = 100Ω, R_{OUT} = R1 + R2 = 10k, gain = 100, R_C = 25.5k, C_L = C_{LC} = 2pF, unless otherwise noted. (See Figure 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Reference and Comparator							
$V_{TH(R)}$ (Note 9)	Rising Input Threshold Voltage	V^+ = 2.7V to 60V, LT6108A V^+ = 2.7V to 60V, LT6108	● ●	395 392	400 400	405 408	mV mV
V_{HYS}	$V_{HYS} = V_{TH(R)} - V_{TH(F)}$	V^+ = 2.7V to 60V		3	10	15	mV
	Comparator Input Bias Current	V_{INC} = 0V, V^+ = 60V	●	–50			nA
V_{OL}	Output Low Voltage	I_{OUTC} = 500µA, V^+ = 2.7V	 ●		60	150 220	mV mV
	High to Low Propagation Delay	5mV Overdrive 100mV Overdrive			3 0.5		µs µs
	Output Fall Time				0.08		µs
t_{RESET}	Reset Time	LT6108-1 Only			0.5		µs
t_{RPW}	Valid $\overline{RST}$ Pulse Width	LT6108-1 Only	●	2		15	µs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Input and output pins have ESD diodes connected to ground. The SENSEHI and SENSELO pins have additional current handling capability specified as SENSEHI, SENSELO Input Current.

Note 3: The LT6108I is guaranteed to meet specified performance from –40°C to 85°C. LT6108H is guaranteed to meet specified performance from –40°C to 125°C.

Note 4: Supply current is specified with the comparator output high. When the comparator output goes low the supply current will increase by 75µA typically.

Note 5: The full-scale input sense voltage and the maximum output current must be considered to achieve the specified performance.

Note 6: Supply voltage and input common mode voltage are varied while amplifier input offset voltage is monitored.

Note 7: The specified gain error does not include the effect of external resistors R_{IN} and R_{OUT}. Although gain error is only guaranteed between 12V and 60V, similar performance is expected for V^+ < 12V, as well.

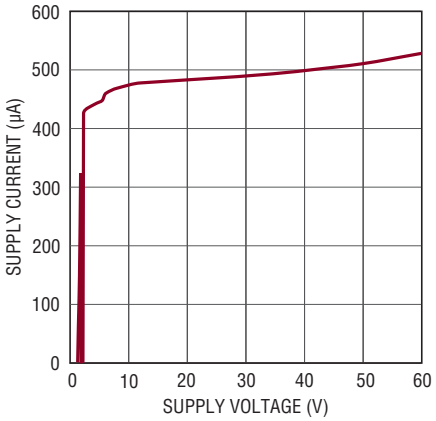
Note 8: Refer to SENSELO, SENSEHI Range in the Applications Information section for more information.

Note 9: The input threshold voltage which causes the output voltage of the comparator to transition from high to low is specified. The input voltage which causes the comparator output to transition from low to high is the magnitude of the difference between the specified threshold and the hysteresis.

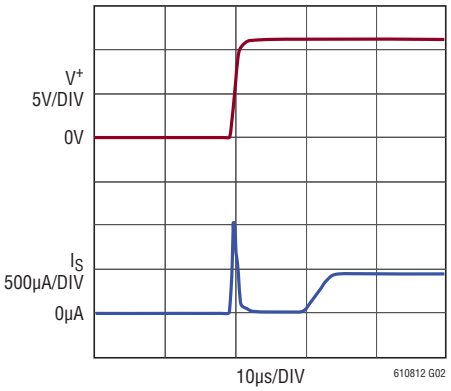
TYPICAL PERFORMANCE CHARACTERISTICS

Performance characteristics taken at T_A = 25°C, V^+ = 12V, V_{PULLUP} = V^+, V_{EN} = $V_{EN/\overline{RST}}$ = 2.7V, R_{IN} = 100Ω, R_{OUT} = R1 + R2 = 10k, gain = 100, R_C = 25.5k, C_L = C_{LC} = 2pF, unless otherwise noted. (See Figure 3)

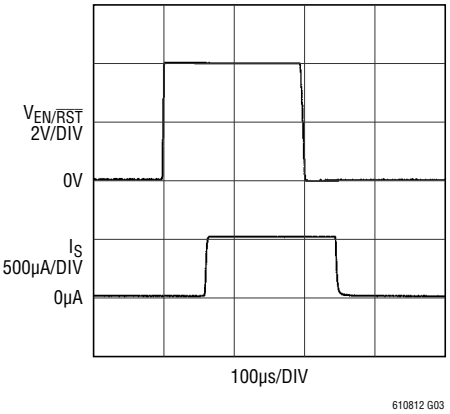
Supply Current vs Supply Voltage



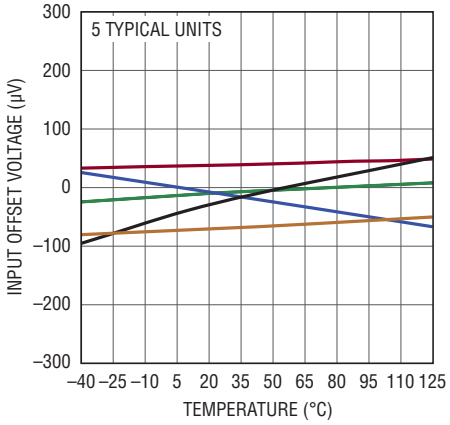
Start-Up Supply Current



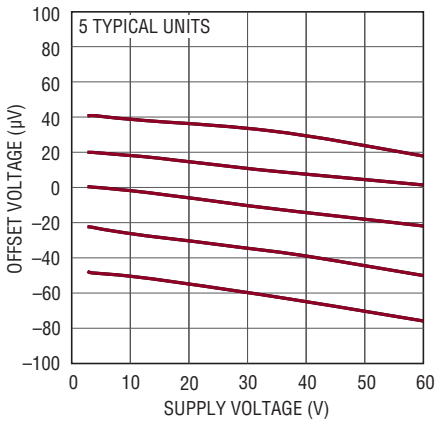
Enable/Disable Response



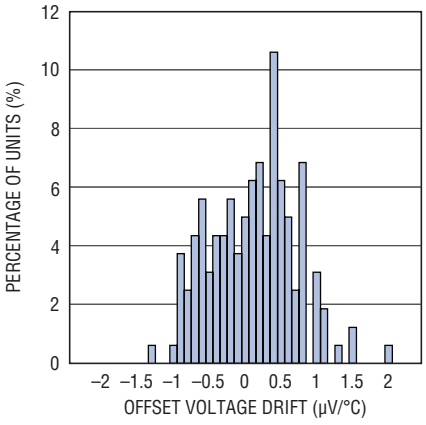
Input Offset Voltage vs Temperature



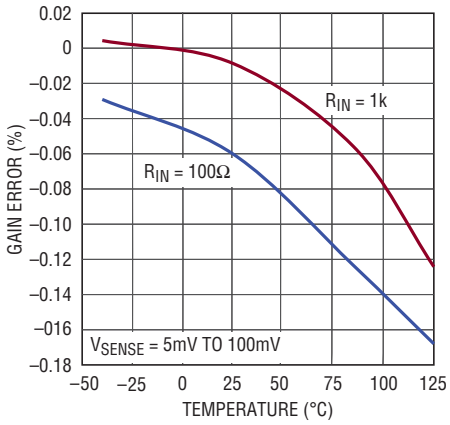
Amplifier Offset Voltage vs Supply Voltage



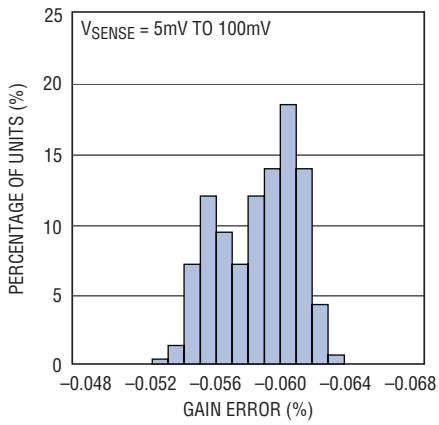
Offset Voltage Drift Distribution



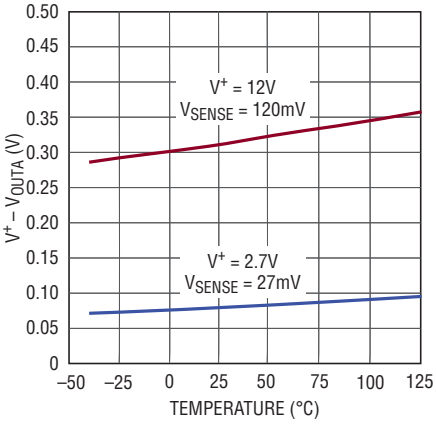
Amplifier Gain Error vs Temperature



Amplifier Gain Error Distribution



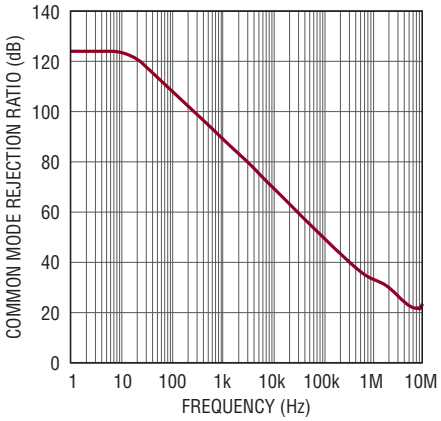
Amplifier Output Swing vs Temperature



TYPICAL PERFORMANCE CHARACTERISTICS

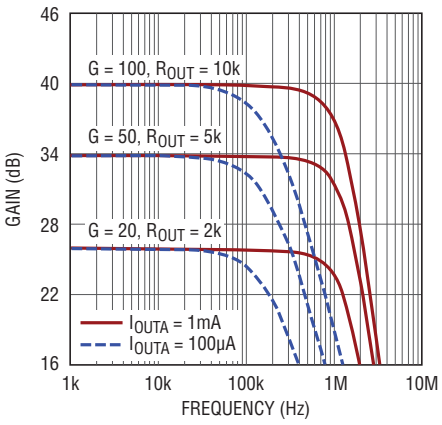
Performance characteristics taken at T_A = 25°C, V^+ = 12V, V_{PULLUP} = V^+, V_{EN} = $V_{EN/\overline{RST}}$ = 2.7V, R_{IN} = 100Ω, R_{OUT} = R1 + R2 = 10k, gain = 100, R_C = 25.5k, C_L = C_{LC} = 2pF, unless otherwise noted. (See Figure 3)

Common Mode Rejection Ratio vs Frequency



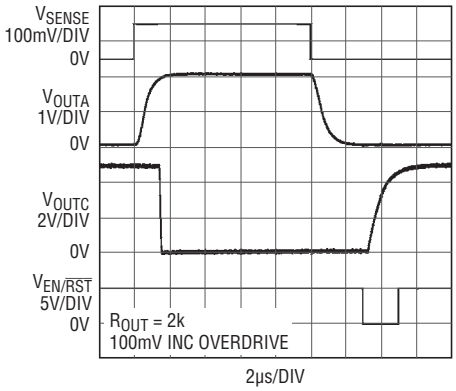
610812 G09

Amplifier Gain vs Frequency



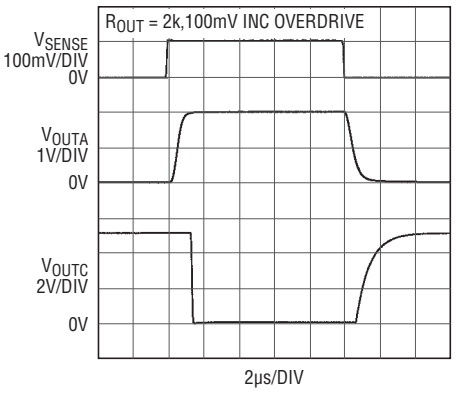
610812 G10

LT6108-1 Step Response



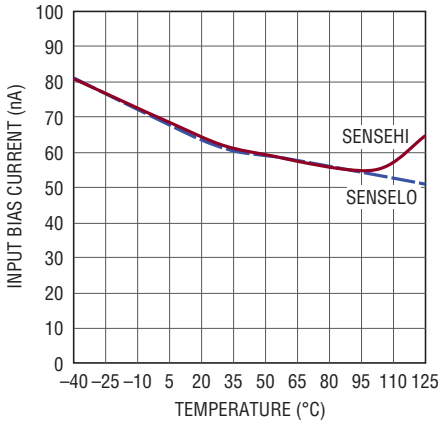
610812 G11

LT6108-2 Step Response



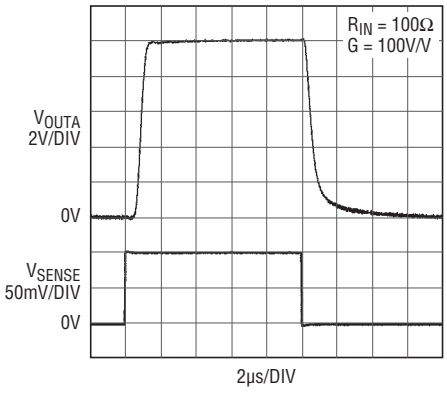
610812 G12

Amplifier Input Bias Current vs Temperature



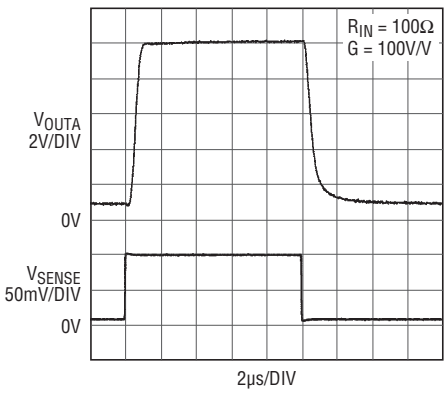
610812 G13

Amplifier Step Response (V_{SENSE} = 0mV to 100mV)



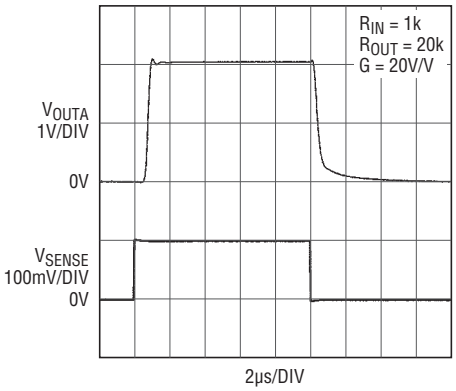
610812 G14

Amplifier Step Response (V_{SENSE} = 10mV to 100mV)



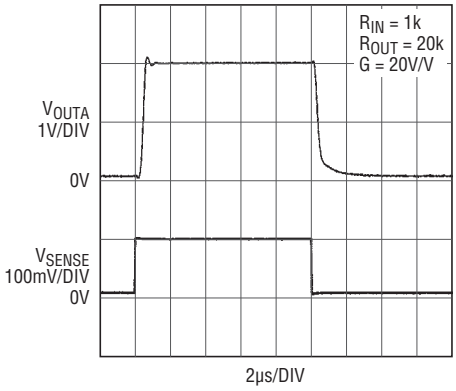
610812 G15

Amplifier Step Response (V_{SENSE} = 0mV to 100mV)



610812 G16

Amplifier Step Response (V_{SENSE} = 10mV to 100mV)

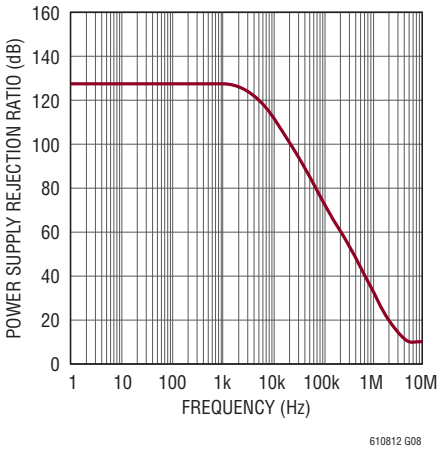


610912 G17

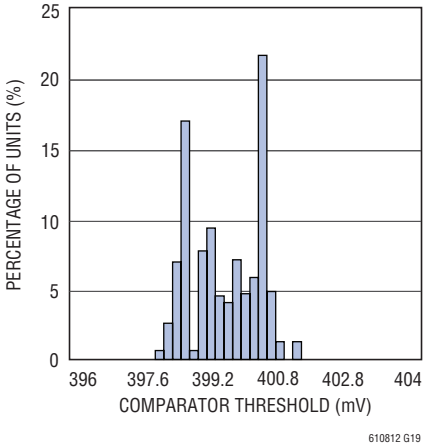
TYPICAL PERFORMANCE CHARACTERISTICS

Performance characteristics taken at T_A = 25°C, V^+ = 12V, V_{PULLUP} = V^+, V_{EN} = $V_{EN/\overline{RST}}$ = 2.7V, R_{IN} = 100Ω, R_{OUT} = R1 + R2 = 10k, gain = 100, R_C = 25.5k, C_L = C_{LC} = 2pF, unless otherwise noted. (See Figure 3)

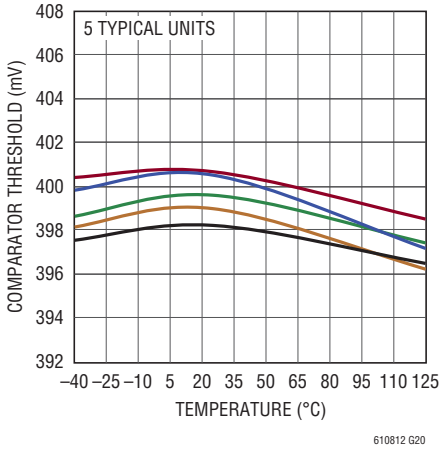
Power Supply Rejection Ratio vs Frequency



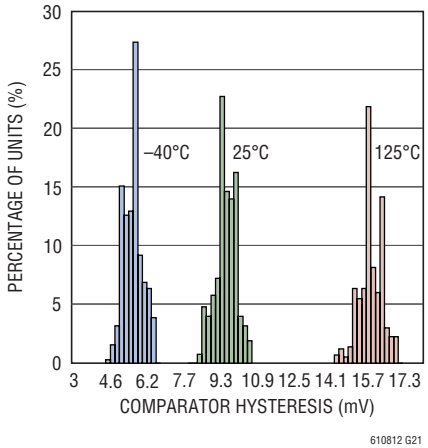
Comparator Threshold Distribution



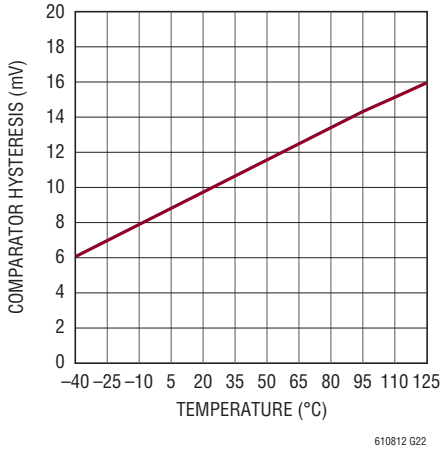
Comparator Threshold vs Temperature



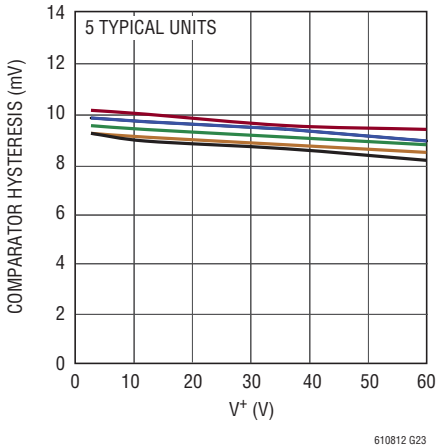
Hysteresis Distribution



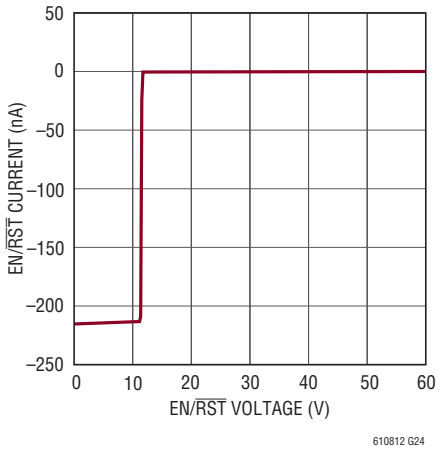
Hysteresis vs Temperature



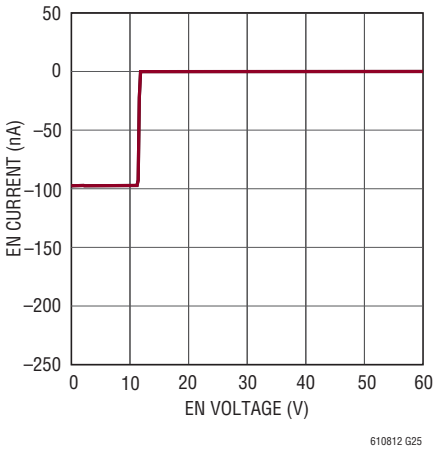
Hysteresis vs Supply Voltage



LT6108-1 EN/$\overline{RST}$ Current vs Voltage



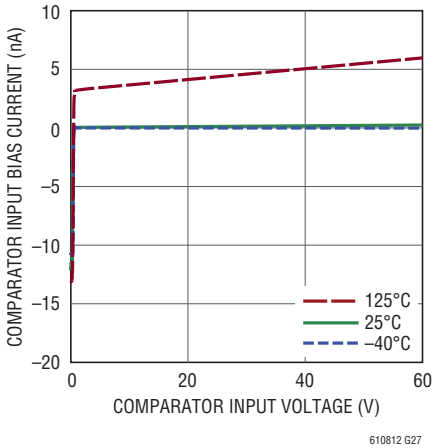
LT6108-2 EN Current vs Voltage



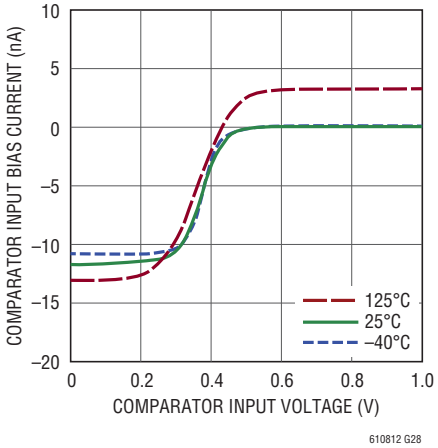
TYPICAL PERFORMANCE CHARACTERISTICS

Performance characteristics taken at T_A = 25°C, V^+ = 12V, V_{PULLUP} = V^+, V_{EN} = $V_{EN/\overline{RST}}$ = 2.7V, R_{IN} = 100Ω, R_{OUT} = R1 + R2 = 10k, gain = 100, R_C = 25.5k, C_L = C_{LC} = 2pF, unless otherwise noted. (See Figure 3)

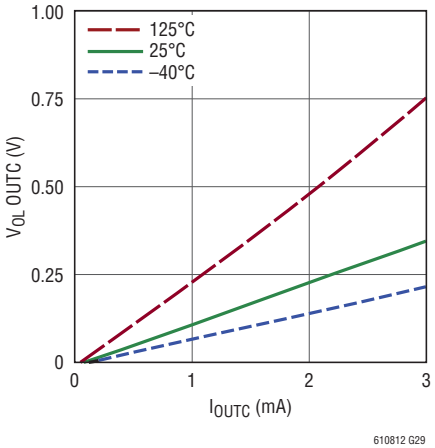
Comparator Input Bias Current vs Input Voltage



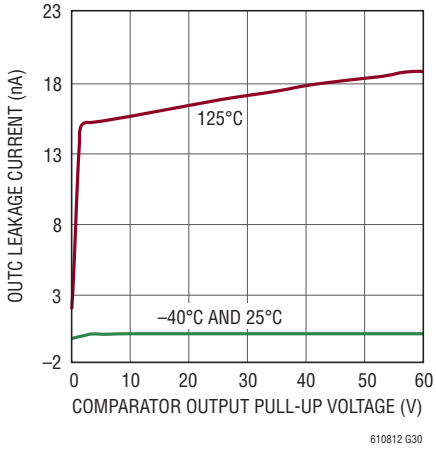
Comparator Input Bias Current vs Input Voltage



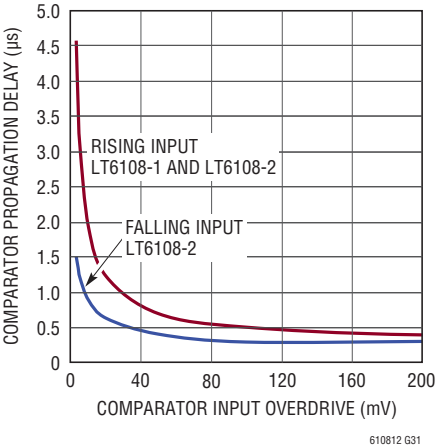
Comparator Output Low Voltage vs Output Sink Current



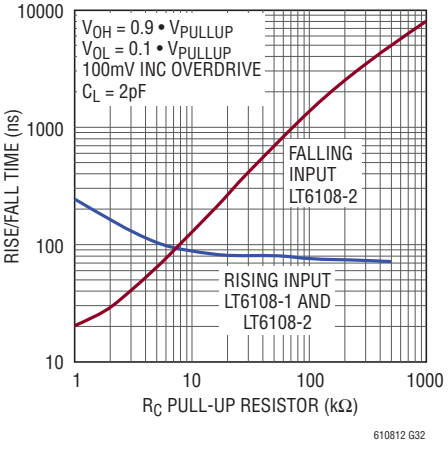
Comparator Output Leakage Current vs Pull-Up Voltage



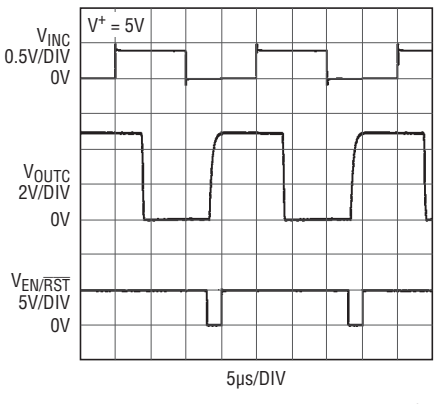
Comparator Propagation Delay vs Input Overdrive



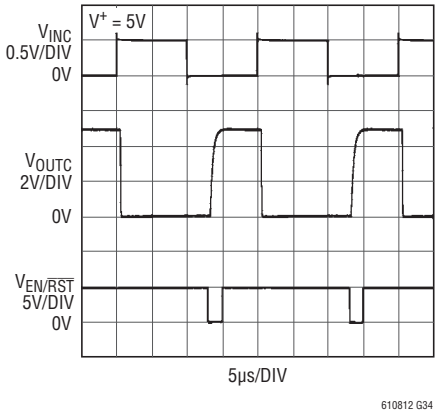
Comparator Rise/Fall Time vs Pull-Up Resistor



LT6108-1 Comparator Step Response (5mV INC Overdrive)



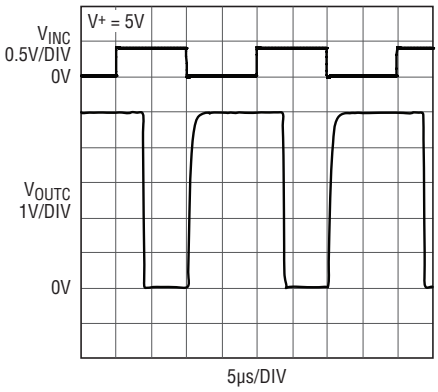
LT6108-1 Comparator Step Response (100mV INC Overdrive)



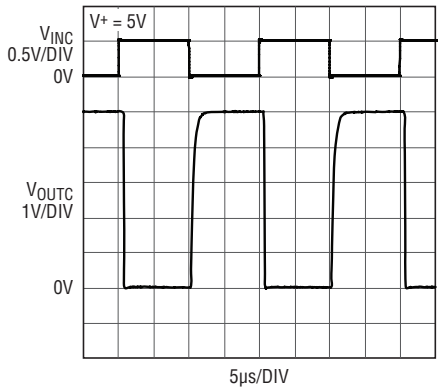
TYPICAL PERFORMANCE CHARACTERISTICS

Performance characteristics taken at T_A = 25°C, V^+ = 12V, V_{PULLUP} = V^+, V_{EN} = $V_{EN/\overline{RST}}$ = 2.7V, R_{IN} = 100Ω, R_{OUT} = R1 + R2 = 10k, gain = 100, R_C = 25.5k, C_L = C_{LC} = 2pF, unless otherwise noted. (See Figure 3)

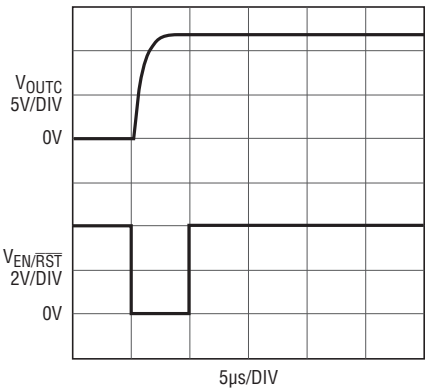
LT6108-2 Comparator Step Response (5mV INC Overdrive)



LT6108-2 Comparator Step Response (100mV INC Overdrive)



LT6108-1 Comparator Reset Response



PIN FUNCTIONS

SENSELO (Pin 1): Sense Amplifier Input. This pin must be tied to the load end of the sense resistor.

EN/$\overline{RST}$ (Pin 2, LT6108-1 Only): Enable and Latch Reset Input. When the EN/$\overline{RST}$ pin is pulled high the LT6108-1 is enabled. When the EN/$\overline{RST}$ pin is pulled low for longer than typically 40µs, the LT6108-1 will enter the shutdown mode. Pulsing this pin low for between 2µs and 15µs will reset the comparator of the LT6108-1.

EN (Pin 2, LT6108-2 Only): Enable Input. When the enable pin is pulled high the LT6108-2 is enabled. When the enable pin is pulled low for longer than typically 40µs, the LT6108-2 will enter the shutdown mode

OUTC (Pin 3): Open-Drain Comparator Output. Off-state voltage may be as high as 60V above V^-, regardless of V^+ used.

V^- (Pin 4): Negative Supply Pin. This pin is normally connected to ground.

INC (Pin 5): This is the inverting input of the comparator. The other comparator input is internally connected to the 400mV reference.

OUTA (Pin 6): Current Output of the Sense Amplifier. This pin will source a current that is equal to the sense voltage divided by the external gain setting resistor, R_{IN}.

V^+ (Pin 7): Positive Supply Pin. The V^+ pin can be connected directly to either side of the sense resistor, R_{SENSE}. When V^+ is tied to the load end of the sense resistor, the SENSEHI pin can go up to 0.2V above V^+. Supply current is drawn through this pin.

SENSEHI (Pin 8): Sense Amplifier Input. The internal sense amplifier will drive SENSEHI to the same potential as SENSELO. A resistor (typically R_{IN}) tied from supply to SENSEHI sets the output current, I_{OUT} = V_{SENSE}/R_{IN}, where V_{SENSE} is the voltage developed across R_{SENSE}.

Exposed Pad (Pin 9, DCB Package Only): V^-. The exposed pad may be left open or connected to device V^-. Connecting the exposed pad to a V^- plane will improve thermal management in high voltage applications. The exposed pad should not be used as the primary connection for V^-.

BLOCK DIAGRAMS

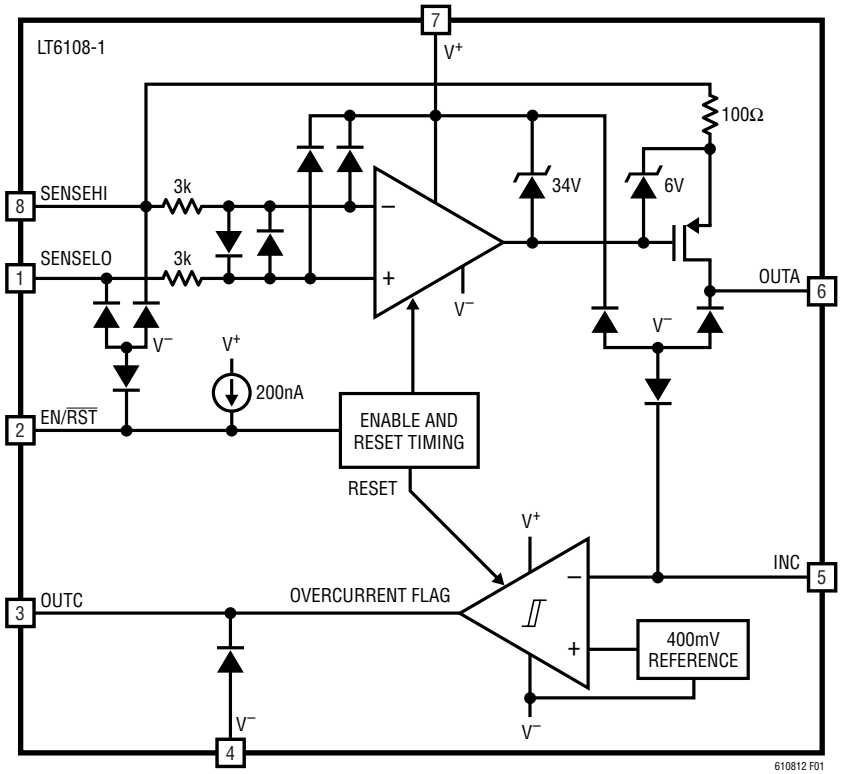


Figure 1. LT6108-1 Block Diagram (Latching Comparator)

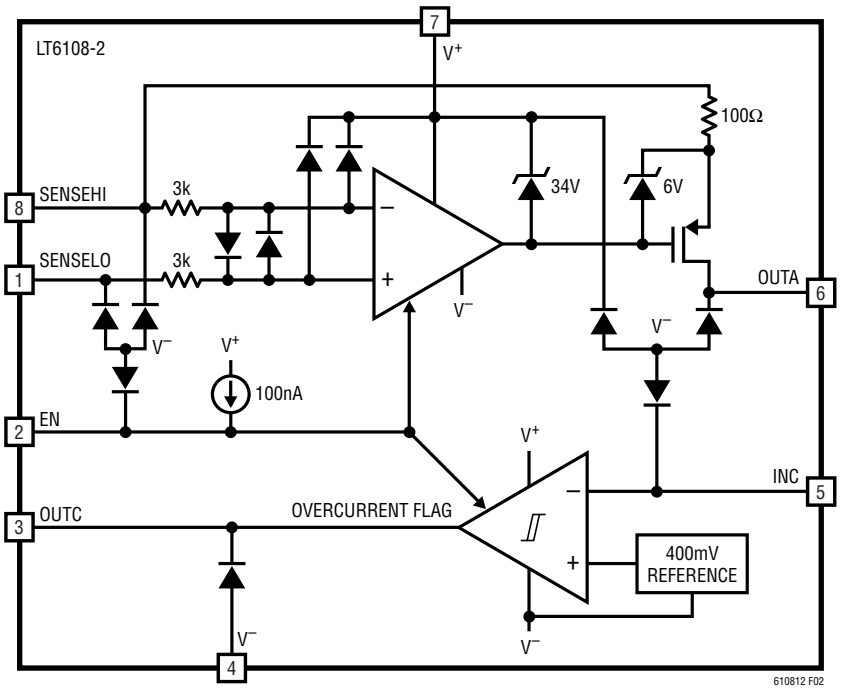


Figure 2. LT6108-2 Block Diagram (Non-Latching Comparator)

APPLICATIONS INFORMATION

The LT6108 high side current sense amplifier provides accurate monitoring of currents through an external sense resistor. The input sense voltage is level-shifted from the sensed power supply to a ground referenced output and is amplified by a user-selected gain to the output. The output voltage is directly proportional to the current flowing through the sense resistor.

The LT6108 comparator has a threshold set with a built-in 400mV precision reference and has 10mV of hysteresis. The open-drain output can be easily used to level shift to digital supplies.

Amplifier Theory of Operation

An internal sense amplifier loop forces SENSEHI to have the same potential as SENSELO as shown in Figure 3. Connecting an external resistor, R_{IN}, between SENSEHI and V_{SUPPLY} forces a potential, V_{SENSE}, across R_{IN}. A corresponding current, I_{OUTA}, equal to V_{SENSE}/R_{IN}, will flow through R_{IN}. The high impedance inputs of the sense amplifier do not load this current, so it will flow through an internal MOSFET to the output pin, OUTA.

The output current can be transformed back into a voltage by adding a resistor from OUTA to V^-(typically ground). The output voltage is then:

$$V_{OUT} = V^- + I_{OUTA} \bullet R_{OUT}$$

where R_{OUT} = R1 + R2 as shown in Figure 3.

Table 1. Example Gain Configurations

GAIN	R_{IN}	R_{OUT}	V_{SENSE} FOR V_{OUT} = 5V	I_{OUTA} AT V_{OUT} = 5V
20	499Ω	10k	250mV	500µA
50	200Ω	10k	100mV	500µA
100	100Ω	10k	50mV	500µA

Useful Equations

Input Voltage: $V_{SENSE} = I_{SENSE} \bullet R_{SENSE}$

Voltage Gain: $\frac{V_{OUT}}{V_{SENSE}} = \frac{R_{OUT}}{R_{IN}}$

Current Gain: $\frac{I_{OUTA}}{I_{SENSE}} = \frac{R_{SENSE}}{R_{IN}}$

Note that $V_{SENSE(MAX)}$ can be exceeded without damaging the amplifier, however, output accuracy will degrade as V_{SENSE} exceeds $V_{SENSE(MAX)}$, resulting in increased output current, I_{OUTA}.

Selection of External Current Sense Resistor

The external sense resistor, R_{SENSE}, has a significant effect on the function of a current sensing system and must be chosen with care.

First, the power dissipation in the resistor should be considered. The measured load current will cause power dissipation as well as a voltage drop in R_{SENSE}. As a result, the sense resistor should be as small as possible while still providing the input dynamic range required by the measurement. Note that the input dynamic range is the difference between the maximum input signal and the minimum accurately reproduced signal, and is limited primarily by input DC offset of the internal sense amplifier of the LT6108. To ensure the specified performance, R_{SENSE} should be small enough that V_{SENSE} does not exceed $V_{SENSE(MAX)}$ under peak load conditions. As an example, an application may require the maximum sense voltage be 100mV. If this application is expected to draw 2A at peak load, R_{SENSE} should be set to 50mΩ.

Once the maximum R_{SENSE} value is determined, the minimum sense resistor value will be set by the resolution or dynamic range required. The minimum signal that can be accurately represented by this sense amplifier is limited by the input offset. As an example, the LT6108 has a maximum input offset of 125µV. If the minimum current is 20mA, a sense resistor of 6.25mΩ will set V_{SENSE} to 125µV. This is the same value as the input offset. A larger sense resistor will reduce the error due to offset by increasing the sense voltage for a given load current. Choosing a 50mΩ R_{SENSE} will maximize the dynamic range and provide a system that has 100mV across the sense resistor at peak load (2A), while input offset causes an error equivalent to only 2.5mA of load current.

In the previous example, the peak dissipation in R_{SENSE} is 200mW. If a 5mΩ sense resistor is employed, then the effective current error is 25mA, while the peak sense voltage is reduced to 10mV at 2A, dissipating only 20mW.

APPLICATIONS INFORMATION

The low offset and corresponding large dynamic range of the LT6108 make it more flexible than other solutions in this respect. The 125µV maximum offset gives 72dB of dynamic range for a sense voltage that is limited to 500mV max.

Sense Resistor Connection

Kelvin connection of the SENSEHI and SENSELO inputs to the sense resistor should be used in all but the lowest power applications. Solder connections and PC board interconnections that carry high currents can cause significant error in measurement due to their relatively large resistances. One 10mm × 10mm square trace of 1oz copper is approximately 0.5mΩ. A 1mV error can be caused by as little as 2A flowing through this small interconnect. This will cause a 1% error for a full-scale V_{SENSE} of 100mV. A 10A load current in the same interconnect will cause a 5% error for the same 100mV signal. By isolating the sense traces from the high current paths, this error can be reduced by orders of magnitude. A sense resistor with integrated Kelvin sense terminals will give the best results. Figure 3 illustrates the recommended method for connecting the SENSEHI and SENSELO pins to the sense resistor.

Selection of External Input Gain Resistor, R_{IN}

R_{IN} should be chosen to allow the required speed and resolution while limiting the output current to 1mA. The maximum value for R_{IN} is 1k to maintain good loop stability. For a given V_{SENSE}, larger values of R_{IN} will lower power dissipation in the LT6108 due to the reduction in I_{OUT} while smaller values of R_{IN} will result in faster response time due to the increase in I_{OUT}. If low sense currents must be resolved accurately in a system that has a very wide dynamic range, a smaller R_{IN} may be used if the maximum I_{OUTA} current is limited in another way, such as with a Schottky diode across R_{SENSE} (Figure 4). This will reduce the high current measurement accuracy by limiting the result, while increasing the low current measurement resolution.

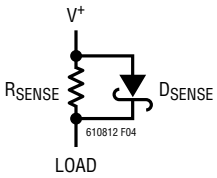


Figure 4. Shunt Diode Limits Maximum Input Voltage to Allow Better Low Input Resolution Without Overranging

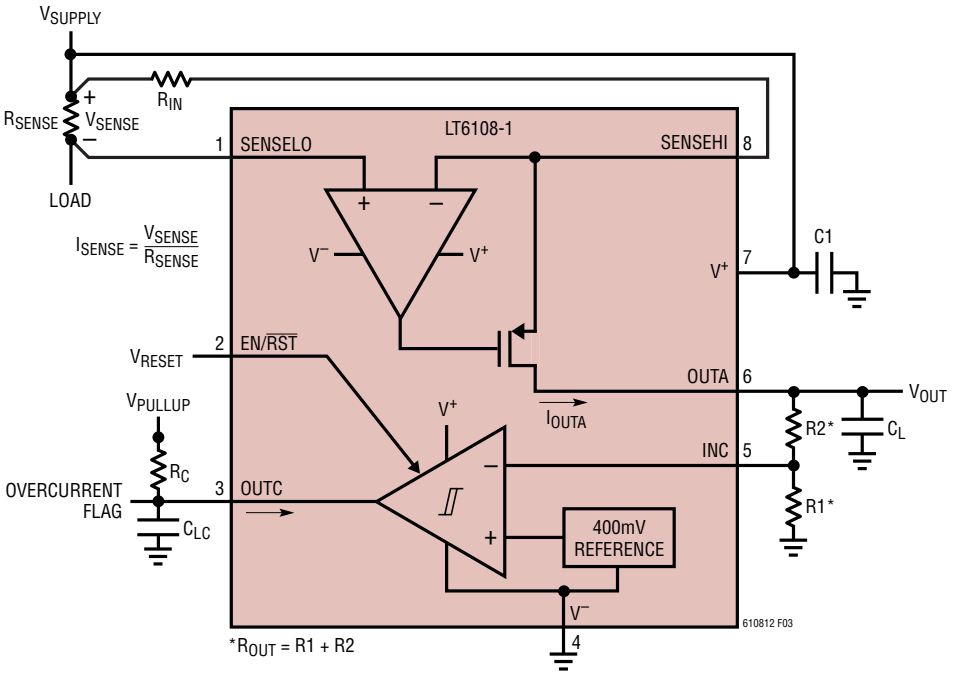


Figure 3. LT6108-1 Typical Connection

APPLICATIONS INFORMATION

This approach can be helpful in cases where occasional bursts of high currents can be ignored.

Care should be taken when designing the board layout for R_{IN}, especially for small R_{IN} values. All trace and interconnect resistances will increase the effective R_{IN} value, causing a gain error.

The power dissipated in the sense resistor can create a thermal gradient across a printed circuit board and consequently a gain error if R_{IN} and R_{OUT} are placed such that they operate at different temperatures. If significant power is being dissipated in the sense resistor then care should be taken to place R_{IN} and R_{OUT} such that the gain error due to the thermal gradient is minimized.

Selection of External Output Gain Resistor, R_{OUT}

The output resistor, R_{OUT}, determines how the output current is converted to voltage. V_{OUT} is simply $I_{OUTA} \bullet R_{OUT}$. Typically, R_{OUT} is a combination of resistors configured as a resistor divider which has a voltage tap going to the comparator input to set the comparator threshold.

In choosing an output resistor, the maximum output voltage must first be considered. If the subsequent circuit is a buffer or ADC with limited input range, then R_{OUT} must be chosen so that $I_{OUTA(MAX)} \bullet R_{OUT}$ is less than the allowed maximum input range of this circuit.

In addition, the output impedance is determined by R_{OUT}. If another circuit is being driven, then the input impedance of that circuit must be considered. If the subsequent circuit has high enough input impedance, then almost any useful output impedance will be acceptable. However, if the subsequent circuit has relatively low input impedance, or draws spikes of current such as an ADC load, then a lower output impedance may be required to preserve the accuracy of the output. More information can be found in the Output Filtering section. As an example, if the input impedance of the driven circuit, $R_{IN(DRIVEN)}$, is 100 times R_{OUT}, then the accuracy of V_{OUT} will be reduced by 1% since:

$$V_{OUT} = I_{OUTA} \bullet \frac{R_{OUT} \bullet R_{IN(DRIVEN)}}{R_{OUT} + R_{IN(DRIVEN)}}$$

$$= I_{OUTA} \bullet R_{OUT} \bullet \frac{100}{101} = 0.99 \bullet I_{OUTA} \bullet R_{OUT}$$

Amplifier Error Sources

The current sense system uses an amplifier and resistors to apply gain and level-shift the result. Consequently, the output is dependent on the characteristics of the amplifier, such as gain error and input offset, as well as the matching of the external resistors.

Ideally, the circuit output is:

$$V_{OUT} = V_{SENSE} \bullet \frac{R_{OUT}}{R_{IN}};\ V_{SENSE} = R_{SENSE} \bullet I_{SENSE}$$

In this case, the only error is due to external resistor mismatch, which provides an error in gain only. However, offset voltage, input bias current and finite gain in the amplifier can cause additional errors:

Output Voltage Error, $\Delta V_{OUT(VOS)}$, Due to the Amplifier DC Offset Voltage, V_{OS}

$$\Delta V_{OUT(VOS)} = V_{OS} \bullet \frac{R_{OUT}}{R_{IN}}$$

The DC offset voltage of the amplifier adds directly to the value of the sense voltage, V_{SENSE}. As V_{SENSE} is increased, accuracy improves. This is the dominant error of the system and it limits the available dynamic range.

Output Voltage Error, $\Delta V_{OUT(IBIAS)}$, Due to the Bias Currents I_B^+ and I_B^-

The amplifier bias current I_B^+ flows into the SENSELO pin while I_B^- flows into the SENSEHI pin. The error due to I_B is the following:

$$\Delta V_{OUT(IBIAS)} = R_{OUT} \left(I_B^+ \bullet \frac{R_{SENSE}}{R_{IN}} - I_B^- \right)$$

Since $I_B^+ \approx I_B^- = I_{BIAS}$, if $R_{SENSE} << R_{IN}$ then,

$$\Delta V_{OUT(IBIAS)} = -R_{OUT}\ (I_{BIAS})$$

It is useful to refer the error to the input:

$$\Delta V_{VIN(IBIAS)} = -R_{IN}\ (I_{BIAS})$$

For instance, if I_{BIAS} is 100nA and R_{IN} is 1k, the input referred error is 100µV. This error becomes less significant as the value of R_{IN} decreases. The bias current error can

APPLICATIONS INFORMATION

be reduced if an external resistor, R_{IN}^+, is connected as shown in Figure 5, the error is then reduced to:

$$V_{OUT(IBIAS)} = \pm R_{OUT} \bullet I_{OS};\ I_{OS} = I_B^+ - I_B^-$$

Minimizing low current errors will maximize the dynamic range of the circuit.

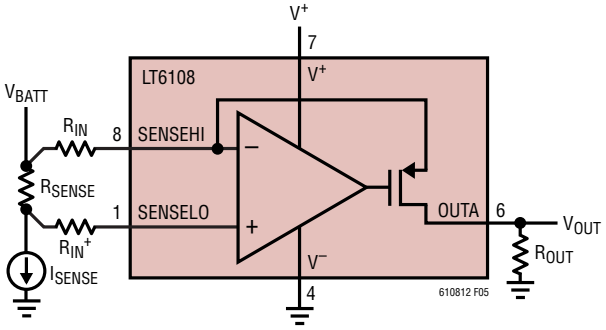


Figure 5. R_{IN}^+ Reduces Error Due to I_B

Output Voltage Error, $\Delta V_{OUT(GAIN\ ERROR)}$, Due to External Resistors

The LT6108 exhibits a very low gain error. As a result, the gain error is only significant when low tolerance resistors are used to set the gain. Note the gain error is systematically negative. For instance, if 0.1% resistors are used for R_{IN} and R_{OUT} then the resulting worst-case gain error is –0.4% with R_{IN} = 100Ω. Figure 6 is a graph of the maximum gain error which can be expected versus the external resistor tolerance.

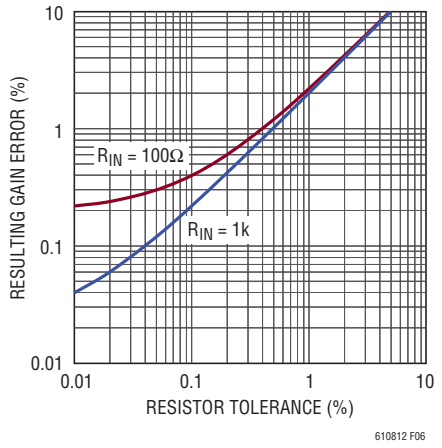


Figure 6. Gain Error vs Resistor Tolerance

Output Current Limitations Due to Power Dissipation

The LT6108 can deliver a continuous current of 1mA to the OUTA pin. This current flows through R_{IN} and enters the current sense amplifier via the SENSEHI pin. The power dissipated in the LT6108 due to the output signal is:

$$P_{OUT} = (V_{SENSEHI} - V_{OUTA}) \bullet I_{OUTA}$$

Since $V_{SENSEHI} \approx V^+$, $P_{OUTA} \approx (V^+ - V_{OUTA}) \bullet I_{OUTA}$

There is also power dissipated due to the quiescent power supply current:

$$P_S = I_S \bullet V^+$$

The comparator output current flows into the comparator output pin and out of the V^- pin. The power dissipated in the LT6108 due to the comparator is often insignificant and can be calculated as follows:

$$P_{OUTC} = (V_{OUTC} - V^-) \bullet I_{OUTC}$$

The total power dissipated is the sum of these dissipations:

$$P_{TOTAL} = P_{OUTA} + P_{OUTC} + P_S$$

At maximum supply and maximum output currents, the total power dissipation can exceed 150mW. This will cause significant heating of the LT6108 die. In order to prevent damage to the LT6108, the maximum expected dissipation in each application should be calculated. This number can be multiplied by the θ_{JA} value, 163°C/W for the MS8 package or 64°C/W for the DFN, to find the maximum expected die temperature. Proper heat sinking and thermal relief should be used to ensure that the die temperature does not exceed the maximum rating.

Output Filtering

The AC output voltage, V_{OUT}, is simply $I_{OUTA} \bullet Z_{OUT}$. This makes filtering straightforward. Any circuit may be used which generates the required Z_{OUT} to get the desired filter response. For example, a capacitor in parallel with R_{OUT} will give a lowpass response. This will reduce noise at the output, and may also be useful as a charge reservoir to keep the output steady while driving a switching circuit

APPLICATIONS INFORMATION

such as a MUX or ADC. This output capacitor in parallel with R_{OUT} will create an output pole at:

$$f_{-3dB} = \frac{1}{2 \bullet \pi \bullet R_{OUT} \bullet C_L}$$

SENSELO, SENSEHI Range

The difference between V_{BATT} (see Figure 7) and V^+, as well as the maximum value of V_{SENSE}, must be considered to ensure that the SENSELO pin doesn't exceed the range listed in the Electrical Characteristics table. The SENSELO and SENSEHI pins of the LT6108 can function from 0.2V above the positive supply to 33V below it. These operating voltages are limited by internal diode clamps shown in Figures 1 and 2. On supplies less than 35.5V, the lower range is limited by V^- + 2.5V. This allows the monitored supply, V_{BATT}, to be separate from the LT6108 positive supply as shown in Figure 7. Figure 8 shows the range of operating voltages for the SENSELO and SENSEHI inputs, for different supply voltage inputs (V^+). The SENSELO and SENSEHI range has been designed to allow the LT6108 to monitor its own supply current (in addition to the load), as long as V_{SENSE} is less than 200mV. This is shown in Figure 9.

Minimum Output Voltage

The output of the LT6108 current sense amplifier can produce a non-zero output voltage when the sense voltage is zero. This is a result of the sense amplifier V_{OS} being forced across R_{IN} as discussed in the Output Voltage Error, $\Delta V_{OUT(VOS)}$ section. Figure 10 shows the effect of the input offset voltage on the transfer function for parts at the V_{OS} limits. With a negative offset voltage, zero input

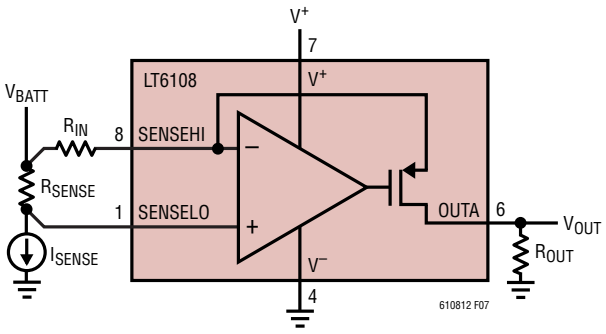


Figure 7. V^+ Powered Separately from Load Supply (V_{BATT})

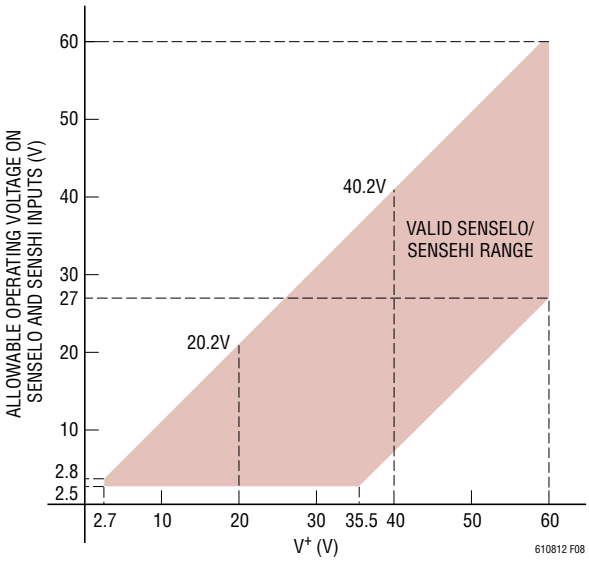


Figure 8. Allowable SENSELO, SENSEHI Voltage Range

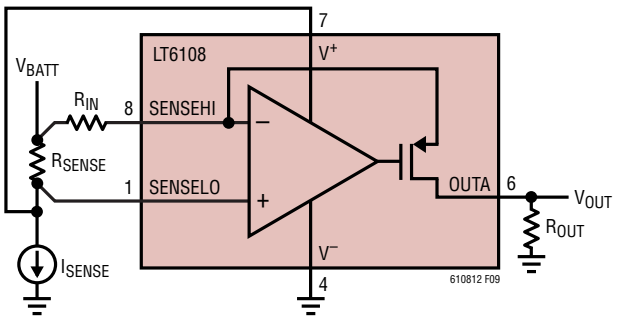


Figure 9. LT6108 Supply Current Monitored with Load

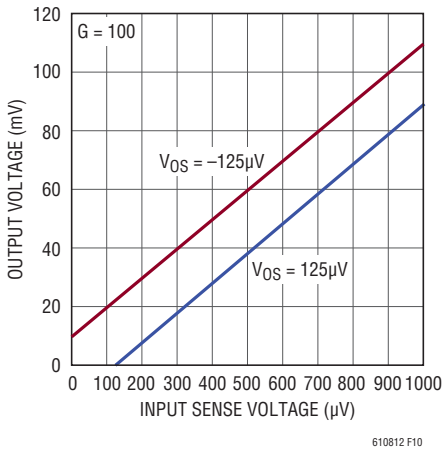


Figure 10. Amplifier Output Voltage vs Input Sense Voltage

APPLICATIONS INFORMATION

sense voltage produces an output voltage. With a positive offset voltage, the output voltage is zero until the input sense voltage exceeds the input offset voltage. Neglecting V_{OS}, the output circuit is not limited by saturation of pull-down circuitry and can reach 0V.

Response Time

The LT6108 amplifier is designed to exhibit fast response to inputs for the purpose of circuit protection or current monitoring. This response time will be affected by the external components in two ways, delay and speed.

If the output current is very low and an input transient occurs, there may be an increased delay before the output voltage begins to change. The Typical Performance Characteristics show that this delay is short and it can be improved by increasing the minimum output current, either by increasing R_{SENSE} or decreasing R_{IN}. Note that the Typical Performance Characteristics are labeled with respect to the initial sense voltage.

The speed is also affected by the external components. Using a larger R_{OUT} will decrease the response time, since $V_{OUT} = I_{OUTA} \bullet Z_{OUT}$ where Z_{OUT} is the parallel combination of R_{OUT} and any parasitic and/or load capacitance. Note that reducing R_{IN} or increasing R_{OUT} will both have the effect of increasing the voltage gain of the circuit. If the output capacitance is limiting the speed of the system, R_{IN} and R_{OUT} can be decreased together in order to maintain the desired gain and provide more current to charge the output capacitance.

The response time of the comparator is the sum of the propagation delay and the fall time. The propagation delay is a function of the overdrive voltage on the input of the comparator. A larger overdrive will result in a lower propagation delay. This helps achieve a fast system response time to fault events. The fall time is affected by the load on the output of the comparator as well as the pull-up voltage.

The LT6108 amplifier has a typical response time of 500ns and the comparators have a typical response time of 500ns. When configured as a system, the amplifier output drives the comparator input causing a total system response time which is typically greater than that implied by the individually specified response times. This is due to the overdrive on the comparator input being determined by the speed of the amplifier output.

Internal Reference and Comparator

The integrated precision reference and comparator combined with the high precision current sense allow for rapid and easy detection of abnormal load currents. This is often critical in systems that require high levels of safety and reliability. The LT6108-1 comparator is optimized for fault detection and is designed with a latching output. The latching output prevents faults from clearing themselves and requires a separate system or user to reset the output. In applications where the comparator output can intervene and disconnect loads from the supply, a latched output is required to avoid oscillation. The latching output is also useful for detecting problems that are intermittent. The comparator output on the LT6108-2 is non-latching and can be used in applications where a latching output is not desired.

The comparator has one input available externally. The other comparator input is connected internally to the 400mV precision reference. The input threshold (the voltage which causes the output to transition from high to low) is designed to be equal to that of the reference. The reference voltage is established with respect to the device V^- connection.

Comparator Input

The comparator input can swing from V^- to 60V regardless of the supply voltage used. The input current for inputs well above the threshold is just a few pAs. With decreasing input voltage, a small bias current begins to be drawn out of the input near the threshold, reaching 50nA max when at ground potential. Note that this change in input bias current can cause a small nonlinearity in the OUTA transfer function if the comparator input is coupled to the amplifier output with a voltage divider. For example, if the maximum comparator input current is 50nA, and the resistance seen looking out of the comparator input is 1k, then a change in output voltage of 50µV will be seen on the analog output when the comparator input voltage passes through its threshold.

APPLICATIONS INFORMATION

Setting Comparator Threshold

The comparator has an internal 400mV precision reference. In order to set the trip point of the LT6108 comparator as configured in Figure 11, the input sense voltage at which the comparator will trip, $V_{SENSE(TRIP)}$ must be calculated:

$$V_{SENSE(TRIP)} = I_{SENSE(TRIP)} \bullet R_{SENSE}$$

The selection of R_{IN} is discussed in the Selection of External Input Gain Resistor R_{IN} section. Once R_{IN} is selected, R_{OUT} can be calculated:

$$R_{OUT} = R_{IN} \frac{400mV}{V_{SENSE(TRIP)}}$$

Since the amplifier output is connected directly to the comparator input, the gain from V_{SENSE} to V_{OUT} is:

$$A_V = \frac{400mV}{V_{SENSE(TRIP)}}$$

As shown in Figure 12, R2 can be used to increase the gain from V_{SENSE} to V_{OUT} without changing $V_{SENSE(TRIP)}$. As before, R1 can be easily calculated:

$$R1 = R_{IN} \frac{400mV}{V_{SENSE(TRIP)}}$$

The gain is now:

$$A_V = \frac{R1+R2}{R_{IN}}$$

This gain equation can be easily solved for R2:

$$R2 = A_V \bullet R_{IN} - R1$$

If the configuration of Figure 11 gives too much gain, R2 can be used to reduce the gain without changing $V_{SENSE(TRIP)}$ as shown in Figure 13. A_V can be easily calculated:

$$A_V = \frac{R1}{R_{IN}}$$

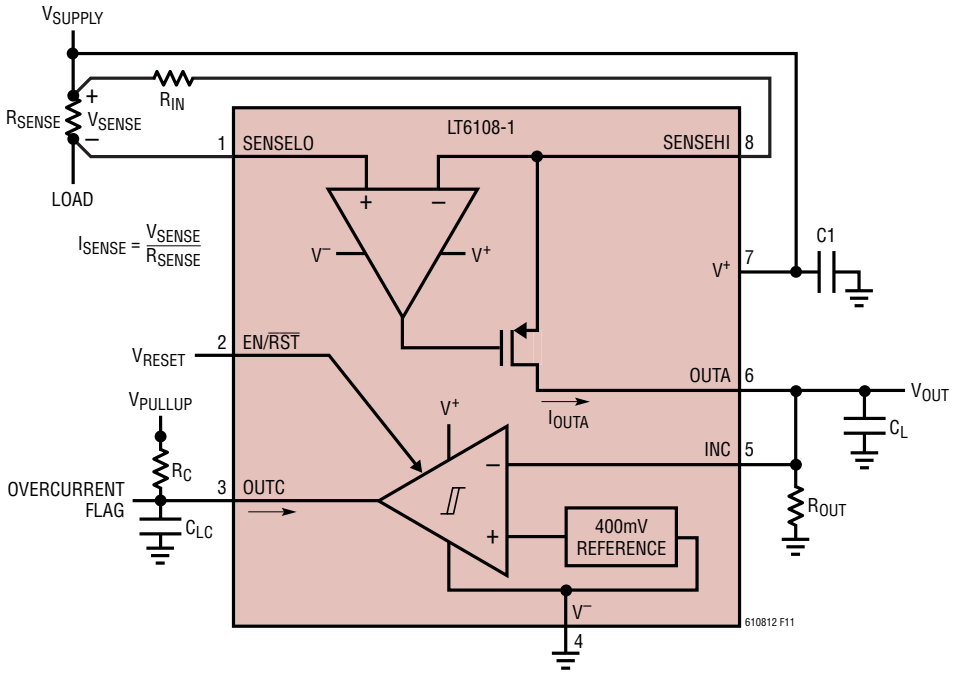


Figure 11. Basic Comparator Configuration

APPLICATIONS INFORMATION

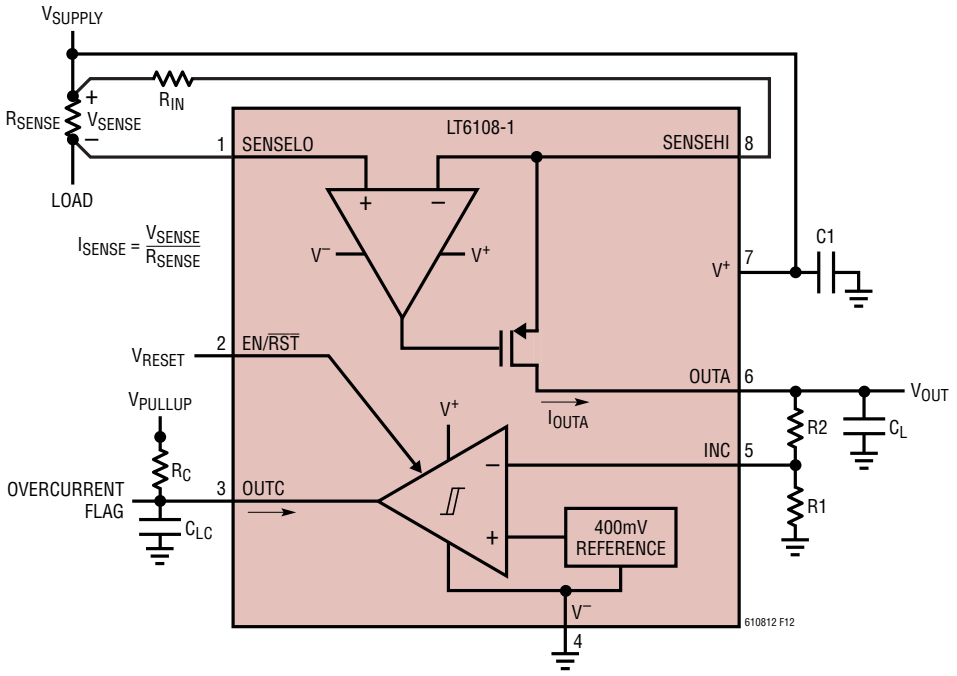


Figure 12: Comparator Configuration with Increased A_V

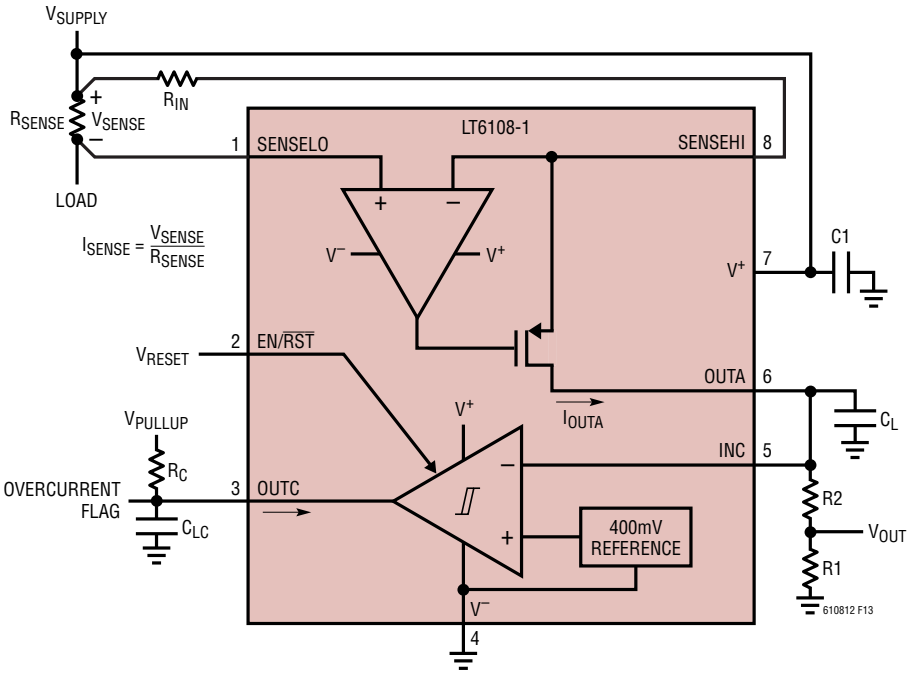


Figure 13: Comparator Configuration with Reduced A_V

APPLICATIONS INFORMATION

This gain equation can be easily solved for R1:

$$R1 = A_V \bullet R_{IN}$$

The value of R2 can be calculated:

$$R2 = \frac{400mV \bullet R_{IN} - V_{SENSE(TRIP)} \bullet R1}{V_{SENSE(TRIP)}}$$

Hysteresis

The comparator has a typical built-in hysteresis of 10mV to simplify design, ensure stable operation in the presence of noise at the input, and to reject supply noise that might be induced by state change load transients. The hysteresis is designed such that the threshold voltage is altered when the output is transitioning from low to high as is shown in Figure 14.

External positive feedback circuitry can be employed to increase the effective hysteresis if desired, but such circuitry will have an effect on both the rising and falling input thresholds, V_{TH} (the actual internal threshold remains unaffected).

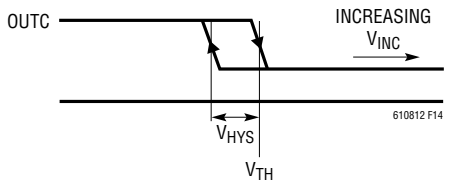


Figure 14. Comparator Output Transfer Characteristics

Figure 15 shows how to add additional hysteresis to the comparator.

R5 can be calculated from the amplifier output current which is required to cause the comparator output to trip, I_{OVER}.

$$R5 = \frac{400mV}{I_{OVER}}, \text{ Assuming } (R1+R2) >> R5$$

To ensure (R1 + R2) >> R5, R1 should be chosen such that R1 >> R5 so that V_{OUTA} does not change significantly when the comparator trips.

R3 should be chosen to allow sufficient V_{OL} and comparator output rise time due to capacitive loading.

R2 can be calculated:

$$R2 = R1 \bullet \left(\frac{V_{DD} - 390mV}{V_{HYS(EXTRA)}} \right)$$

Note that the hysteresis being added, $V_{HYS(EXTRA)}$, is in addition to the typical 10mV of built-in hysteresis. For very large values of R2 PCB related leakage may become an issue. A tee network can be implemented to reduce the required resistor values.

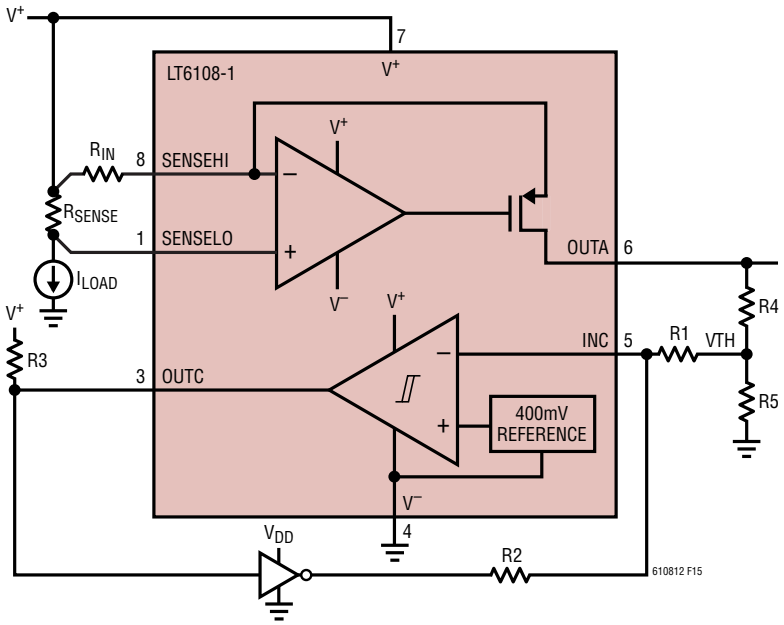


Figure 15. Inverting Comparator with Added Hysteresis

APPLICATIONS INFORMATION

The approximate total hysteresis is:

$$V_{HYS} = 10mV + R1 \bullet \left(\frac{V_{DD} - 390mV}{R2} \right)$$

For example, to achieve I_{OVER} = 900µA with 50mV of total hysteresis, R5 = 442Ω. Choosing R1 = 4.42k, R3 = 10k and V_{DD} = 5V results in R2 = 513k.

The analog output voltage will also be affected when the comparator trips due to the current injected into R5 by the positive feedback. Because of this, it is desirable to have (R1 + R2) >> R5. The maximum V_{OUTA} error caused by this can be calculated as:

$$\Delta V_{OUTA} = V_{DD} \bullet \left(\frac{R5}{R1+R2+R5} \right)$$

In the previous example, this is an error of 4.3mV at the output of the amplifier or 43µV at the input of the amplifier assuming a gain of 100.

When using the comparator with its input decoupled from the output of the amplifier it may be driven directly by a voltage source. It is useful to know the threshold voltage equations with additional hysteresis. The input rising edge threshold which causes the output to transition from high to low is:

$$V_{TH(R)} = 400mV \bullet \left(1 + \frac{R1}{R2} \right)$$

The input falling edge threshold which causes the output to transition from low to high is:

$$V_{TH(F)} = 390mV \left(1 + \frac{R1}{R2} \right) - V_{DD} \left(\frac{R1}{R2} \right)$$

Comparator Output

The comparator output can maintain a logic-low level of 150mV while sinking 500µA. The output can sink higher currents at elevated V_{OL} levels as shown in the Typical Performance Characteristics. Load currents are conducted to the V^- pin. The output off-state voltage may range between 0V and 60V with respect to V^-, regardless of the supply voltage used.

EN/$\overline{RST}$ Pin (LT6108-1 Only)

The EN/$\overline{RST}$ pin performs the two functions of resetting the latch on the comparator as well as shutting down the LT6108-1. When this pin is pulled high the LT6108-1 is enabled. After powering on the LT6108-1, the comparator must be reset in order to guarantee a valid state at its output.

Applying a pulse to the EN/$\overline{RST}$ pin will reset the comparator from its tripped low state as long as the input on the comparator is below the threshold and hysteresis. For example, if V_{INC} is pulled higher than 400mV and latches the comparator, a reset pulse will not reset that comparator unless its input is held below the threshold by a voltage greater than the 10mV typical hysteresis. The comparator output typically unlatches in 0.5µs with 2pF of capacitive load. Increased capacitive loading on the comparator output will cause an increased unlatch time.

Figure 16 shows the reset functionality of the EN/$\overline{RST}$ pin. The width of the pulse applied to reset the comparator must be greater than $t_{RPW(MIN)}$ (2µs) but less than $t_{RPW(MAX)}$ (15µs). Applying a pulse that is longer than 40µs typically (or tying the pin low) will cause the part to enter shutdown. Once the part has entered shutdown, the supply current will be reduced to 3µA typically and the amplifier, comparator and reference will cease to function until the EN/$\overline{RST}$ pin is transitioned high. When the part is disabled, both the amplifier and comparator outputs are high impedance.

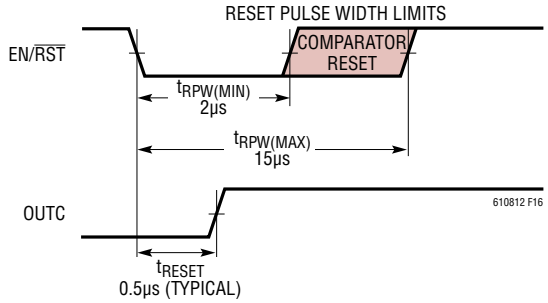


Figure 16. Comparator Reset Functionality

When the EN/$\overline{RST}$ pin is transitioned from low to high to enable the part, the amplifier output PMOS can turn on momentarily causing typically 1mA of current to flow into the SENSEHI pin and out of the OUTA pin. Once the amplifier is fully on, the output will go to the correct

APPLICATIONS INFORMATION

current. Figure 17 shows this behavior and the impact it has on V_{OUTA}. Circuitry connected to OUTA can be protected from these transients by using an external diode to clamp V_{OUTA}, or a capacitor to filter V_{OUTA}.

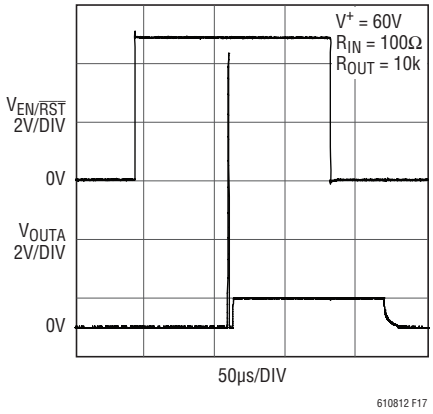


Figure 17. Amplifier Enable Response

EN Pin (LT6108-2)

When this pin is pulled high, the LT6108-2 is enabled. When the enable pin is pulled low for longer than 40µs typically, the LT6108-2 will enter the shutdown mode.

Power Up

After powering on the LT6108-1, the comparator must be reset in order to guarantee a valid state at its output. Fast supply ramps may cause a supply current transient during start-up as shown in the Typical Performance Characteristics. This current can be lowered by reducing the edge speed of the supply.

Reverse-Supply Protection

The LT6108 is not protected internally from external reversal of supply polarity. To prevent damage that may occur during this condition, a Schottky diode should be added in series with V^- (Figure 18). This will limit the reverse current through the LT6108. Note that this diode will limit the low voltage operation of the LT6108 by effectively reducing the supply voltage to the part by V_D.

Also note that the comparator reference, comparator output and EN/$\overline{RST}$ input are referenced to the V^- pin. In order to preserve the precision of the reference and to avoid driving the comparator inputs below V^-, R2 must connect to the V^- pin. This will shift the amplifier output voltage up by V_D. V_{OUTA} can be accurately measured

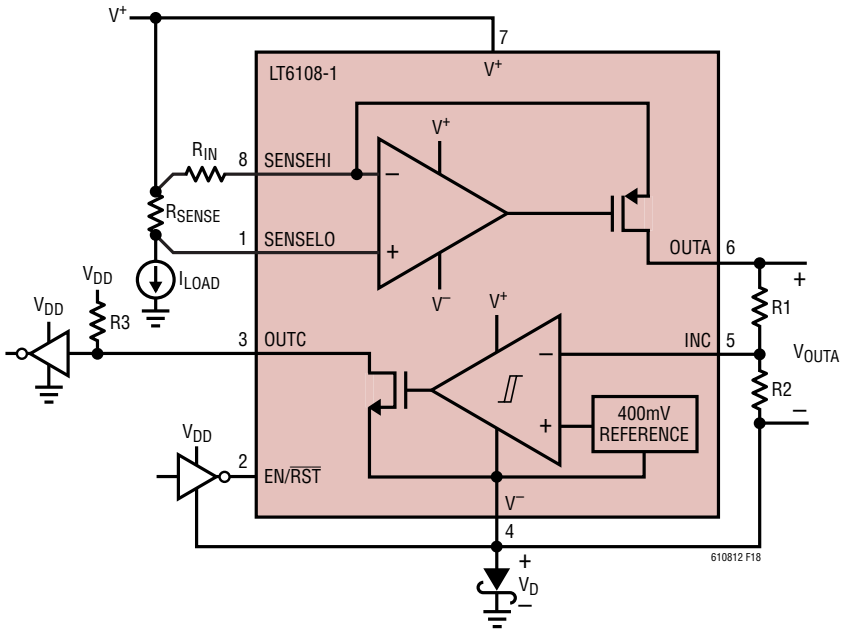


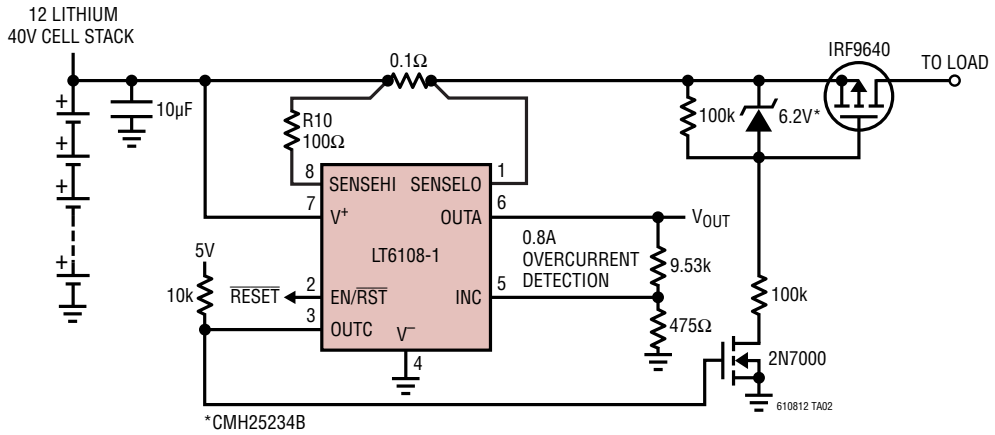
Figure 18. Schottky Prevents Damage During Supply Reversal

APPLICATIONS INFORMATION

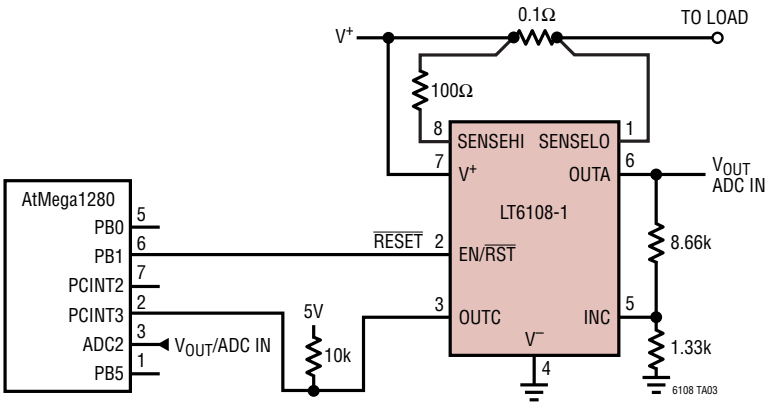
differentially across R1 and R2. The comparator output low voltage will also be shifted up by V_D. The EN/$\overline{RST}$ pin threshold is referenced to the V^- pin. In order to provide valid input levels to the LT6108 and avoid driving EN/$\overline{RST}$ below V^- the negative supply of the driving circuit should be tied to V^- of the LT6108.

TYPICAL APPLICATIONS

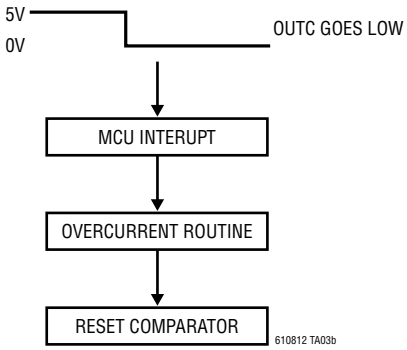
Overcurrent Battery Fault Protection



MCU Interfacing with Hardware Interrupts



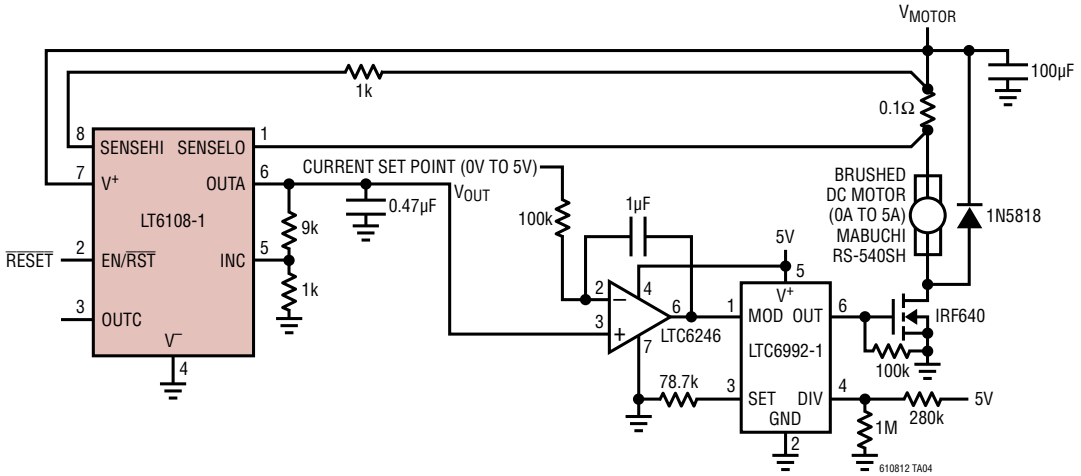
Example:



The comparator is set to have a 300mA overcurrent threshold. The MCU will receive the comparator output as a hardware interrupt and immediately run an appropriate fault routine.

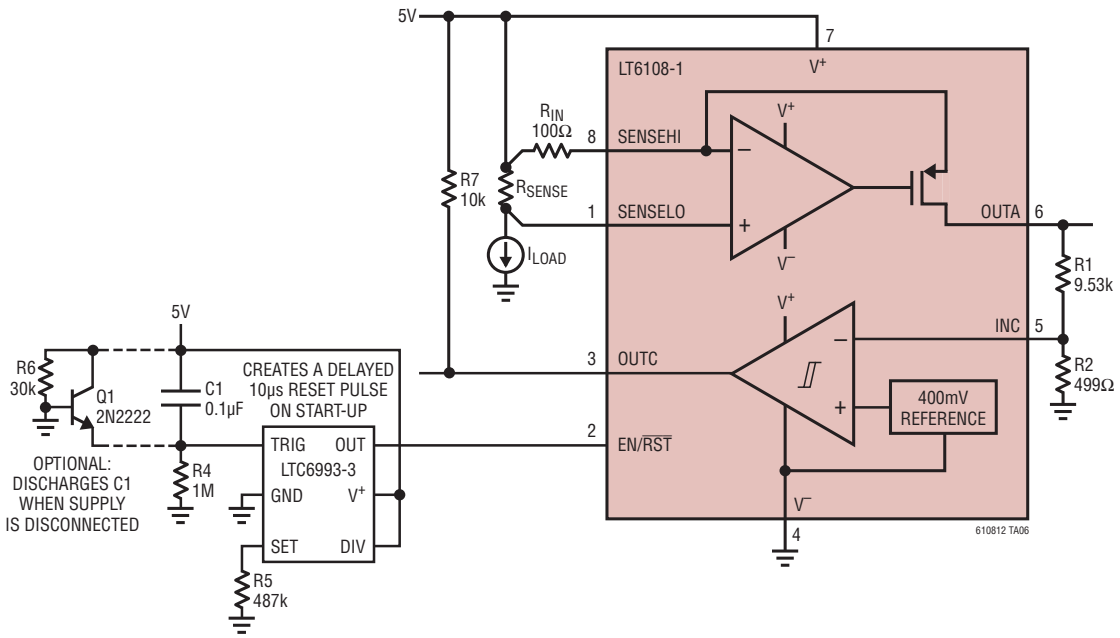
TYPICAL APPLICATIONS

Simplified DC Motor Torque Control



The figure above shows a simplified DC motor control circuit. The circuit controls motor current, which is proportional to motor torque; the LT6108 is used to provide current feedback to an integrator that servos the motor current to the current set point. The LTC®6992 is used to convert the output of the difference amp to the motors PWM control signal.

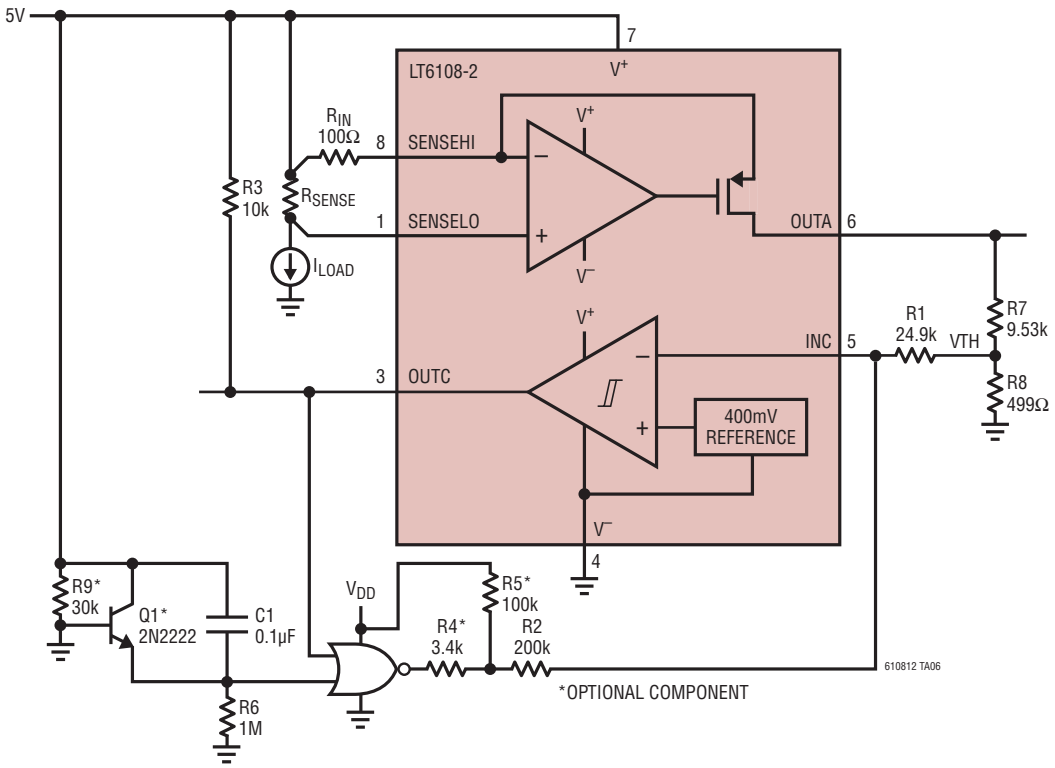
Power-On Reset or Disconnect Using TimerBlox® Circuit



The LTC6993-3 provides a 10µs reset pulse to the LT6108-1. The reset pulse is delayed by R4 and C1 whose time constant must be greater than 10ms and longer than the supply turn-on time. Optional components R6 and Q1 discharge capacitor C1 when the supply and/or ground are disconnected. This ensures that when the power supply and/or ground are restored, capacitor C1 can fully recharge and trigger the LTC6993-3 to produce another comparator reset pulse. These optional components are particularly useful if the power and/or ground connections are intermittent, as can occur when PCB are plugged into a connector.

TYPICAL APPLICATIONS

LT6108-2 with External Latch and Power-On Reset or Disconnect



An external latch is implemented with positive feedback. R6 and C1 provide a reset pulse on power-up. The time constant formed by R6 and C1 should be set slower than that of the supply. Optional components R9 and Q1 discharge capacitor C1 when the supply and/or ground are disconnected. This ensures that when the power supply and/or ground are restored, capacitor C1 can fully recharge. While C1 is charging, the NOR gate output is low, ensuring that the comparator powers up in the correct state. These optional components are particularly useful if the power and/or ground connections are intermittent, as can occur when PCB are plugged into a connector. R4 and R5 are optional and minimize the movement of the rising input threshold voltage.

The input rising edge threshold which causes the output to transition from high to low is:

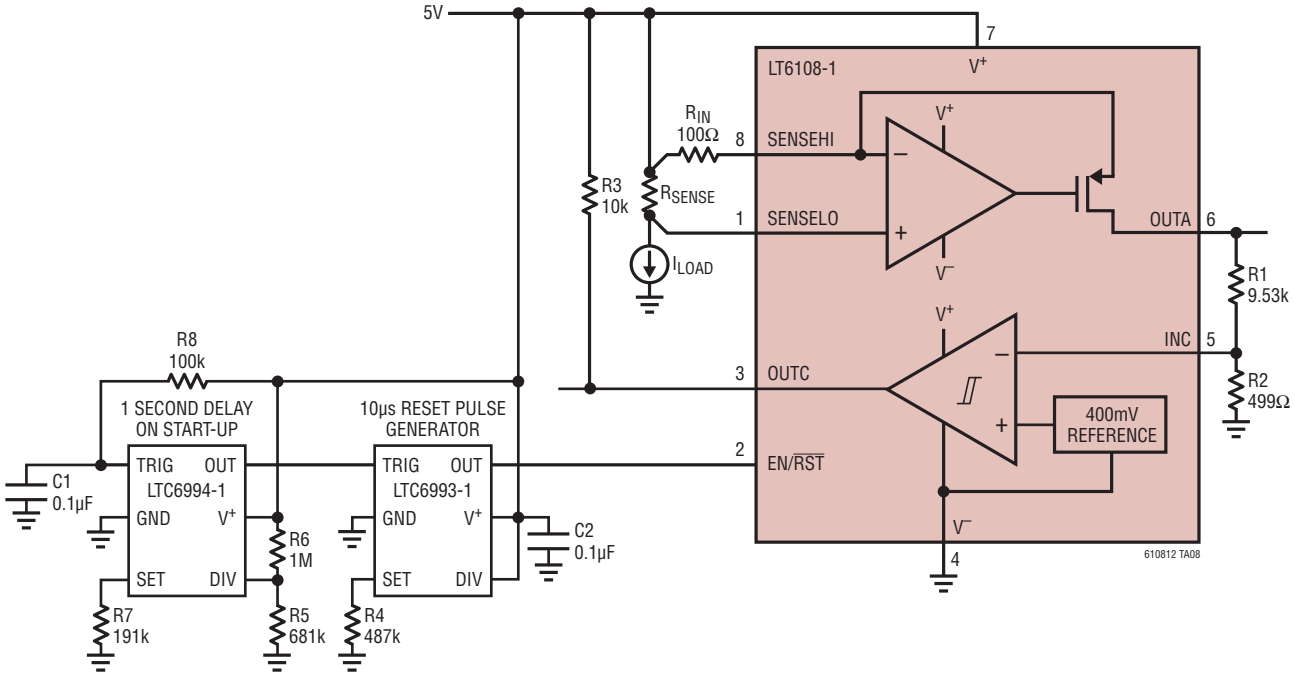
$$V_{TH(R)} = 400mV \text{ if } R4 = R5 \bullet \left(\frac{400mV}{V_{DD} - 400mV} \right)$$

The input falling edge which causes the output to transition from low to high is:

$$V_{TH(F)} = 390mV \bullet R1 \bullet \left(\frac{1}{R1} + \frac{1}{R2 + R4||R5} \right) - \left(\frac{V_{DD} \bullet R1}{R2 + R4||R5} \right)$$

TYPICAL APPLICATIONS

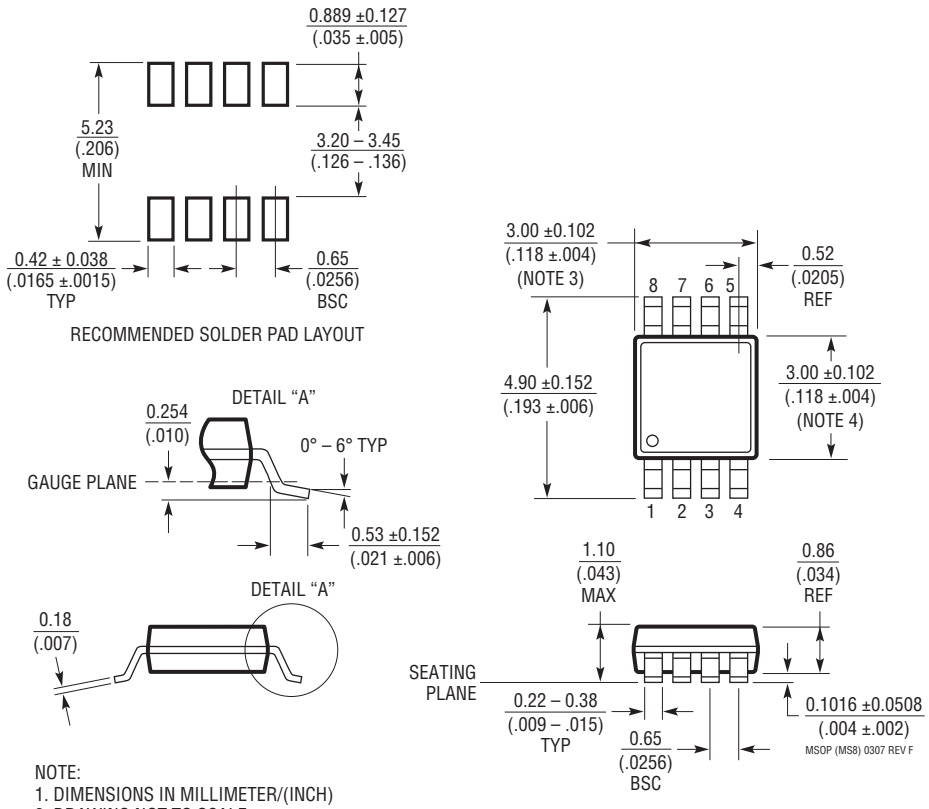
Precision Power-On Reset Using TimerBlox Circuit



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

MS8 Package
8-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1660 Rev F)

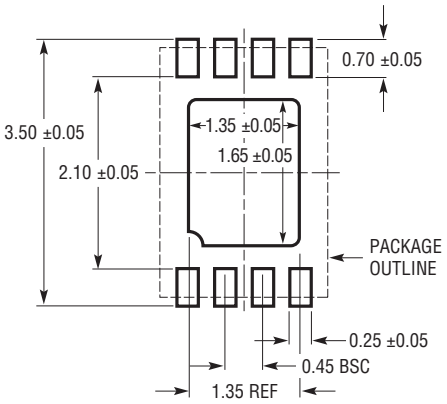


NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

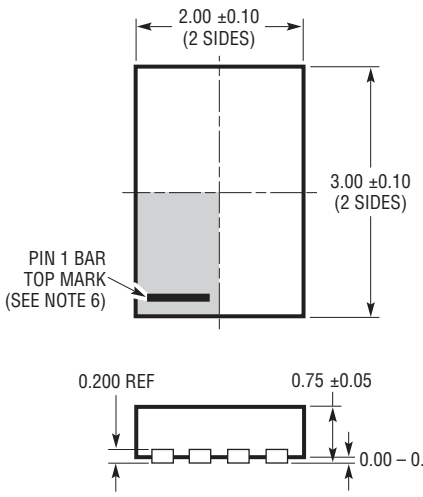
PACKAGE DESCRIPTION

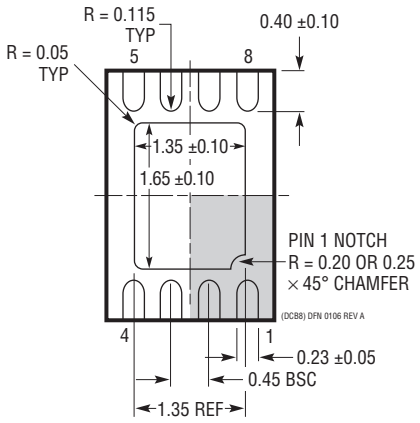
Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

DCB Package
8-Lead Plastic DFN (2mm × 3mm)
(Reference LTC DWG # 05-08-1718 Rev A)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED





BOTTOM VIEW—EXPOSED PAD

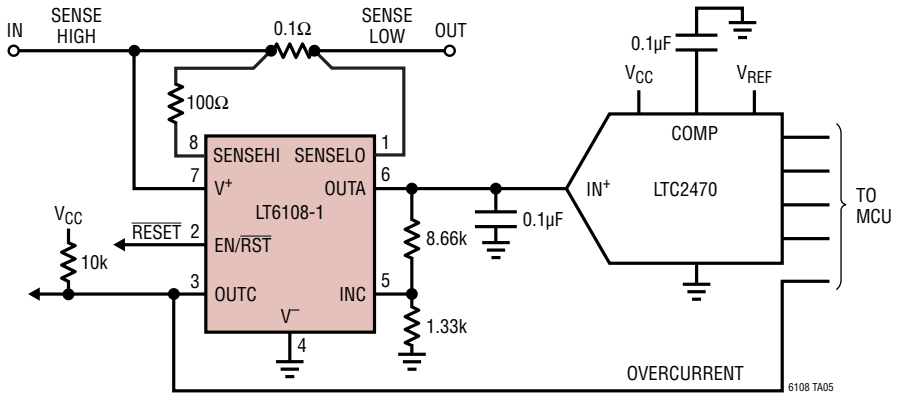
NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	12/12	Addition of A-grade Performance and Electrical Characteristics	1, 3, 4, 5, 12, 13, 16 (Fig10), 28
		Addition of A-grade Order Information	2
		Clarification to Absolute Maximum Short Circuit Duration	2
		Clarification to nomenclature used in Typical Performance Characteristics	6, 7, 9
		Clarification to Description of EN/$\overline{\text{RST}}$ Pin Function	10
		Internal Reference Block redrawn for consistency	11, 13, 18, 19
		Additional information provided to Reverse Supply Protection	22
		Correction to Overcurrent Battery Fault Protection diagram	23

TYPICAL APPLICATION

ADC Driving Application



The low sampling current of the LTC2470 16-bit delta sigma ADC is ideal for the LT6108.

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1787	Bidirectional High Side Current Sense Amplifier	2.7V to 60V, 75µV Offset, 60µA Quiescent, 8V/V Gain
LTC4150	Coulomb Counter/Battery Gas Gauge	Indicates Charge Quantity and Polarity
LT6100	Gain-Selectable High Side Current Sense Amplifier	4.1V to 48V, Gain Settings: 10, 12.5, 20, 25, 40, 50V/V
LTC6101	High Voltage High Side Current Sense Amplifier	Up to 100V, Resistor Set Gain, 300µV Offset, SOT-23
LTC6102	Zero Drift High Side Current Sense Amplifier	Up to 100V, Resistor Set Gain, 10µV Offset, MSOP8/DFN
LTC6103	Dual High Side Current Sense Amplifier	4V to 60V, Resistor Set Gain, 2 Independent Amps, MSOP8
LTC6104	Bidirectional High Side Current Sense Amplifier	4V to 60V, Separate Gain Control for Each Direction, MSOP8
LT6105	Precision Rail-to-Rail Input Current Sense Amplifer	–0.3V to 44V Input Range, 300µV Offset, 1% Gain Error
LT6106	Low Cost High Side Current Sense Amplifier	2.7V to 36V, 250µV Offset, Resistor Set Gain, SOT-23
LT6107	High Temperature High Side Current Sense Amplifier	2.7V to 36V, –55°C to 150°C, Fully Tested: –55°C, 25°C, 150°C
LT6109	High Side Current Sense Amplifier with Reference and Comparators	2.7V to 60V, 125µV, Resistor Set Gain, ±1.25% Threshold Error
LT6700	Dual Comparator with 400mV Reference	1.4V to 18V, 6.5µA Supply Current

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1630 McCarthy Blvd., Milpitas, CA 95035-7417
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Test Report

DFB Laser Diode

Part No.: APLD-1310D-S5-A7A
Serial No.: 1
Date: 14/10/2013

Optical and Electrical Characteristics (@ 25C):

Parameter	Value	Dimensions
CW optical power, P_{op}	**5**	mW
Central wavelength at P_{op}, λ	**1310**	nm
Operating current, I_{op}	**16.8**	mA
Threshold current, I_{th}	**6.2**	mA
Monitor current, $I_{m\ op}$	**376.3**	uA
Efficiency	**0.47**	mW/mA
Package type	**TO-18**	
Cap	**Aspherical Lens Cap**	
Pin type	**A**	

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Test Report

CWDM DFB Laser Diode

Part No.: APLD-1490-cwdm-S5-A7A
Serial No.: 1
Date: 14/10/2013

Optical and Electrical Characteristics (@ 25C):

Parameter	Value	Dimensions
CW optical power, P_{op}	**5**	mW
Central wavelength at P_{op}, λ	**1490**	nm
Operating current, I_{op}	**25.5**	mA
Threshold current, I_{th}	**9.3**	mA
Monitor current, $I_{m\,op}$	**302.6**	uA
Efficiency	**0.31**	mW/mA
Package type	**TO-18**	
Cap	**Aspherical Lens Cap**	
Pin type	**A**	

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Test Report

DFB Laser Diode

Part No.: APLD-1550D-S5-A7A
Serial No.: 1
Date: 14/10/2013

Optical and Electrical Characteristics (@ 25C):

Parameter	Value	Dimensions
CW optical power, P_{op}	**5**	mW
Central wavelength at P_{op}, λ	**1550**	nm
Operating current, I_{op}	**24.2**	mA
Threshold current, I_{th}	**7.7**	mA
Monitor current, $I_{m\ op}$	**166.2**	uA
Efficiency	**0.30**	mW/mA
Package type	**TO-18**	
Cap	**Aspherical Lens Cap**	
Pin type	**A**	

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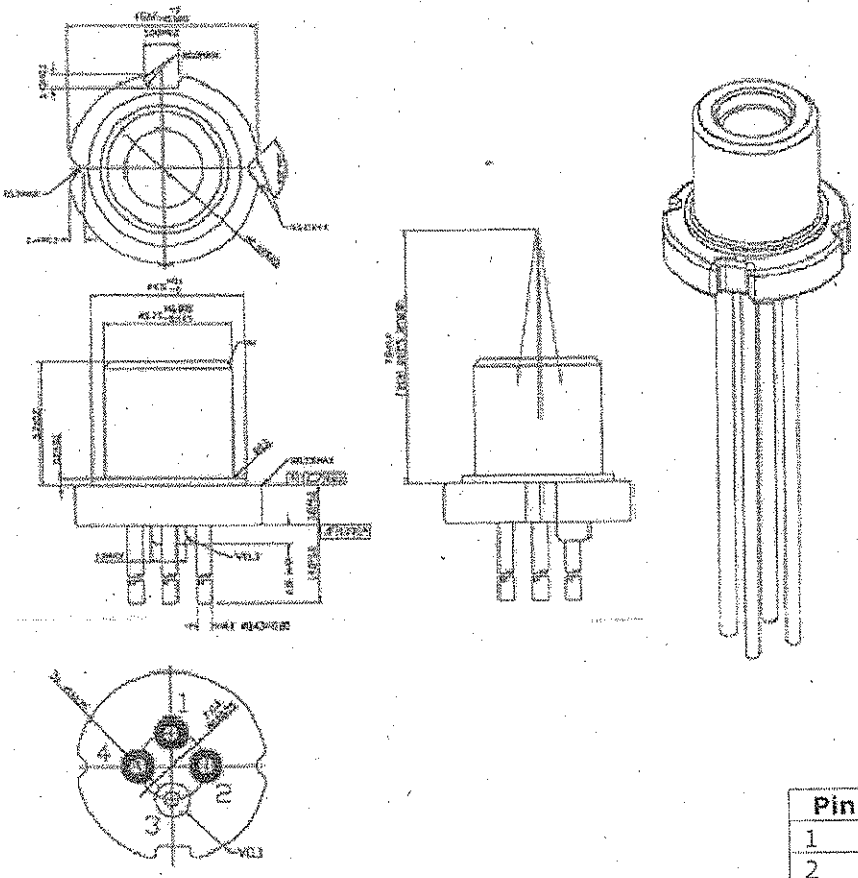
Dimensions and Pin Assignment (type A):



Pin #	Function
1	PD Cathode
2	PD Anode
3	LD Anode, GND
4	LD Cathode

Focal Length = 7.5 ± 1.0 mm

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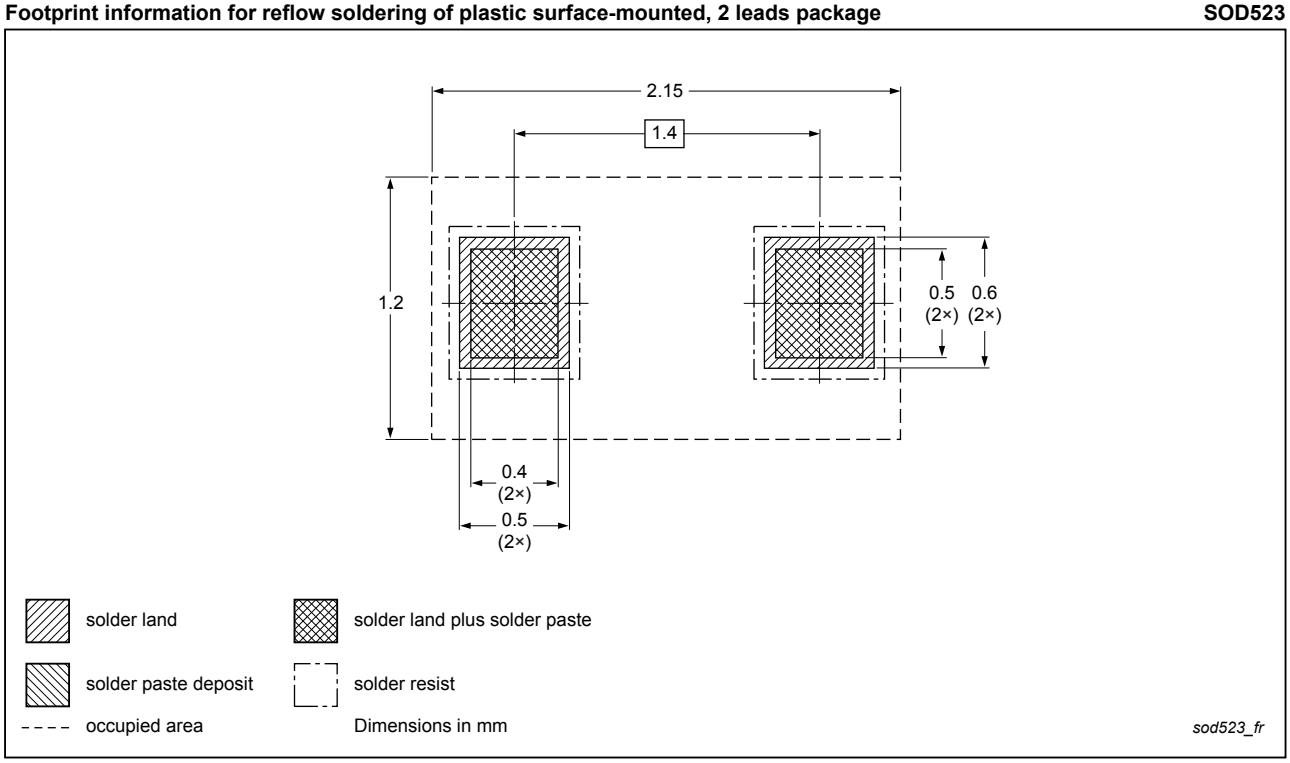
Reflow soldering footprint

Footprint information for reflow soldering of plastic surface-mounted, 2 leads package **SOD523**



6.4 Planos

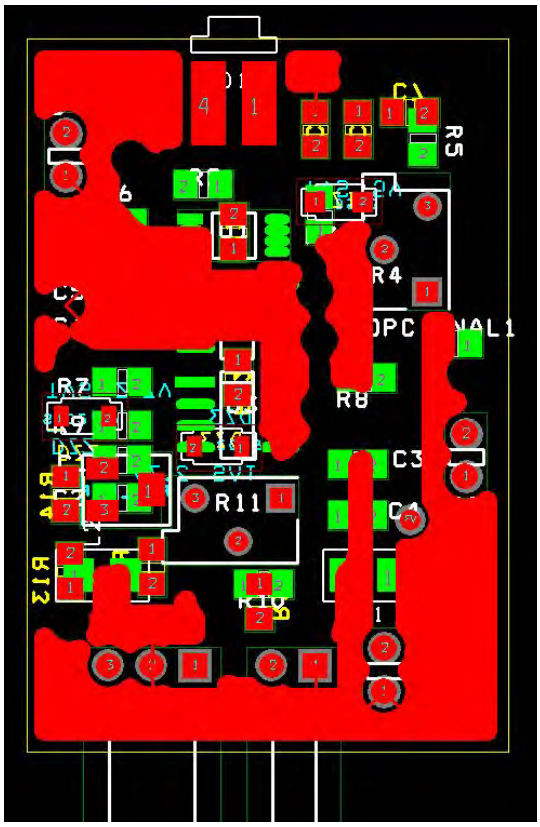


Ilustración 36 Capa Bottom sin rutar

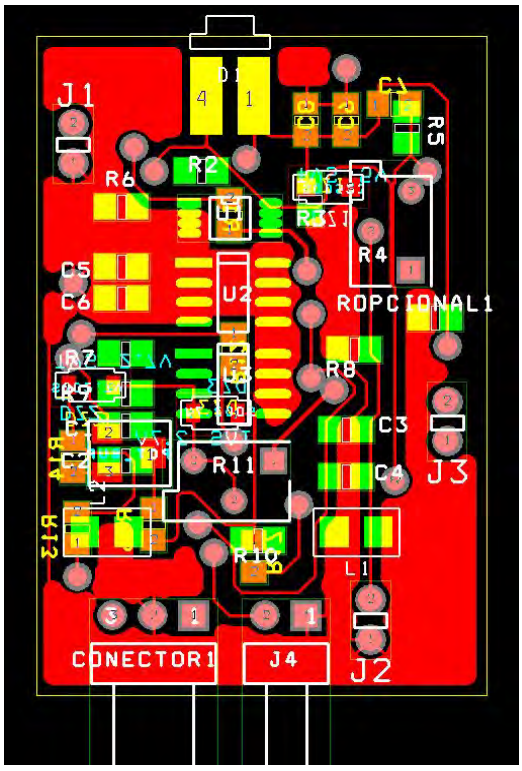


Ilustración 37 Capa Bottom rutada

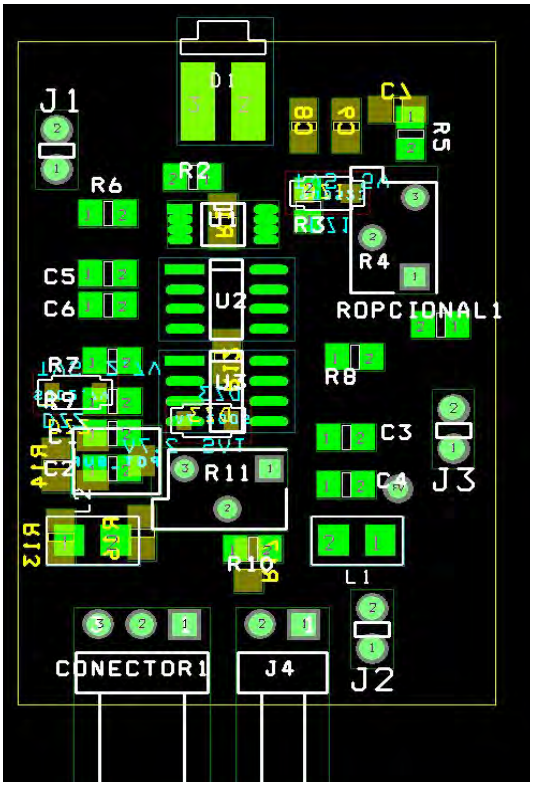


Ilustración 38 Distribución de componentes en la PCB

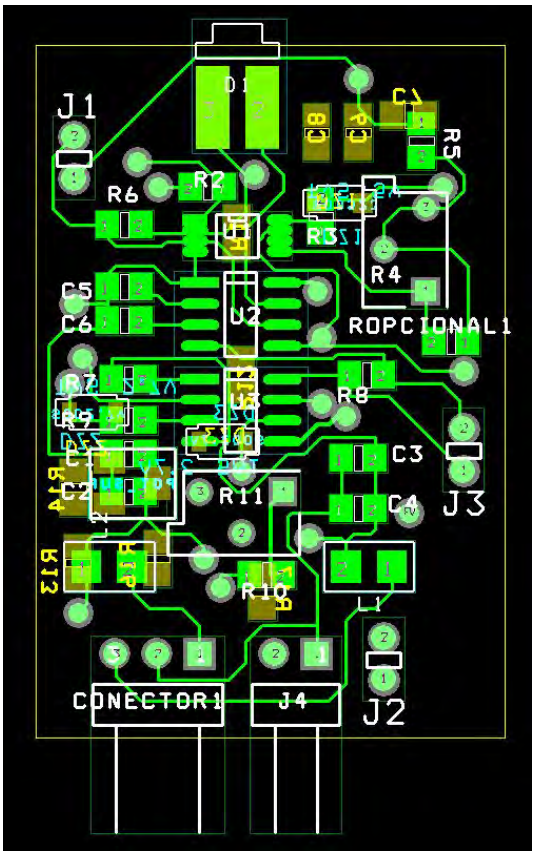


Ilustración 39 Capa Top rutada

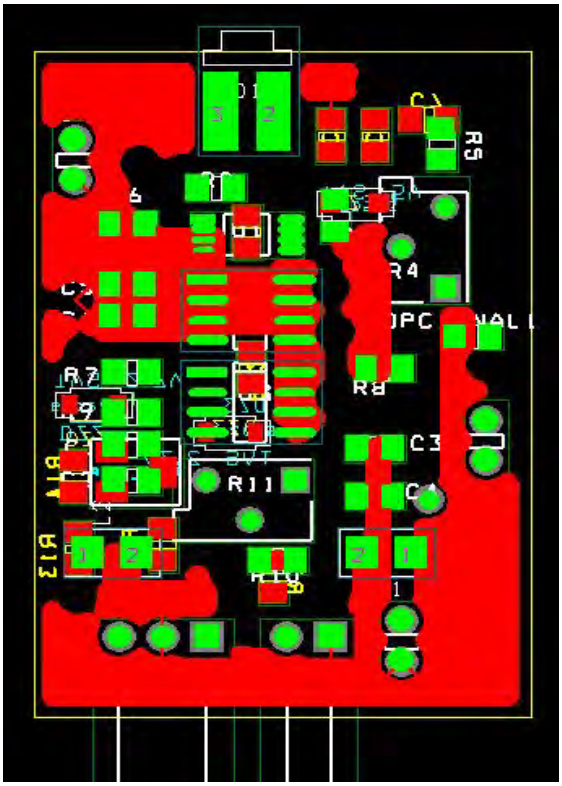


Ilustración 41 Capas Top y Bottom sin rutar

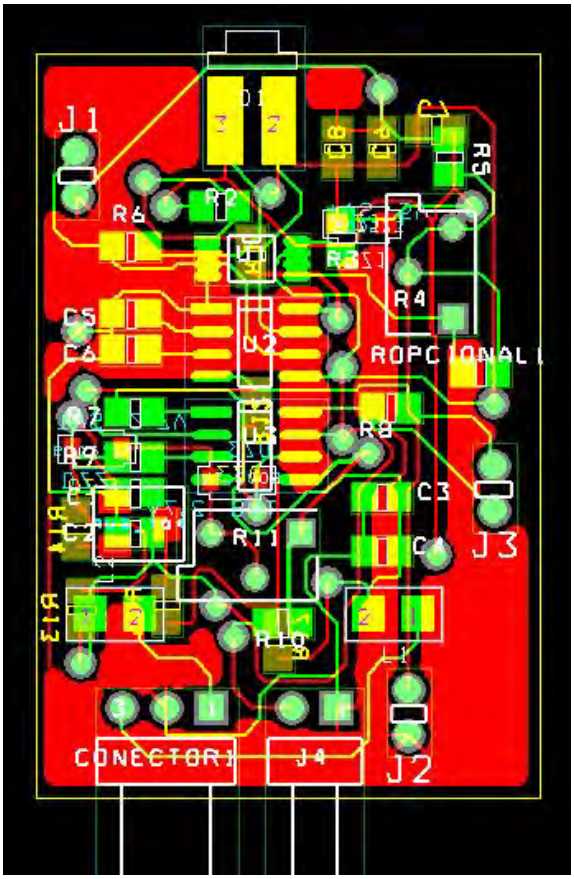


Ilustración 40 Capas Top y Bottom rutadas

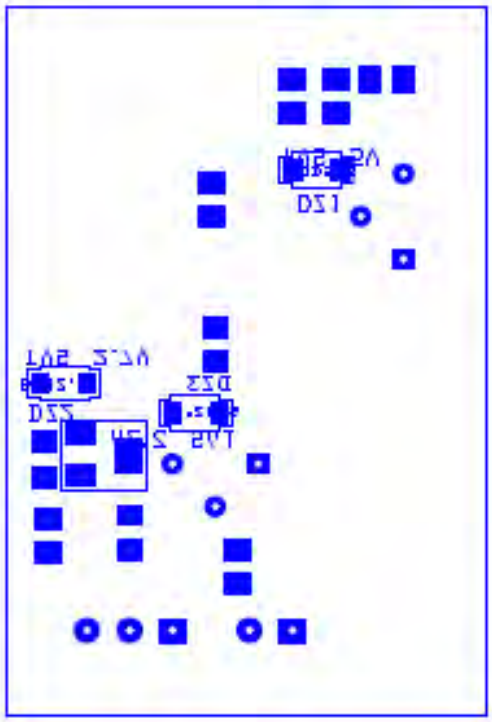


Ilustración 42 Capa Bottom

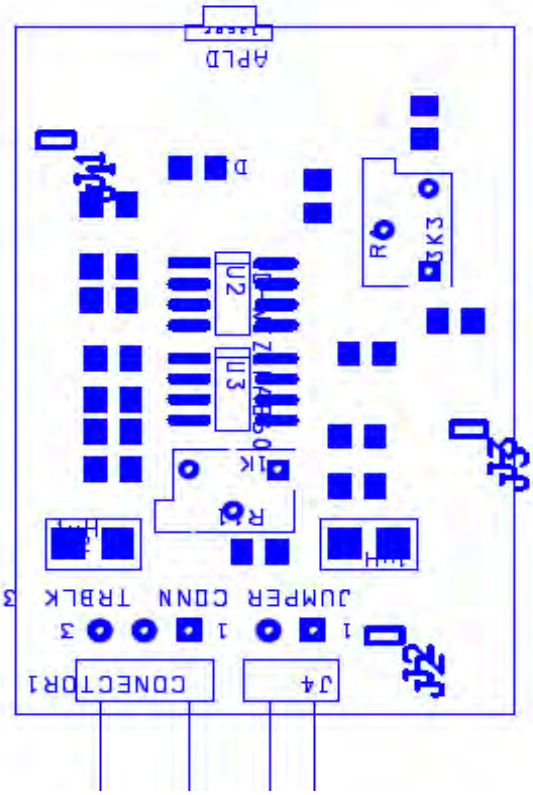


Ilustración 43 Capa Top

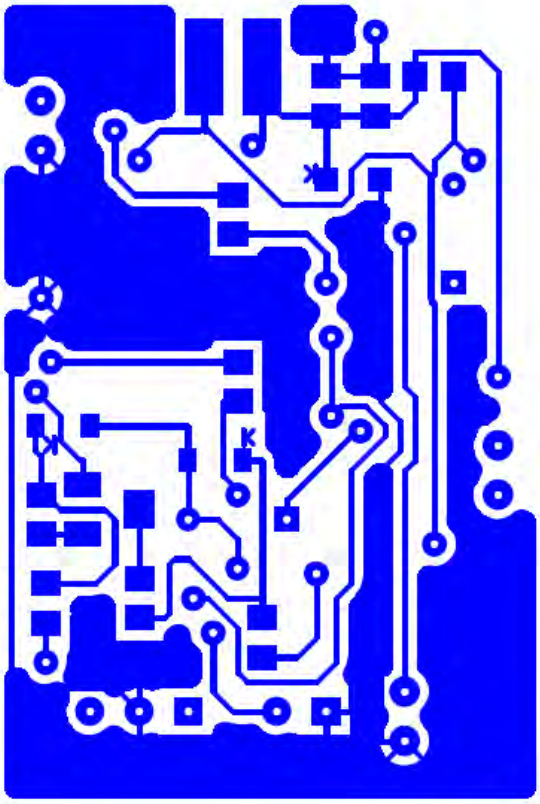


Ilustración 45 Rutado Capa Bottom

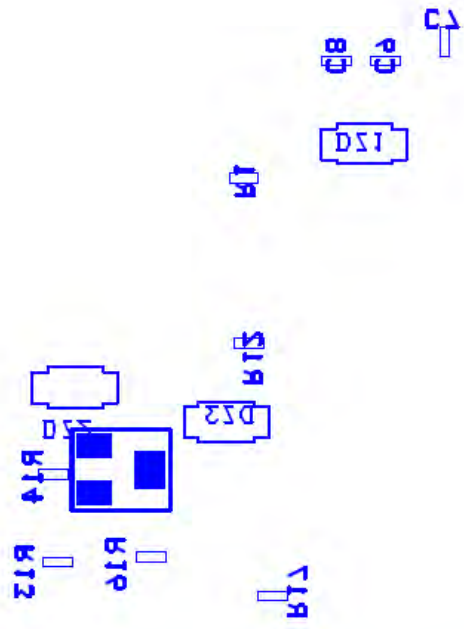


Ilustración 44 Silkscreen Capa Bottom

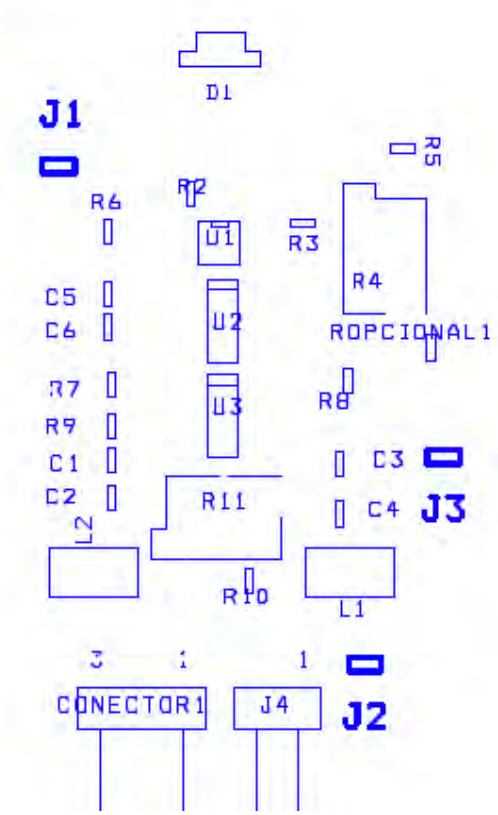


Ilustración 46 Silkscreen Capa Top

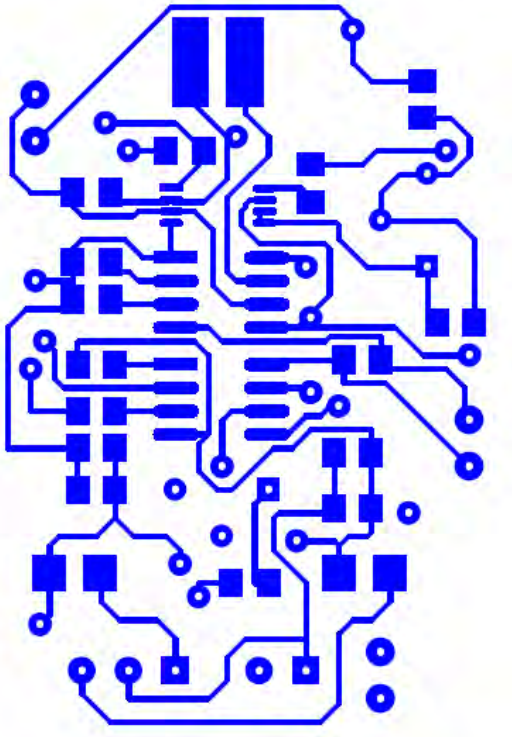
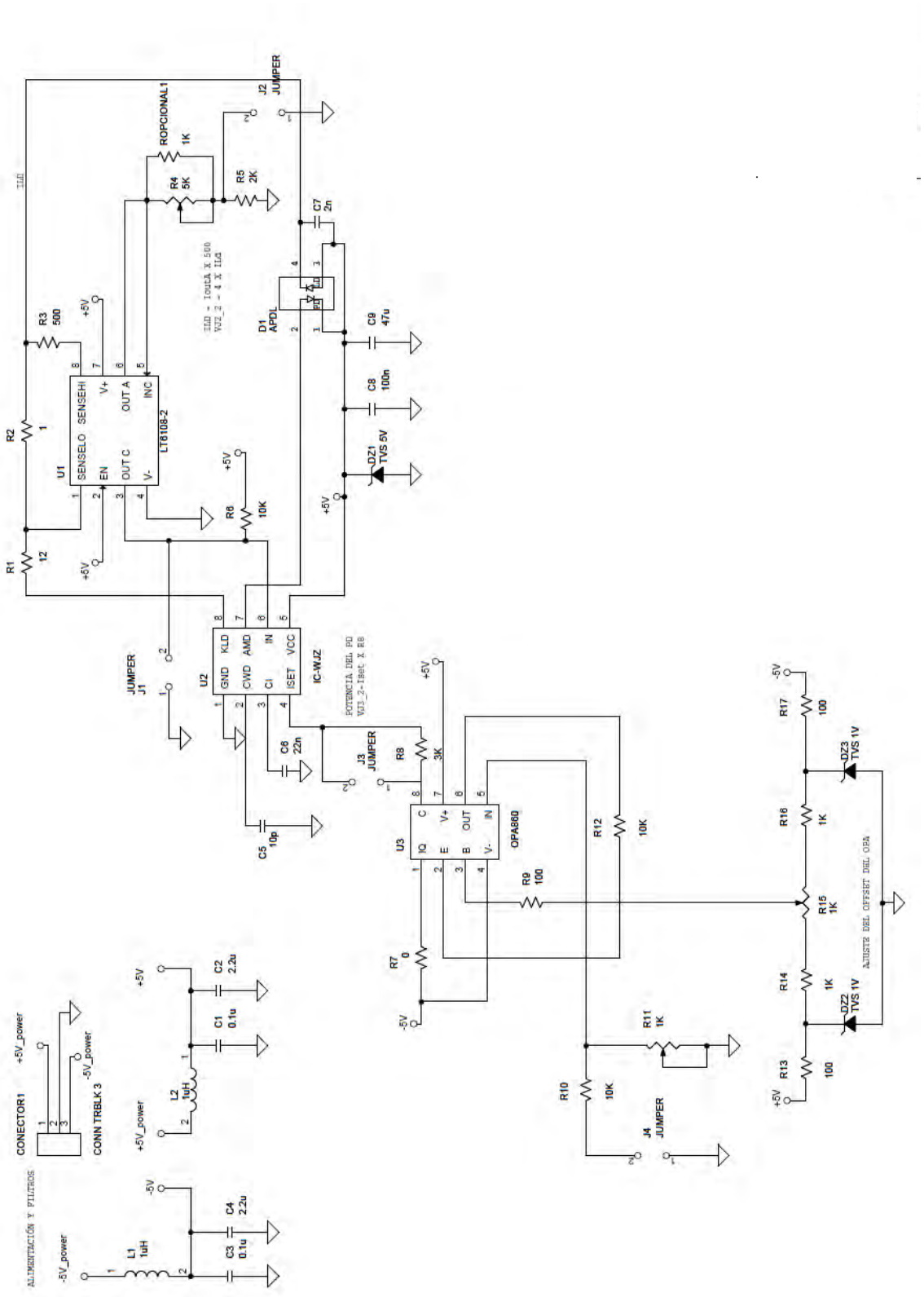


Ilustración 47 Rutado Capa Top

6.5 Esquema del circuito



7. Referencias

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