

# Addressing Schemes Generation for Multiplexed AFLC Displays with Color, Gray Scale and Video Rate Capability

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## 1.- Introduction

In the last years, fiat liquid crystal displays (LCD) have experienced a great spreading, both in its applications as in its manufacturing technology. Ferroelectric Liquid Crystals (FLCs) is the technology on which the research has been mainly focused [1].

Ferroelectric materials are oriented by electric fields. When the SmC\* material is confined into extremely thin sandwiches, lower than 2( $\mu\text{m}$ ), only two states are energetically stable. This is the so-called surface stabilization (SSFLC) [2] of this structure. Applying a DC signal, opposite to polarization, the molecule switches from one state to the other, and without signal the molecules stay in their initial positions. On the other hand, typical antiferroelectric liquid crystal (AFLCs) present double hysteresis (tristability) and analogue gray-scale. Both FLCs and AFLCs show voltage threshold for the optical switching but associated with different physical mechanisms. More recently, thresholdless, hysteresis-free V-shaped switching was observed in AFLC mixtures.

AFLCs have focused a great attention from industrial and scientific community. They show interesting electrooptical properties such as fast response, intrinsic analogue gray scale, wide viewing angle, among others, which are appropriate for high-end video display applications [3].

On the other hand, the performance of the AFLC displays is determined by their electrical and optical behavior [4].

## 2.- Driver Design and Implementation

Several possible approaches have been initially considered, but the following scheme has been yet built in order to address of a 4 x 4 test AFLC display. To demonstrate its video-rate

capability, four sequential colors (RGBG) have been used as backlight. This would permit to check the electrooptical performance of the AFLC display working to video rate. The figure 1 shows a block diagram of the proposed prototype for the signal of row selection. As it can be seen, the system is based on a microcontroller system (Cygnal C8051F310) which manages the following aspects:

- o selection (by means of 2 bits) of the one among the possible four levels through the analogue multiplexor.
- o Temporization of each time slot of the row signal.
- o Synchronization of the data load with the selection pulse of the each row.
- o Selection of the positive/negative framerate (by means of 1 bit), for obtaining DC compensation.
- o Data acquisition of the gray levels from an external memory for each pixel.

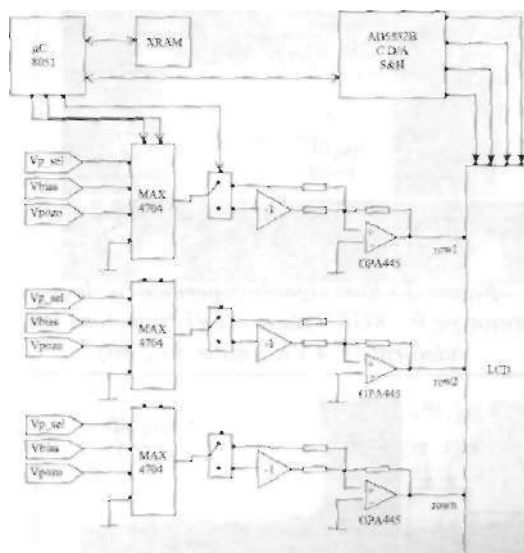


Figure 1. Schematic for the generation of the row selection signal.

To generate the different voltage levels for the pulse selection, holding (bias), well and reset slots [5], a schematic diagram with the circuits used is showed in figure 2. Variable resistors and buffers are employed to choose the appropriate voltage level for each of the four mentioned slots. The operational amplifier (OPA445) amplifies the signal coming from analogue switches to provide maximum values up to  $\pm 35\text{V}$ .

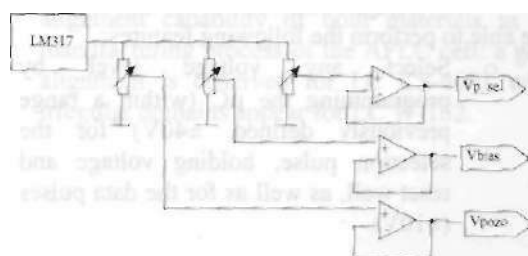


Figure 2. Schematic for the generation of input signals of the analogue switch.

The (iC has 3 timers which will be used to generate the control signals to shape the waveform to address the rows. A diagram showing this can be seen in figure 4.

- o Choose any temporal window by programming the uC (with a minimum resolution of 1 us) for  $t^{ne}$  selection pulse, holding voltage and reset well.
- o Up to 64 gray levels can be stabilized
- o Ease to program any parameter of the addressing waveform for rows and columns as well.

Figures 5-8 acquired from a digital oscilloscope are shown to demonstrate the right functioning of the driver implemented.

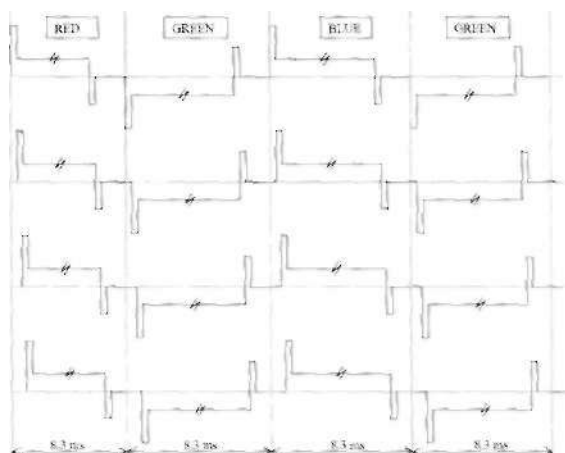


Figure 3.- Row signals generated by the prototype for RGBG sequence (1 frametime for video-rate =  $4 \times 8,3 \text{ ms} = 33,2 \text{ ms}$ )

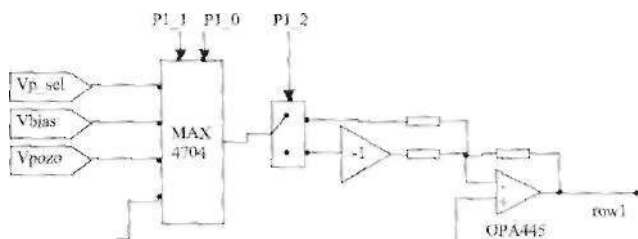


Figure 4.- Control signals coming from three timers of *juC* (Pl\_0, Pl\_1 and Pl\_2) to generate the signal row.

The timers work to make the temporization of each time slot that shapes the row signal as follows: the bits 0 and 1 of port 1 select the appropriate voltage level in the analogue switch, while the bit 2 selects the right semicycle (positive or negative).

The design described for the driver would be able to perform the following features:

- o Select any voltage level by programming the uC (within a range previously defined,  $\pm 40\text{V}$ ) for the selection pulse, holding voltage and reset well, as well as for the data pulses ( $\pm 10\text{V}$ ).

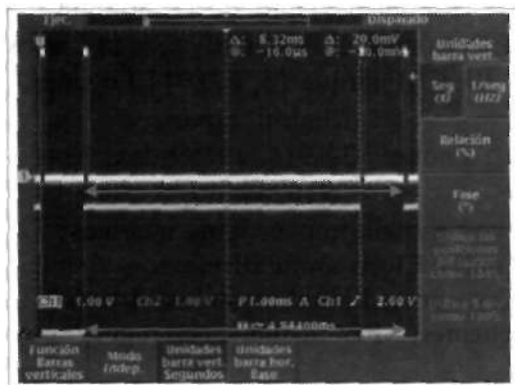


Figure 5.- The yellow and blue Unes represent the control signals associated to the bits `pl_0` and `pl_1`, respectively. The period is 8,3 ms for each one of them.

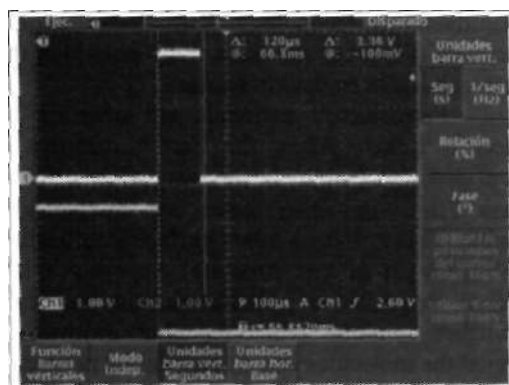


Figure 6.- The yellow and blue Unes represent the control signals associated to the bits `pl_0` and `pl_1`, respectively. The period is 8,3 ms for each one of them (time scale expanded).

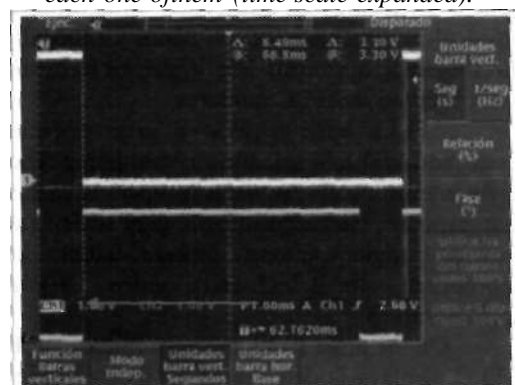


Figure 7. The yellow and blue Unes represent the control signals associated to the bits `pl_2` and `pl_1`, respectively. The yellow signal changes when the semicycle of the row signal is inverted.

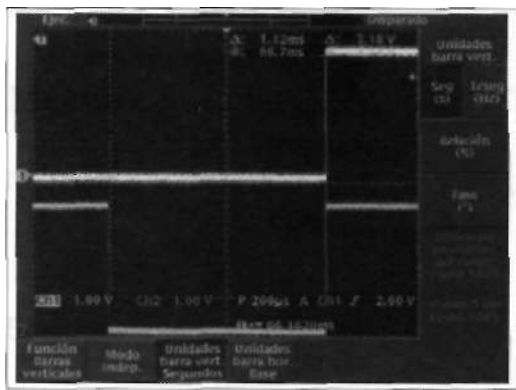


Figure 8. The yellow and blue Unes represent the control signáis associated to the bits  $pl\_2$  and  $pl\_1$ , respectively (time scale expanded).

Additionally, we need 2 bits (LED1, LED0) of the uC port to select the appropriate lighting LED, always following the sequence: RGBG, RGBG, ... LEDs are switched ON once the data in all columns have been loaded and stabilized. The table I presents the combination of the bits (LED1, LED0) that permits the selection of the right LED. The main reason to repeat the LED green during a framerate is to sure that the data have always the same voltage level avoiding the flicker in the display. As an example of this, the figure 9 shows the synchronism signal for the LEDs blue and red.

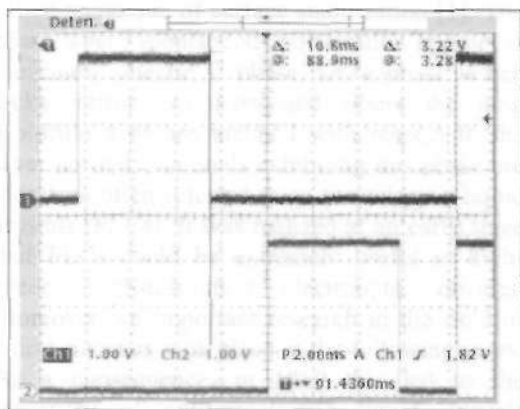


Figure 9. Synchronism signáis for LEDs red and blue during a framerate.

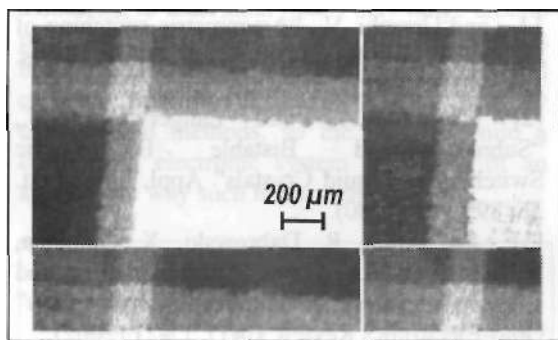
| Lighting LED | LED1 | LED0 | Time   |
|--------------|------|------|--------|
| Red          | 0    | 1    | 5.8 ms |
| None         | 0    | 0    | 2.5 ms |
| Green        | 1    | 0    | 5.8 ms |
| None         | 0    | 0    | 2.5 ms |
| Blue         | 1    | 1    | 5.8 ms |
| None         | 0    | 0    | 2.5 ms |
| Green        | 1    | 0    | 5.8 ms |
| none         | 0    | 0    | 2.5 ms |

Table I. Two bits of  $\mu C$  (LED1, LED0) select the LED that we want to switch ON. Time is taken from the moment that data are stabilized.

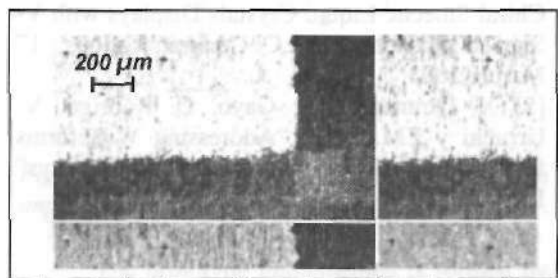
Concerning to the column driver, data are monopolar pulses varying their amplitude between 0V and 12V. The intermediate values corresponding to the different gray levels previously defined. The microcontroller will take the gray levels of each pixel from an external memory connected to it. The appropriate voltage level will address the LCD pixels through digital-analogue converters and sample&hold circuits.

#### 4.- Preliminary Experimental Results and Discussion

We have applied the signals generated from the prototyped driver to two AFLC displays supplied from CLIQ-UPM Group. Figures 10-11 show preliminary results obtained for the gray levels in two AFLC materials tested: CS-4001 (commercial) and W-162 (experimental).



(a)



(b)

Figure 10. Switching of 4 pixels giving different gray levels when they are addressed by the signals generated by the driver developed: (a) LC material CS-4001; (b) LC material W-162.

As it can be seen, the best results concerning to the uniformity of gray scale are obtained for the LC commercial material (CS-4001) compared with the experimental one (W-162). The reason may be attributed to the alignment capability of both materials in the manufacturing process of the AFLC cell: a good alignment is observed for LC CS-4001 while irregular domains appear for LC W-162.

## 5.- Conclusions

A new row and column driver to address multiplexed AFLC displays with color and video rate capability has been designed. The architecture chosen to allow addressing any number of pixels by reproducing the hardware circuits for a row and column so times as necessary. Preliminary waveforms have been acquired with a digital oscilloscope showing the right functioning of the implemented prototype.

## 6.- Acknowledgements

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## 7.- References

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