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A Pulse Frequency Modulation VCO-ADC in 40nm

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Abstract—This paper describes the architecture and implementation of a novel voltage controlled oscillator based analog-to-digital converter (VCO-ADC). Instead of a ring oscillator (RO), the VCO is built with a pulse frequency modulation (PFM) architecture where an analog feedback loop ensures both oscillation and linearity of the voltage-to-frequency conversion. A multi-bit, self-centering, noise-shaped output is achieved by sampling a digital delay line that acts as a part of the oscillator and as a multi-bit quantizer. A prototype has been implemented in a 40nm CMOS process. Although most of the circuit elements are taken from a standard digital library, a transconductor is required as input stage. To ensure proper linearity, a bulk-driven transconductor has been designed. The ADC measurements reach 53 dB of SNDR at 1 GHz sampling frequency in a 20 MHz bandwidth with a pseudo-differential architecture. Powered at 1.1 V, the power consumption is 3.5 mW. The active area is 0.08 mm². The resulting FoM equals 242 fJ/step.

Index Terms—Analog-to-digital conversion, noise shaping, pulse frequency modulation, voltage controlled oscillator.

I. INTRODUCTION

VOLTAGE controlled oscillator based analog-to-digital converters (VCO-ADCs) are considered as a potential architecture to overcome the poor performance of analog nanometer CMOS circuits [1]. VCO-ADCs behave like noise-shaped oversampled systems and can be implemented with mostly digital circuits, in special ring oscillators (ROs) [2]. The main drawback of VCO-ADCs that use ROs is the non-linear voltage-to-frequency transfer function of the VCO, which limits the resolution of the converter. Attempts to overcome this issue include the use of digital calibration [2], dithering [3] or digital precodeing [4]. However these techniques lead to large and power-hungry circuits. Recently, new ways to deal with the non-linearity problem have been proposed [5], [6].

A pulse frequency modulation (PFM) VCO-ADC architecture was described in [7], [8] as an alternative to VCO-ADCs implemented with ROs. This architecture is intrinsically linear and can be mostly designed with digital circuits. The differences between PFM-based and RO-based VCO-ADCs were outlined in [9]. In this paper, an implementation of a PFM VCO-ADC in 40nm is presented. The prototype reaches 8.5-bit ENOB for 20 MHz bandwidth (BW) with 3.5 mW of power consumption. A linear bulk-driven transconductor architecture is also described. This transconductor achieves 65 dB attenuation of the third harmonic distortion (HD3) at full scale input.

II. PFM VCO-ADC ARCHITECTURE

A. Linear model of the PFM VCO-ADC

The operating principle of a PFM VCO-ADC can be described with the help of Fig. 1(a), where the input signal \( x(t) \) is encoded with a pulse frequency modulator and sampled with a digital delay line. The pulse frequency modulator is composed of a VCO, an edge detector block that generates a Dirac delta impulse at each rising edge of the VCO output \( u(t) \), and a pulse shaping filter \( h(t) \) that generates a square pulse with length \( T_d \) at each impulse in \( d(t) \). Signal \( d(t) \) is only theoretical and cannot be implemented in practice. We make use of it just to explain the linear model of the proposed architecture. We will see later how to go from this linear model to a real circuit.

The equations that describe every signal in Fig. 1(a) and the PFM-based theory that applies here were extensively discussed in [7], [9]. According to [7], in order to avoid aliasing effects that degrade the performance, we must satisfy:

\[
T_d = \frac{1}{f_s} = T_i,
\]

where \( f_s \) is the sampling frequency used later in the delay line. From [7], the linear model of Fig. 1(a) is the one depicted in Fig. 1(b), where signal \( y(t) \) follows:

\[
Y^\ast(s) = K_{VCO} \cdot X^\ast(s) + \left( 1 - z^{-1} \right) M(s)^\ast,
\]

where \( ^\ast \) is the star operator, \( M(s) \) represents the VCO modulation components and \( K_{VCO} \), the gain of the VCO.

Equation (2) shows that the system works similar to a first-order \( \Delta \Sigma \) modulator. Whereas the input signal \( X(s) \) is seen
at the output as it is but multiplied by the VCO gain, the modulation components \( M(s) \) are first-order noise shaped. Consequently, the PFM architecture could be used itself as an ADC.

We will consider next how this architecture can be transformed into an efficient ADC. VCO-ADCs are usually implemented with multiphase ROs [2]. A multiphase architecture produces a multibit output. In the case of PFM VCO-ADCs, a multibit output can be implemented if the oscillating signal \( y(t) \) is sampled after a continuous-time finite-impulse-response (FIR) filter [10]. Such FIR filter operates on a binary, pulse like signal. Therefore its delays can be implemented with a digital delay line as shown in Fig. 1(a). This delay line is composed of \( N \) time delay elements, with a nominal delay of \( T_i / N \) each. All the outputs of the delays are added into a multibit digital signal that is sampled afterwards. In the right side of Fig. 1(b) we can see the linear model of this delay line. Similarly to (2), we can get the following expression for the output signal \( Y_D(s) \):

\[
Y_D(s) \approx N \cdot K_{VCO} \cdot X(s) + \left( 1 - z^{-1} \right) \sum_{i=0}^{N-1} e^{-i\pi s} M(s).
\]  

Equation (3) shows that the modulation components are filtered by an additional low-pass FIR filter, which implies a resolution enhancement with respect to (2).

B. System Level Architecture

The building block diagram of Fig. 2(a) illustrates how the PFM VCO-ADC architecture was implemented in the chip. Fig. 2(a) is composed of an integrator, an asynchronous comparator with a fixed threshold voltage \( V_{th} \), a rising-edge triggered monostable, and a feedback digital-to-analog converter (DAC) with a gain \( K_{DAC} \) that closes the loop. This circuit behaves similarly to the combination of a VCO followed by an edge detector and the \( h(t) \) filter, which is the architecture depicted in Fig. 1(a). The advantage here is that the monostable pulse is embedded in the oscillation loop, which improves the linearity of the VCO if compared to a conventional RO [2]. The output of the monostable \( y(t) \) is a pulse frequency modulated signal. The delay chain of Fig. 1(a) will be implemented later on inside the monostable circuit of the chip.

In Fig. 2(b) we can see an example of the typical waveforms involved in the oscillation loop. As can be observed, the sign switching of \( e(t) \) makes the integrated signal \( \xi(t) \) to increase or decrease. If the monostable is idle and no pulse is being generated, \( e(t) \) is positive and \( \xi(t) \) increases. When \( e(t) \) reaches \( V_{th} \), the comparator triggers the monostable and a constant-length pulse is generated. The pulse is fed back into the integrator. This forces \( e(t) \) to be negative and \( \xi(t) \) is decreased. When the pulse finishes, \( e(t) \) increases again and the oscillation cycle is repeated. The lowest value reached by \( e(t) \) at the end of the monostable pulse depends on \( x(t) \). Then, the time that \( e(t) \) takes to reach \( V_{th} \) afterwards also depends on \( x(t) \). If we keep the notation of Fig. 2(b), the oscillation frequency of the system \( f_{osc}(t) \) can be calculated as follows:

\[
f_{osc}(t) = f_0 + K_{VCO} \cdot x(t) = \frac{V_{DD} - K_{DAC} V_{GND}}{K_{DAC} T_e (V_{DD} - V_{GND})} + \frac{1}{K_{DAC} T_e (V_{DD} - V_{GND})} \cdot V_{GND} x(t),
\]  

where \( V_{DD} \) is the supply voltage and \( V_{GND} \) is the ground supply. As can be observed, \( f_{osc}(t) \) depends linearly on \( x(t) \). As opposite to prior works, the linearity does not depend on the compensation of the nonlinear delay dependence of an inverter [6] or on digital calibration circuits [2].

A behavioral model of the PFM VCO-ADC was simulated to check the performance of the system. Fig. 3 depicts the results of the simulation. The parameters used in the simulation are: \( f_0 = 1 \) GHz, \( B = 20 \) MHz, \( f_{osc} = 500 \) MHz and \( N = 15 \). The input signal is a -3 dBFS sinusoidal waveform with frequency equal to 1 MHz. The resulting SNDR equals 58 dB.

C. Circuit Implementation

The circuit implemented in the chip is depicted in Fig. 2(c). This circuit corresponds to a pseudo-differential implementation of the block diagram of Fig. 2(a). The block diagram uses a fully differential input stage that drives two oscillators encoding the input signal [2]. Two 5-pF capacitors are used to perform a current integration. The current integration is split into two components, the input signal and the feedback pulse. The input voltage \( x(t) \) is converted into a differential current by means of a transconductor \( g_{in} \). The integration of the feedback pulse is implemented by means of two independent single-bit current DACs (IDACs). The voltage in the capacitor is compared to a threshold value with an open-loop comparator implemented with a chain of inverters. The integrating capacitors are connected to \( V_{DD} \), therefore \( e(t) \) in the chip is actually the mirrored version of signal \( e(t) \) in Fig. 2(b) with respect to \( V_{DD} \). The comparator output triggers a monostable composed of a rising-edge triggered set-reset flip-flop and a chain of 15 digital buffers. The different phases of the oscillator are taken from the outputs of these digital buffers, which implement the delay line of Fig. 1(a). Finally, each output of the digital buffers is sampled and post-processed. The chip has been designed and implemented in a 40nm CMOS process with a supply voltage of 1.1 V.

A. Bulk-Driven Transconductor

The circuit employed for the transconductor is a bulk-driven degenerated differential-pair structure. As can be observed in Fig. 2(c), the transconductor is placed in an open-loop configuration. Consequently, the associated distortion will not be compensated by any loop and might degrade the final SNDR. Therefore, a highly linear architecture is required to keep the distortion components below the in-band quantization noise level.

It is known that bulk-driven circuits are especially suitable for low voltage designs [11]. First of all, the threshold voltage requirements are removed. In addition, the conductance of a bulk-driven MOSFET is lower than its gate-driven equivalent. Our design benefits from these two facts because they
Fig. 2. (a) PFM-based oscillation loop, (b) Chronogram of PFM-based oscillation loop, (c) Implemented circuit of the PFM VCO-ADC, and (d) System sensitivity to variations in the length of the digital pulse.

Fig. 3. Behavioral simulation of the proposed PFM VCO-ADC.

Fig. 4. PFM VCO-ADC circuits: (a) Transconductor, (b) IDAC, (c) Comparator, (d) Monostable.
the gain of the oscillator. The current sources are connected by
different current switch to either the integrating capacitor
or to a dummy resistance $R_{DAC}$. This way, $M_5$ and $M_6$ keep
always biased and ringing in the output current is mitigated.

C. Comparator, monostable and digital logic

The design of the comparator, the monostable, the sampling
circuitry and the digital output interface shown in Fig. 2(c)
mostly based on the standard 40nm CMOS digital library.

Fig. 4(c) depicts the circuit of the comparator, built as a
cascade of inverters. As the rest oscillation frequency of the
loop is in the order of hundreds of MHz, the comparator delay
must be very low. The maximum capacitor voltage swing is
of 30 mV only. Consequently, a high-gain and high-speed
inverter architecture is required, at least for the first inverter.
The comparator is therefore implemented with a first current-
controlled NMOS-based inverter followed by two standard
CMOS inverters. $V_{th}$ is the switching voltage of the first
inverter. The output of this structure is already a digital signal
that triggers the monostable.

With respect to the sampling circuit, we may notice that it
is not the conventional sampling architecture used for VCO-
ADCs implemented with XOR gates [2]. We require the
sampled pulse to be equal to $T_c$, regardless of the actual length
of the square pulse generated by the monostable. Fig. 2(d)
shows the sensitivity of the system to variations in the length
of the digital pulse. The proposed sampling circuit of Fig. 2(c)
is a 1-bit counter with asynchronous reset, that counts up with
the rising edges of the phases of the monostable $\phi(t)$ and is
cleared each rising edge of the clock signal. This way, we
make sure that every pulse is translated to each output with
only one sample at logic '1' avoiding data replication.

The delay line used in the monostable is composed of 15
taps implemented with digital inverters (see Fig. 4(d)). The
independent tap outputs are encoded with a thermometer to
binary logic (T2B) to minimize the number of output bits.

Finally, the output data stream is stored in an on-chip first-in
first-out (FIFO) RAM, from where data can be read at lower
rate through a USB interface.

D. Calculation of oscillation parameters

If we calculate $f_{osc}(t)$ in Fig. 2(c), we will get:

$$f_{osc}(t) = \frac{I_{DC,em} - I_{DC} + \frac{d}{d_t} x(t)}{C_{m} \cdot R_{dac}} \text{,(5)}$$

where $I_{DC,em}$ is the DC current of the transconductor $g_{m}$.

As can be observed, we have several parameters that can be
trimmed to achieve the desired oscillation parameters. With
that purpose in mind, we have added some programming logic
to both the bias current sources and the IDAC elements, which
can be tailored to program $f_d$ and $V_{CCO}$. The supply voltage
of the monostable is provided by an on-chip programmable
low-dropout regulator (LDO). This allows us to change the
monostable supply voltage to modify the delays of the buffers
and the length of the generated pulse $T_d$.

IV. EXPERIMENTAL RESULTS

The proposed PFM VCO-ADC was fabricated using a 40nm
CMOS process.1.1 V supply voltage in a multi-project test
chip housing common test circuitry such as clock drivers, USB
ports and a RAM. The die photo of the chip is shown in
Fig. 5(a). The layout is arranged symmetrically along the
horizontal axis for the two sides of the pseudo-differential
architecture. It occupies an area of 550 $\mu$m x 290 $\mu$m. If we
take into consideration only the ADC circuit core without the
test interface, the occupied area is 0.08 mm$^2$.

To measure the performance of the chip, we have two
possible interface choices. As a first choice, we have a...
test-pin from where we can observe the oscillation of each VCO. To allow the use of a standard CMOS pad, the VCO output is divided by a factor of four and turned into a 50% duty-cycle square signal. The down-divided signal is captured at high speed using a sampling oscilloscope and stored for post-processing in a computer. Fig. 5(b) shows the spectrum of the ADC through the test-pin with no input signal. A tone can be observed at 100 MHz, corresponding to the idle oscillation frequency programmed at 400 MHz. The power consumption of the clock generator is not included. This work describes a 40nm CMOS prototype of a PFM VCO-ADC. The architecture is implemented with mostly digital circuitry, which makes it suitable for deep-submicron processes. A new highly-linear bulk-driven transconductor is described and practically tested, which enables the system to exhibit high linearity. Measurements taken from the chip shows a peak SNDR= 53 dB for BW= 20 MHz with power consumption of only 3.5 mW and an active area of 0.08 mm².

**TABLE I**

<table>
<thead>
<tr>
<th>Process (nm)</th>
<th>BW (MHz)</th>
<th>SNDR (dB)</th>
<th>Area (mm²)</th>
<th>Power (mW)</th>
<th>FoM (fJ/step)*</th>
</tr>
</thead>
<tbody>
<tr>
<td>[2]</td>
<td>130</td>
<td>63.1</td>
<td>0.078</td>
<td>12.6</td>
<td></td>
</tr>
<tr>
<td>[3]</td>
<td>85</td>
<td>58</td>
<td>0.14</td>
<td>8.2</td>
<td>0.59</td>
</tr>
<tr>
<td>[4]</td>
<td>40</td>
<td>68.8</td>
<td>0.16</td>
<td>4.08</td>
<td>35</td>
</tr>
<tr>
<td>[5]</td>
<td>20</td>
<td>59.1</td>
<td>0.11</td>
<td>4.3</td>
<td>366</td>
</tr>
<tr>
<td>[6]</td>
<td>10</td>
<td>58.1</td>
<td>0.08</td>
<td>0.70(37)</td>
<td></td>
</tr>
<tr>
<td>[7]</td>
<td>25</td>
<td>37.4</td>
<td>0.22</td>
<td>4.8</td>
<td>244</td>
</tr>
<tr>
<td>[8]</td>
<td>16</td>
<td>32.5</td>
<td>0.21</td>
<td>54</td>
<td>64</td>
</tr>
<tr>
<td>This work</td>
<td>40</td>
<td>20</td>
<td>0.08</td>
<td>3.5</td>
<td>242</td>
</tr>
</tbody>
</table>

* Walden Figure-of-Merit.

**REFERENCES**


