UNIVERSIDAD CARLOS III DE MADRID
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PhD Dissertation SUMMARY

CONTRIBUTION TO THE MODELLING AND DESIGN OF LOW POWER AND LOW OVERSAMPLED CONTINUOUS TIME SIGMA DELTA MODULATORS.

Original Title:

CONTRIBUCIÓN AL MODELADO Y DISEÑO DE MODULADORES SIGMA-DELTA EN TIEMPO CONTINUO DE BAJA RELACIÓN DE SOBREMUESTREO Y BAJO CONSUMO DE POTENCIA

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Preface

Continuous-Time Sigma-Delta modulators are often employed as analog-to-digital converters. These modulators are an attractive approach to implement high-speed converters in VLSI systems because they have low sensitivity to circuit imperfections compared to other solutions.

This dissertation is a contribution to the analysis, modeling and design of high-speed Continuous-Time Sigma-Delta modulators. The resolution and the stability of these modulators are limited by two main factors, excess-loop delay and sampling uncertainty. Both factors, among others, have been carefully analyzed and modeled.

A new design methodology is also proposed. It can be used to get an optimum high-speed Continuous-Time Sigma-Delta modulator in terms of dynamic range, stability and sensitivity to sampling uncertainty. Based on the proposed design methodology, a software tool that covers the main steps has been developed.

The methodology has been proved by using the tool in designing a 30 Megabits-per-second Continuous-Time Sigma-Delta modulator with 11-bits of dynamic range. The modulator has been integrated in a 0.13-μm CMOS technology and it has a measured peak SNR of 62.5dB.

The dissertation has been originally written in Spanish. This document is only a summary of the main chapters and contributions and should be considered as a complement of the original work. The main tables and figures have been translated, and references have been included again to help the reader.

Index

Index of tables

Index of figures

Glossary

A/D	Analog-to-Digital (Converter)
CAD	Computer-Aided Design
CMOS	Complementary Metal-Oxide-Semiconductor (Technology)
CT-SDM	Continuous-Time Sigma-Delta Modulator
D/A	Digital-to-Analog (Converter)
DNL	Differential Non-Linearity
DR	Dynamic Range
DT-SDM	Discrete-Time Sigma-Delta Modulator
DWA	Data Weighted Averaging (Dynamic element matching algorithm)
ELD	Excess-Loop Delay
ENOB	Effective Number Of Bits
HD2	Second harmonic power divided by input power
HD3	Third harmonic power divided by input power
HDi	i-th harmonic ower divided by input power
IIR	Infinite Impulse Response
IM3	Third intermodulation product
INL	Integral Non-Linearity
MFB	Multiple feedback
MFF	Multiple Feedforward

MFF&FB	Multiple Feddforward and multiple feedback
MOS	Metal-Oxide-Semiconductor
NRZ	Non-Return-to-Zero
NTF	Noise Transfer Function
OSR	OverSampling Ratio
RZ	Return-to-Zero
SFDR	Spurious-Free Dynamic Range
SNDR	Signal-to-Noise-and-Distortion Ratio
SNR	Signal-to-Noise Ratio
SPI	Serial Programming Interface
STF	Signal Transfer Function

Chapter 1

Design methodologies for Continuous-Time Sigma-Delta Modulators

This chapter summarizes the design techniques for low-pass Continuous-Time Sigma-Delta Modulators (CT-SDM) that are published in the technical literature.

The first section deals with different methods of specifying the NTF of a CT-SDM. The second section discusses architecture selection. Finally, the last section refers the most used tools in the design of CT-SDM.

NTF specification is the first step in a CT-SDM design process. The achieved resolution and stability margin depends on NTF selection.

Consider the block diagram of a CT-SDM and its linear model, both shown in fig. 1.1. The model has a filter block with two inputs and one output. This filter imposes the NTF and STF of the modulator. The NTF of this linear model has a complex computation that will be shown during this chapter.

Nevertheless consider a discrete-time system equivalent to the system shown in fig. 1.1. It can be shown that the dynamic range is given by [Car97]

$$DR = \frac{s_o^2}{n_o^2} = \frac{3}{2} \cdot \frac{2n+1}{\pi^{2n}} \cdot \left(2^N - 1\right)^2 \cdot OSR^{2n+1} \qquad (0.1)$$

where

- s_o^2 = power of a full-scale tone
- n_o^2 = quantization noise in-band power

- n = modulator order
- N = quantizer resolution in bits
- OSR = Oversampling ratio

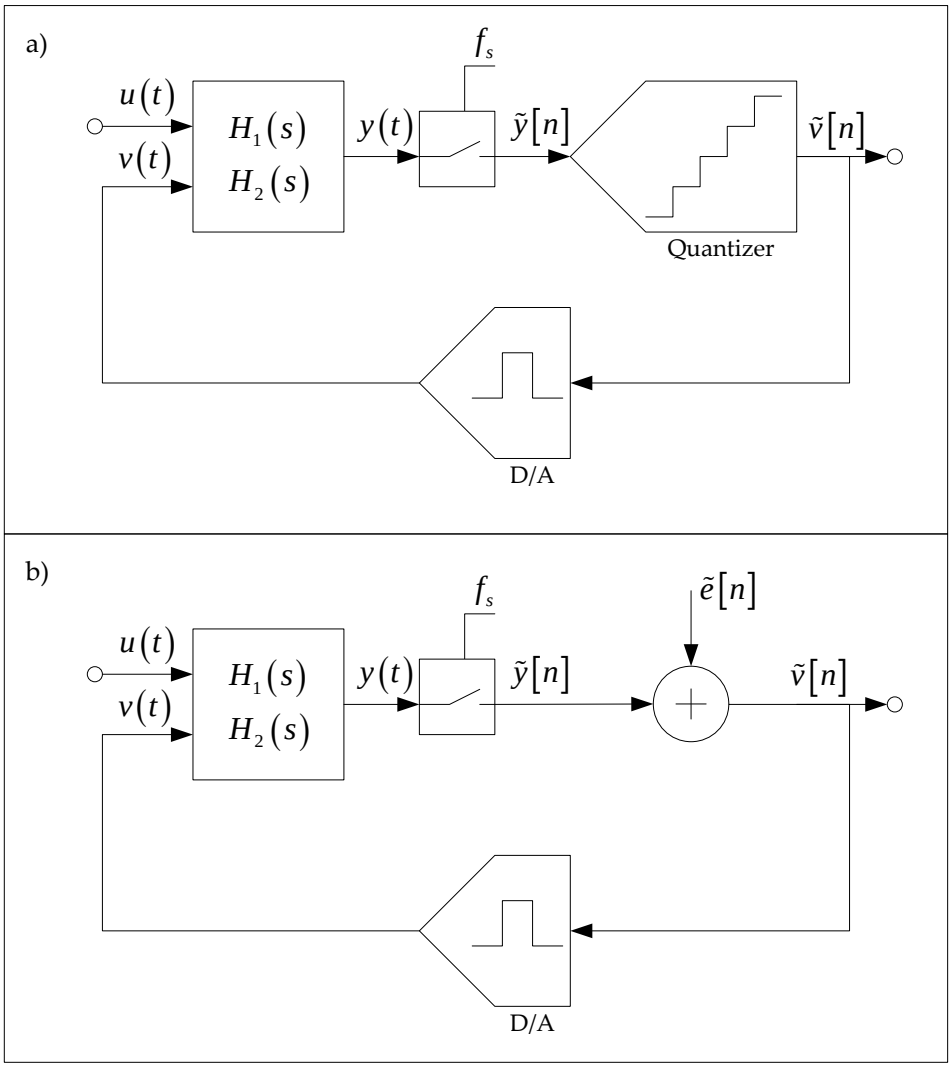

Figure 1.1 CT-SDM Block diagram (a) and its linear model (b)

In an ideal case the dynamic range matches the maximum SNR at the output of a CT-SDM. In practice the maximum SNR is limited by large signal stability.

Equation (0.1) has been obtained assuming the following NTF.

$$N\tilde{T}F(z) = \left(1 - z^{-1}\right)^n \tag{0.2}$$

This NTF corresponds to a filter block composed of a chain of integrators. But the filter block can be implemented with other different strategies, not only with a chain of integrators, as first- and second-order modulators are usually defined.

The design process depends on a proper selection of NTF, which has to be adequate to modulator specifications, and this selection restricts the design of the blocks shown in fig. 1.1.a

1.1 NTF design

There are several publications about CT-SDM design techniques, with different approaches to the analysis of stability, and different approaches to the feasible implementations. This section deals with most common and used methods for the design of CT-SDMs.

There are two main design techniques. One is based on the design of a Discrete-Time Sigma-Delta Modulator (DT-SDM) first, to compute an equivalent CT-SDM afterwards. The other one is based on a full design in continuous-time.

1.1.1 Design technique based on impulse invariance response

This method uses a mathematical transformation to find a CT-SDM that implements the NTF designed in discrete-time domain

The first researcher who used this technique was James C. Candy. The work described in [Can85] has been widely referenced. It is a second order DT-SDM with two feedback paths and, nowadays it is considered as the standard second order Sigma-Delta modulator. Candy uses the impulse invariant method to find an equivalent continuous-time implementation.

There are some other works that use a bilinear transformation [Bro90] or a modified Z -transform [Hor90] in the design of CT-SDMs or in their modeling. In this work we prefer the impulse invariance method because it fits better with the modulator behavior.

The impulse invariance method has been widely applied after the work published in [Can85]. The first works have used some previously well-known DT-SDMs as starting points. Impulse invariance was applied to obtain bandpass CT-SDMs in [Thu91] and [Sch94]. Afterwards R. Schreier proposed a methodology based on impulse invariance in [Sch96]. In that paper the linear blocks of the SDM are described using the state space representation. A similar approach but, without state space representation was followed by [Ben97]. Since that moment, there have been many publications about CT-SDMs. Most of them are summarized in [Che00], which also covers a systematic approach to every linear and non linear aspect of CT-SDMs. Last, [Ger02] adds to the methodology a proposal to select some fundamental parameters of the modulator (order, quantizer resolution, OSR)

Impulse invariance method is based on matching the impulse response of two equivalent systems. Consider the block diagram of a CT-SDM shown in fig. 1.1.a and its open-loop block diagram shown in fig. 1.2.a, where input signal has been removed. The continuous-time open-loop system has a discrete-time equivalent system with matched impulse response at sampling instants, such that

$$Z^{-1}\left\{\tilde{H}_2(z)\right\} = L^{-1}\left\{P(s)\cdot H_2(s)\right\}\Big|_{t=n\cdot T_s} \tag{0.3}$$

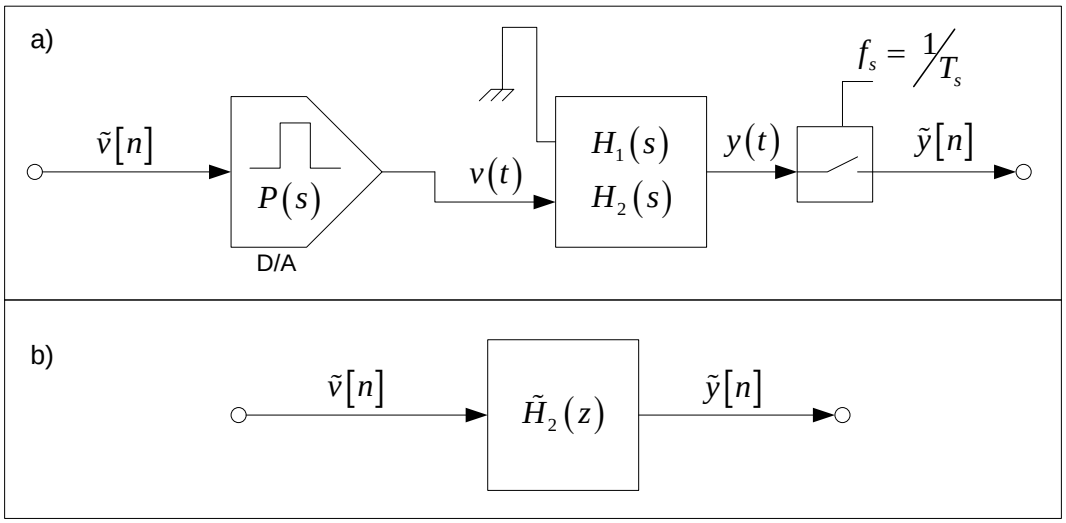

Figure 1.2 CT-SDM open-loop block diagram (a) and DT-SDM open-loop block diagram (b)

The design methodology proposed in [Che00] consists of several steps, as follows:

- Design of a $N\tilde{T}F(z)$ that meets the specifications. The following methods are available:
    - Using a standard or classical modulator
    - Using the method described in [Ada97a], [Sch03]
    - Using CLANS method, described in [Ken93]
    - Using the method described in [Ger02], which takes into account power consumption
- $\tilde{H}_2(z)$ calculation by means of the linear model

$$N\tilde{T}F(z) = \frac{1}{1+\tilde{H}_2(z)} \Rightarrow \tilde{H}_2(z) = \frac{1}{N\tilde{T}F(z)} - 1 \tag{0.4}$$

- D/A pulse type selection and $H_2(s)$ calculation by means of impulse invariance transformation (0.3).
- Architecture selection and computation of its coefficients
- Transient simulation of the architecture in a Spice-like simulator, including linear and non-linear effects.
- $\tilde{H}_2(z)$ extraction from transient simulation by means of impulse invariance transformation, circuit parameters computation and tuning.

1.1.1.1 Sensitivities of the design technique based on impulse invariance

Circuit parameters computation is the main obstacle of this design technique because it is calculated by means of impulse invariance method applied on the result of a transient simulation.

First of all, discrete-time loop-filter ($\tilde{H}_2(z)$) usually has an infinite impulse response, which is a difficulty to numerically apply impulse invariance method. Applying impulse invariance method analytically is feasible but also difficult to implement in practice, except for particular cases.

On the other hand, the modeling of linear and non-linear effects needs to be accurate and the parameters computation has a strong dependency on this accuracy. The result is that the modulator can have a high sensitivity to process variations and/or other non-modeled effects.

Apart from circuit parameters computation, there is another weakness in this design technique. As long as it is based on a discrete-time NTF specification the system is usually optimized for discrete-time purposes, without taking care of some effects that only occurs on continuous-time domain. Excess-loop delay and sampling instant uncertainty are the main effects that usually limit the speed and resolution of CT-SDMs [Che00]. It should be interesting to specify a NTF optimized against these two effects.

1.1.2 Design on continuous-time domain

There is another design technique that is based on specifying a CT-SDM on continuous-time domain only [Bre01]

The technique consist of designing an analog filter, $H_2(s)$, such that

- The system in fig 1.3 is stable. To analyze stability the open-loop root locus is observed.
- The system meets a certain set of specifications (SNR, DR, etc.)

Apart from the above conditions, the design technique also proposes to analyze stability against large signals.

The stability is accomplished by using one of the topologies described in [Bre01] to implement the analog filter. These topologies are the continuous-time counterparts of the topologies described in [Ada97b].

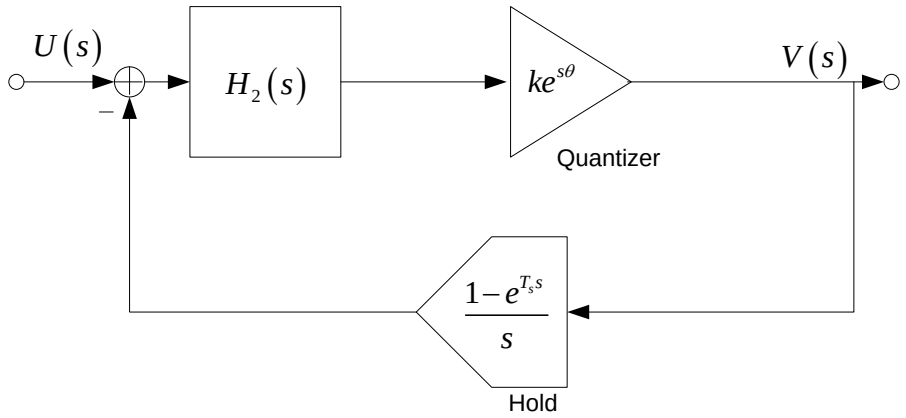

Figure 1.3 Linear model to analyze stability of CT-SDMs according to [Bre01]

1.1.2.1 Disadvantages of the design technique on continuous-time domain

The design technique based on continuous-time domain has two disadvantages as a consequence of the model shown in fig. 1.3.

First of all, the linear model shown in fig. 1.3 is only valid for single-bit CT-SDMs [Hof79].

Second, the model seems to be more adequate for CT-SDMs with high oversampling ratios since it has not included the sampling process that occurs inside the loop.

Apart from the model, the design technique has no reference on how to systematic solve the influence of excess-loop delay and sampling instant uncertainty.

1.1.3 Linear models comparative

This section shows a short comparative of the described design techniques. Each design technique has a linear model that is used to specify and/or analyze the modulator (see fig. 1.4). The comparative study uses both linear models to analyze the same CT-SDM.

We have selected for the comparison two 4th order CT-SDMs with an oversampling ratio of 12 and an excess-loop delay of $50\%T_s$. In both modulators the loop-filter $H_2(s)$ has same DC-gain and pole locations. One modulator has 3 zeros so that the initial value of $H_2(s)$, $h_2(0)$, is bounded. The other modulator has the same 3

zeros plus one extra zero, such that $h_2(0) \to \infty$. The latter modulator corresponds to a modulator compensated for excess-loop delay while the former one is uncompensated [Che00, Luh00].

The selected CT-SDMs has been simulated using an ideal loop-filter, a null input signal and a random noise source (band-limited and with uniform distribution between $\pm 1/\left(2^N - 1\right)$) added at quantizer input. The output spectrum is compared with a computed power spectrum density. The computed spectrum comes from considering each one of the models described before with quantization error as the only input to the system.

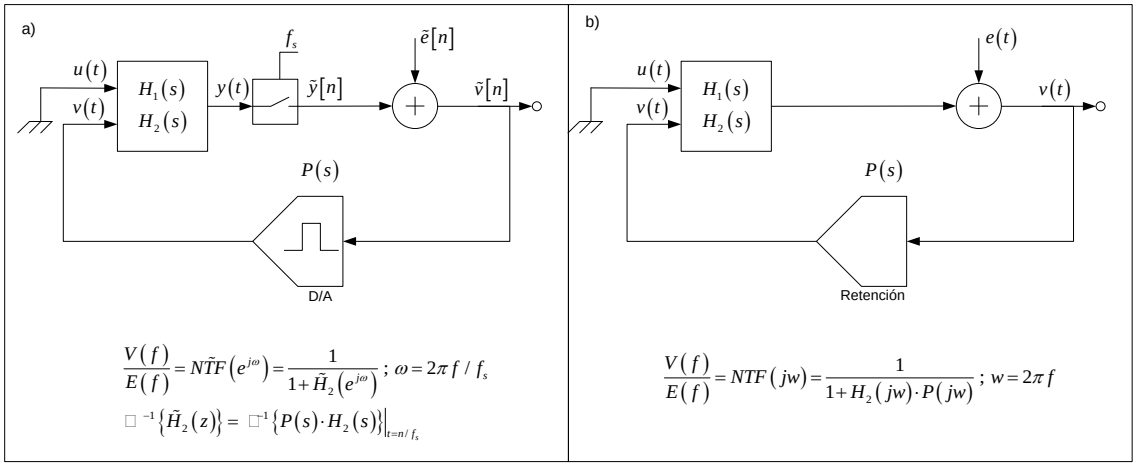

Figure 1.4 Linear models considered in the comparative. a) Design technique based on impulse invariance. b) Design in continuous-time domain

When the modulator has a loop-filter with bounded $h_2(0)$, both models match roughly inside the range $0 \le f \le f_s/2$. But when $h_2(0) \to \infty$, each model gives a different result.

Figures 1.7 and 1.8 show that none of the models fit with transient simulations. It is supposed that impulse invariance model fits better with simulation for low oversampling ratios and the opposite for high oversampling ratios.

The selected modulators are unstable with single-bit quantizers. This behavior is predicted by impulse invariance model because discrete-time NTF does not follow Lee rule [Nor97].

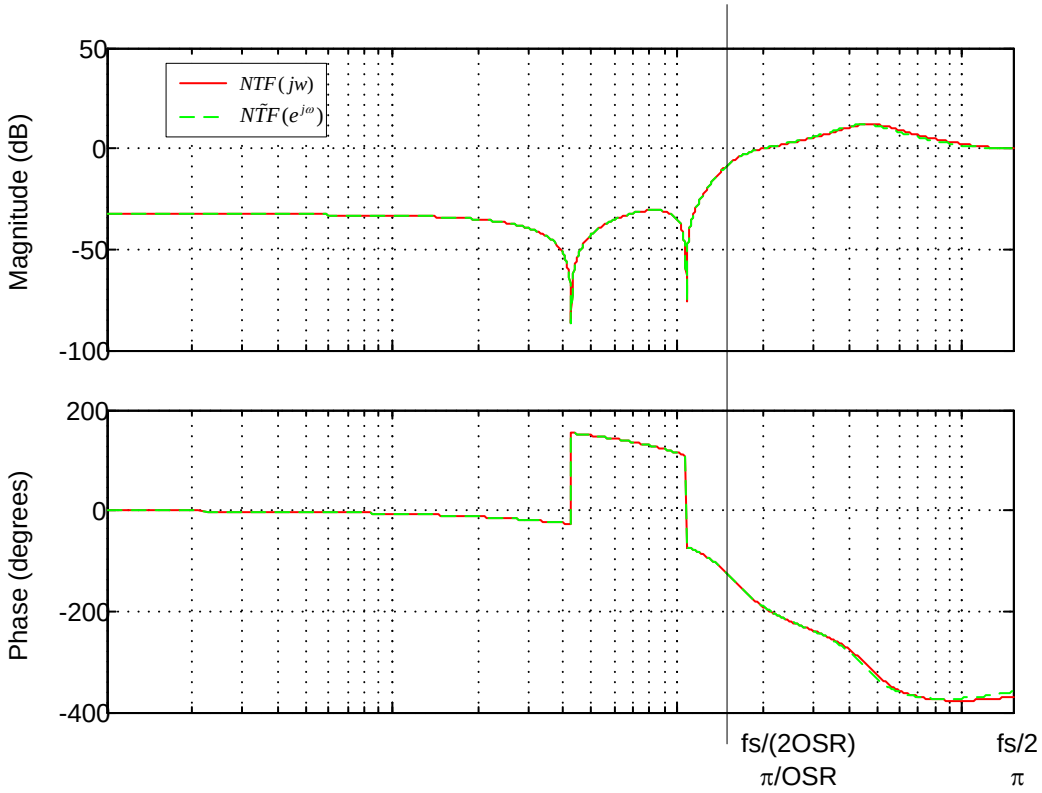

Figure 1.5 Comparison between models when $h_2(0) < C$

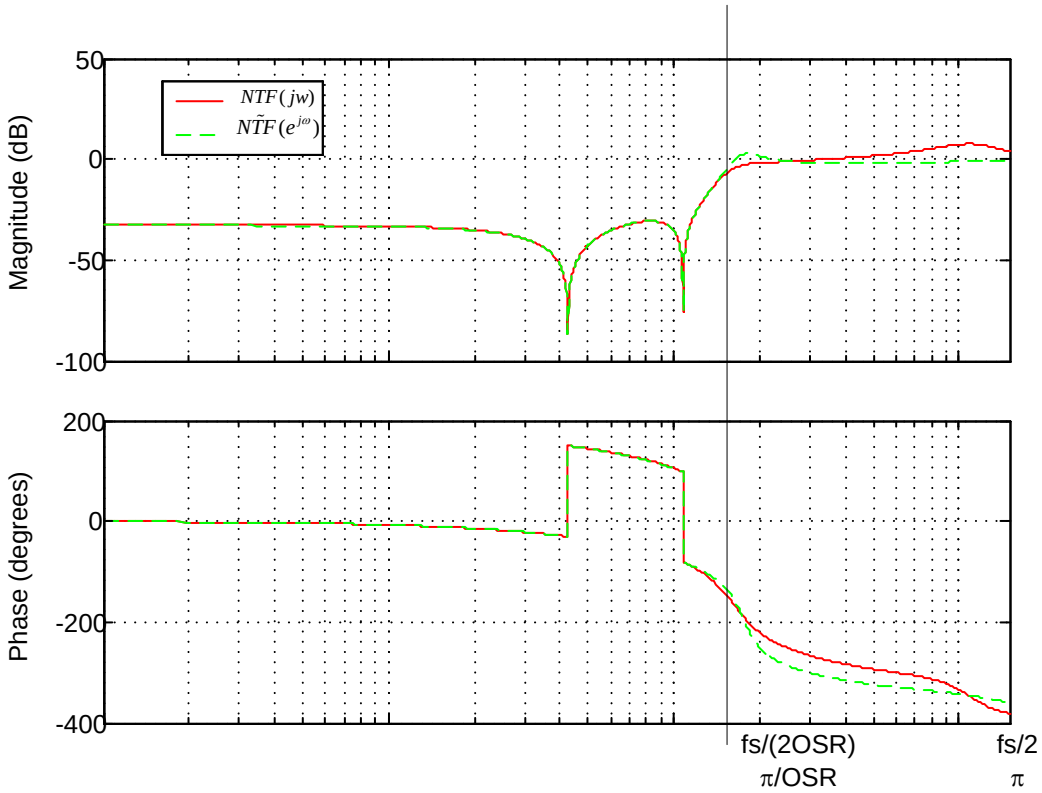

Figure 1.6 Comparison between models when $h_2(0) \to \infty$

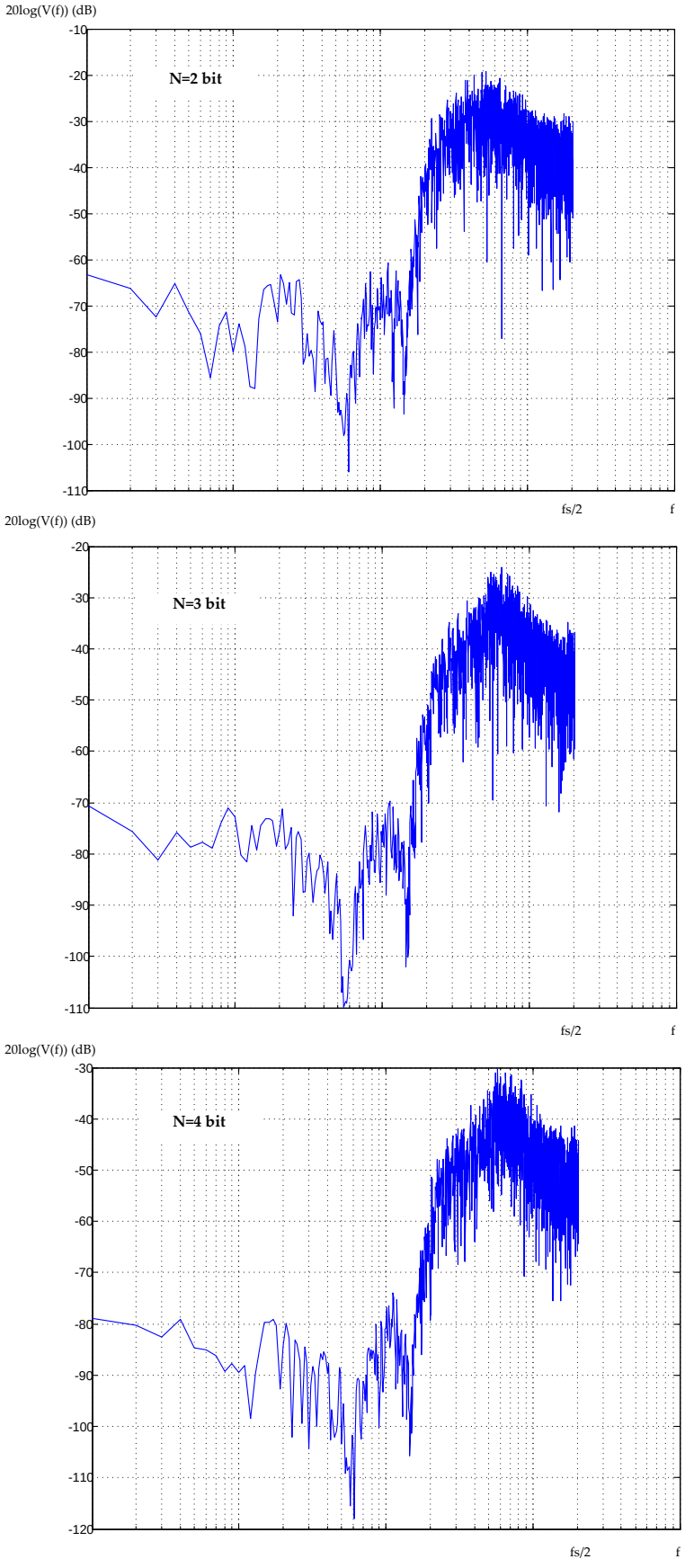

Figure 1.7 Transient simulations of $h_2(0) < C$ *modulator with several quantizer resolutions*

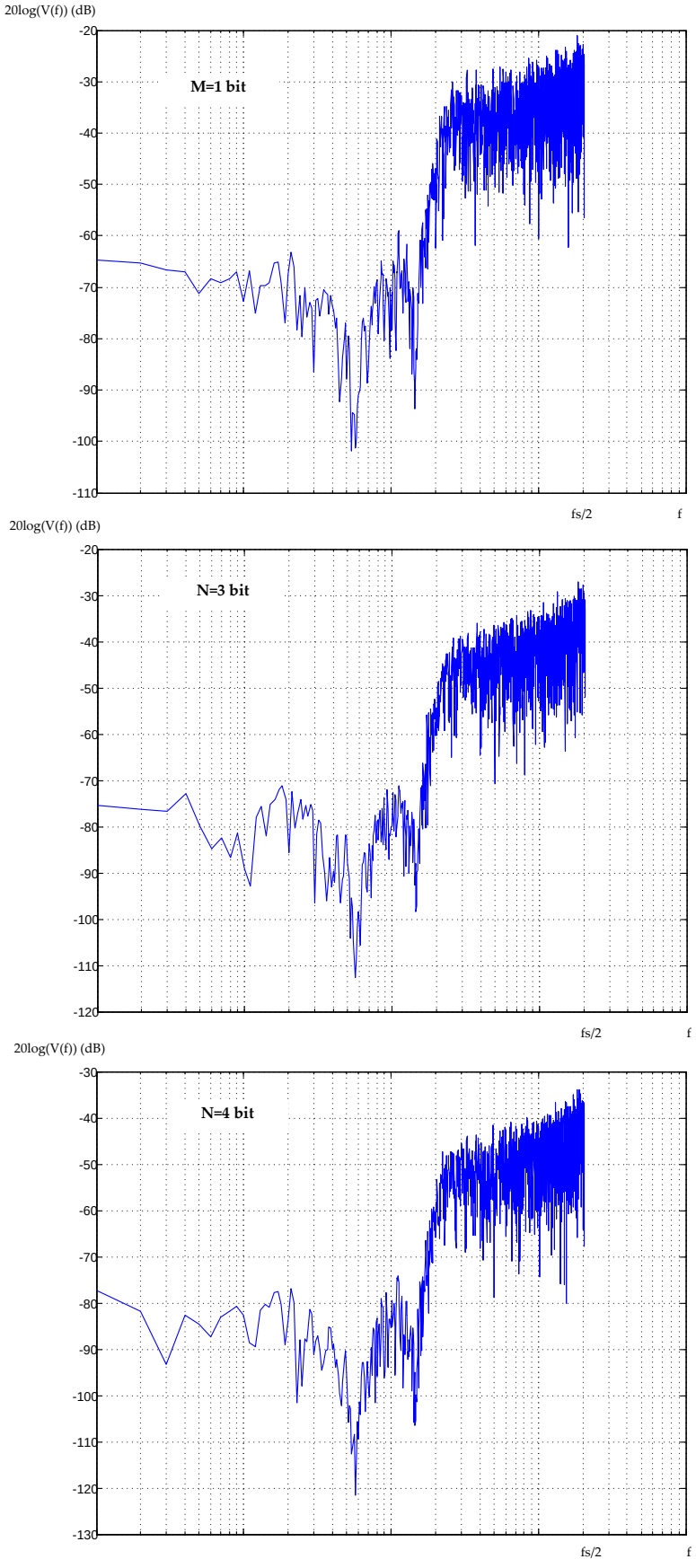

Figure 1.8 Transient simulations of $h_2(0) \to \infty$ *modulator with several quantizer resolutions*

1.2 Loop-filter topologies

Loop-filter topology selection is a design step, no matter the employed design technique. Normally, a certain topology is chosen according to hardware restrictions, power consumption, and distortion and noise considerations. This section does not collect all these restrictions; some of them are given in chapter **¡Error! No se encuentra el origen de la referencia.**, with an application example. Instead of collecting all these restrictions, this chapter gives a general approach to loop-filter implementation possibilities.

1.2.1 State-space description

Grey block shown in fig. 1.9 is a two-inputs one-output linear system with transfer functions $H_1(s)$ and $H_2(s)$. This linear system can be described by means of its state-space equations, as follows,

$$\begin{pmatrix} \dot{x}_1 \\ \vdots \\ \dot{x}_n \end{pmatrix}(t) = \overbrace{\begin{pmatrix} A_{11} & \cdots & A_{1n} \\ \vdots & \ddots & \vdots \\ A_{n1} & \cdots & A_{nn} \end{pmatrix}}^{A} \cdot \begin{pmatrix} x_1 \\ \vdots \\ x_n \end{pmatrix}(t) + \overbrace{\begin{pmatrix} B_{11} & B_{12} \\ \vdots & \vdots \\ B_{n1} & B_{n2} \end{pmatrix}}^{B} \cdot \begin{pmatrix} u \\ -v \end{pmatrix}(t)$$
$$y(t) = \underbrace{\begin{pmatrix} C_1 & \cdots & C_n \end{pmatrix}}_{C} \cdot \begin{pmatrix} x_1 \\ \vdots \\ x_n \end{pmatrix}(t) + \underbrace{\begin{pmatrix} D_1 & D_2 \end{pmatrix}}_{D} \cdot \begin{pmatrix} u \\ -v \end{pmatrix}(t) \tag{0.5}$$

where n is modulator order and $x_i(t)$ is the i-th state variable.

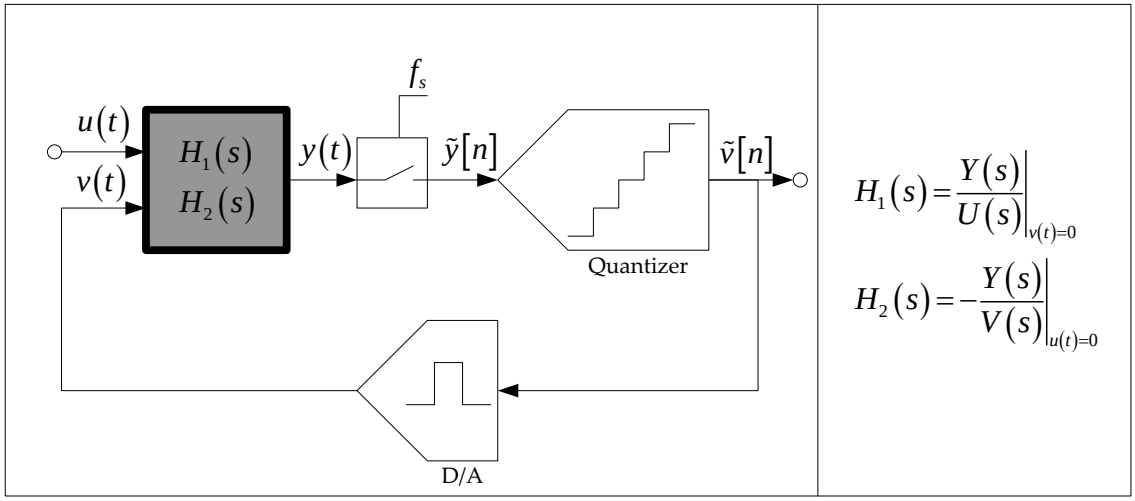

Figure 1.9 CT-SDM Block diagram

State-space description can be summarized in an extended ABCD matrix of size $(n+1)\cdot(n+2)$.

$$ABCD=\left(\begin{array}{c|c} A & B \\ \hline C & D \end{array}\right)=\left(\begin{array}{ccc|cc} A_{11} & \cdots & A_{1n} & B_{11} & B_{12} \\ \vdots & \ddots & \vdots & \vdots & \vdots \\ A_{n1} & \cdots & A_{nn} & B_{n1} & B_{n2} \\ \hline C_1 & \cdots & C_n & D_1 & D_2 \end{array}\right) \tag{0.6}$$

Applying Laplace transformation on (0.5) and after some manipulations, transfer functions can be expressed as

$$\begin{cases} H_1(s)=C\cdot(sI-A)^{-1}\cdot\begin{pmatrix} B_{11} \\ \vdots \\ B_{n1} \end{pmatrix}+D_1 \\ H_2(s)=C\cdot(sI-A)^{-1}\cdot\begin{pmatrix} B_{12} \\ \vdots \\ B_{n2} \end{pmatrix}+D_2 \end{cases} \tag{0.7}$$

Equation (0.7) shows that NTF zeros, i.e. $H_2(s)$ poles, are given by matrix A eigenvalues.

The system described by (0.5) may be implemented with n integrators and n^2+3n+2 coefficients at most. As long as transfer functions have n poles, the system is defined with a minimum of different $3n+2$ coefficients [Der90].

There are an infinite number of implementations of a unique transfer function. Each implementation corresponds to a certain state-space, given by

$$\vec{x}(t) = \begin{pmatrix} x_1 \\ \vdots \\ x_n \end{pmatrix}(t) \tag{0.8}$$

There is a non-singular n-size T transformation matrix for each implementations pair $\vec{x}$ and $\vec{w}$ such that

$$\begin{aligned} &\vec{w}(t) = T \cdot \vec{x}(t) \qquad / \left|T\right| \neq 0 \\ &\begin{cases} \dot{\vec{w}}(t) = T \cdot A \cdot T^{-1} \cdot \vec{w}(t) + T \cdot B \cdot \begin{pmatrix} u \\ -v \end{pmatrix}(t) \\ y(t) = C \cdot T^{-1} \cdot \vec{w}(t) + D \cdot \begin{pmatrix} u \\ -v \end{pmatrix}(t) \end{cases} \end{aligned} \tag{0.9}$$

State-space selection depends on practical restrictions:

- STF and/or anti-aliasing filter specification
- Quantizer resolution
- Power consumption
- Harmonic distortion specification

1.2.2 Particular case: chain of integrators

Consider a low-pass CT-SDM. There are two choices to select A eigenvalues, i.e. NTF zeros. They may be all located at zero frequency or they may be spread over modulator bandwidth.

If A eigenvalues are all zero, the simplest implementation is a chain of integrators. But, if A eigenvalues are all different between them and different from zero, there are more options to implement the linear system, for example with a parallel structure [Der90]

All reported CT-SDMs have topologies based on a chain of integrators, maybe because DT-SDMs also have the same kind of topologies. The main advantage of an architecture consisted on a chain of integrators is the connection between hardware

and state-space equations, supposed that every integrator output corresponds to a state variable. The main disadvantage is that the linearity of first stages has a strong influence on output signal. However, in theory, all known continuous-time filter implementations are available. Using biquads, for example, may be justified if its usage reduces power consumption, simplifies design process and/or reduces distortion.

Focusing on topologies based on a chain of integrators it can be defined the family of architectures shown in fig. 1.10. According to this family it is possible to define any designed $H_1(s)$ and $H_2(s)$. If A eigenvalues are all different from zero, local feedbacks between integrators are needed [Der90].

Consider that A eigenvalues are zero or complex conjugate pairs only. A linear system with pure complex poles is an oscillator. In the other hand two integrators of gains c_1 and c_2, connected in cascade, and feedback by means of a gain g, form an oscillator with resonance frequency $\sqrt{c_1 \cdot c_2 \cdot g}$

The ABCD matrix of this family is defined according to three cases: even order, odd order with a resonator as first stage ($1R$), and odd order with an integrator as first stage ($1I$). The cases where A eigenvalues are all zero are particular cases among the above.

$$ABCD_{n\ even} = \left(\begin{array}{ccccc:cc} 0 & -g_1 \cdot c_1 & & \cdots & 0 & b_1 \cdot c_1 & a_1 \cdot c_1 \\ c_2 & 0 & 0 & & \vdots & & \\ & \ddots & 0 & \ddots & & \vdots & \vdots \\ \vdots & & \ddots & 0 & -g_{(n/2)} \cdot c_{(n-1)} & & \\ 0 & \cdots & & c_n & 0 & b_n \cdot c_n & a_n \cdot c_n \\ \hdashline d_1 & & \cdots & & d_n & b_{(n+1)} & fbe \end{array}\right) \tag{0.10}$$

$$ABCD_{n\ odd}^{1R} = \left(\begin{array}{ccccc:cc} 0 & -g_1 \cdot c_1 & & \cdots & 0 & b_1 \cdot c_1 & a_1 \cdot c_1 \\ c_2 & 0 & 0 & & \vdots & & \\ & \ddots & 0 & \ddots & & \vdots & \vdots \\ \vdots & & \ddots & 0 & 0 & & \\ 0 & \cdots & & c_n & 0 & b_n \cdot c_n & a_n \cdot c_n \\ \hdashline d_1 & & \cdots & & d_n & b_{(n+1)} & fbe \end{array}\right) \tag{0.11}$$

$$ABCD_{n\,odd}^{1I} = \left(\begin{array}{ccccc:cc} 0 & 0 & & \cdots & 0 & b_1 \cdot c_1 & a_1 \cdot c_1 \\ c_2 & 0 & -g_1 \cdot c_2 & & \vdots & & \\ & \ddots & 0 & \ddots & & \vdots & \vdots \\ \vdots & & \ddots & 0 & -g_{(n-1)/2} \cdot c_{(n-1)} & & \\ 0 & \cdots & & c_n & 0 & b_n \cdot c_n & a_n \cdot c_n \\ \hdashline d_1 & & \cdots & & d_n & b_{(n+1)} & fbe \end{array}\right) \tag{0.12}$$

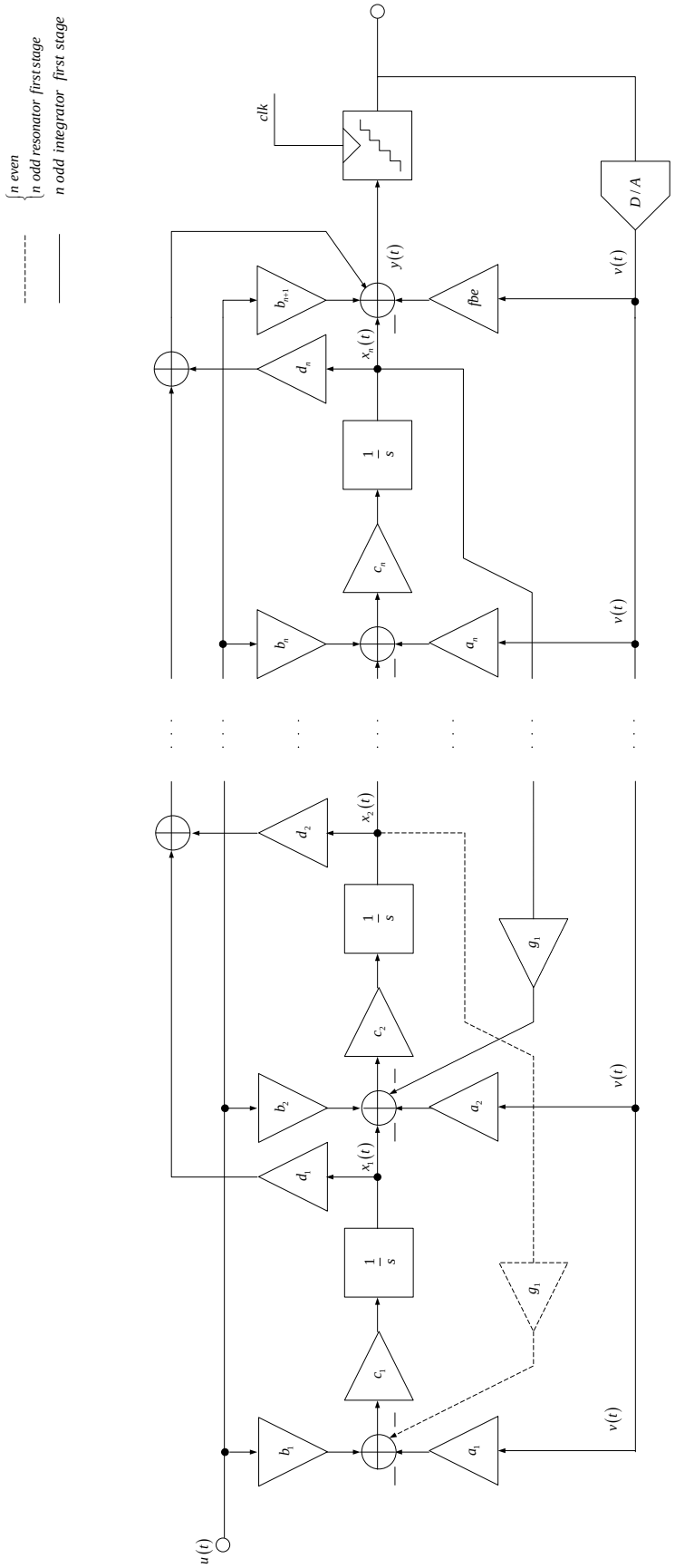

Figure 1.10 CT-SDM Generic architecture based on a chain of integrators

The family of architectures shown in fig. 1.10 has only one D/A converter in the feedback path. In practice there will be one D/A converter per feedback branch, i.e., per each a_i and fbe coefficient.

Input feedforward coefficients, b_i, only have influence on $H_1(s)$, and therefore they only have influence on STF. Feeding the input through these coefficients usually helps to decrease distortion because of the reduction of the dynamic range of state variables. There is a particular case where STF is exactly 1, that is when $b_i = a_i$. Rest of coefficients has influence on both STF and NTF. The usual approach is to implement NTF zeros, i.e. $H_2(s)$ poles, by means of a_i or d_i coefficients. Sometimes it is useful to use both type of coefficients, feedback a_i and feedforward d_i, to increase the degrees of freedom of the system, such that a certain STF can be implemented.

Some particular cases of this family of architectures are described in chapter 7. Notice that standard or canonical forms of describing linear systems are not included in this family of architectures [Oga95], [Mor03].

1.3 Simulation methods. CAD tools.

This section summarizes most common and used design- and simulation-tools at system-level. The summary is focused on specific tools for CT-SDMs. Circuit-level tools are excluded, like Spice, because they are not specific for Sigma-Delta modulators.

The most referenced tool is *'delsig'* Matlab library [Sch03].The functions included in this library are dedicated to DT-SDMs design and simulation. Some functions are originally written in C and then compiled, which reduces CPU time. There are some functions dedicated to architecture selection, among the choices described in [Ada97b]. Some of them use impulse invariant method to obtain bandpass continuous-time topologies, with LC resonators.

One of the problems of all tools dedicated to Sigma-Delta modulators design is transient simulation. Transient simulation is always needed when a Sigma-Delta modulator is designed, even if a linear model is used in the first steps of design. Transient simulation guarantees stability and allows system characterization. In a DT-SDM case, simulation time is proportional to modulator order and the number of samples, as long as the problem to solve is based on difference equations. In a CT-SDM case, the simulator has to numerically solve a set of partial derivative equations, such that a variable integration step is needed. When signal changes quickly, as in a falling or rising clock edge, integration step has to be small, such that simulation time increases. Simulation time can be very large depending on which effects are modeled, such as sampling instant uncertainty, for example. The same phenomenon occurs when some circuit non-linearities are modeled in DT-SDM design.

For the particular case of DT-SDMs design, [Mal03] has solved the problem by means of modeling a wide range of effects at system-level, such that circuit simulators are not longer needed.

In CT-SDM design there are some possibilities to reduce simulation time. One simple solution is to use a compliable code, like ANSI-C, for modeling. Compared to Simulink (Matlab) models or Spice models, C-compiled models are more efficient and less time consuming. The problem of this approach is the low flexibility of the model. For example, adding a block to an existing model may yields to rebuild the entire model. However, Simulink allows to build C-coded and –compiled blocks. This feature has been used in [Med95] and [Rui03] to model operational amplifiers, samplers and quantizers among other blocks with some non-linearities included in the model. Each block has a state-space description in C while Simulink has an adequate solver. This solution is efficient but requires a large block library with many modeled effects.

Another solution in order to decrease simulation time is to use a discrete model by means of a continuous-time to discrete-time mapping, such as impulse invariance method. This solution has been adopted in [Che98], [Bro90] and [Hor90]. The main difficulty of this approach is the modeling of non-idealities, as sampling

instant uncertainty, for example. However this approach is the most efficient in terms of CPU time. Behavioral simulator shown in [Fran02] is an intermediate solution between using a continuous-time to discrete-time mapping and using a compiled code.

Chapter 2

Analysis and modeling of excess-loop delay and clock jitter in CT-SDMs

This chapter is dedicated to the analysis and modeling of the main effects that contribute to performance degradation in a CT-SDM, i.e. excess-loop delay and clock jitter. The proposed design methodology (see chapter 3) uses the models included in this chapter.

2.1 Excess-loop delay

There is a delay inside the loop of a CT-SDM that is not present in a DT-SDM, between sampling instant and the instant where D/A output is updated as a consequence of sampling.

Consider the block diagram shown in fig. 2.1. The quantizer is composed of one or several latched comparators. Comparators output controls one or several D/A converters. Consider each D/A converter consisted of current steering sources. In an ideal case output current changes with clock edge. In practice, transistors inside comparators and D/As cannot switch instantaneously and therefore there is a delay in the feedback loop, which is called *Excess-Loop Delay (ELD)*.

ELD has been widely analyzed by many researchers. One of the most detailed and extensive contribution is written in [Che00, chapter 4]. It also includes a wide reference list.

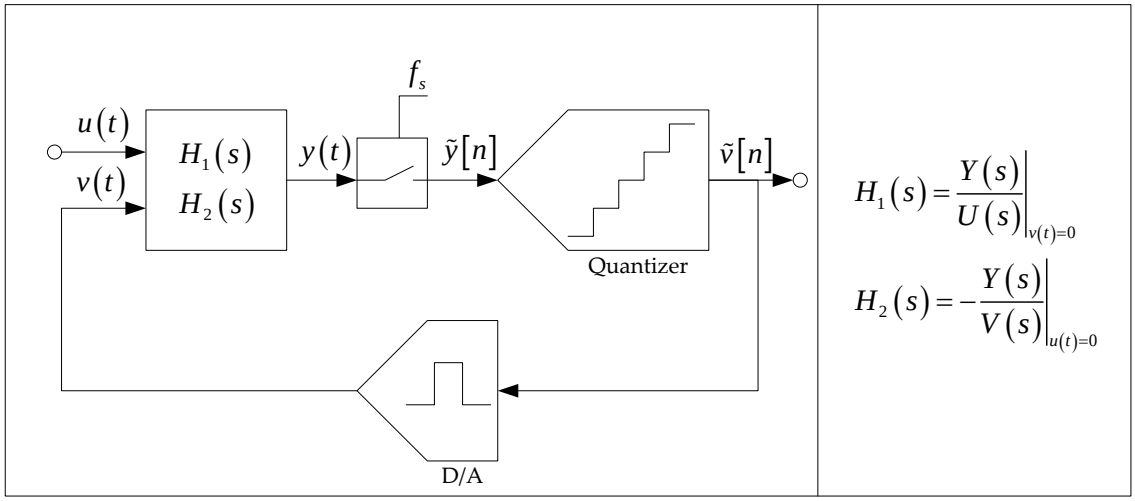

Figure 2.1 CT-SDM Block diagram

ELD usually increases CT-SDM instability and therefore decreases maximum achievable resolution.

This section is dedicated to the analysis and modeling of ELD effect on low OSR CT-SDMs. Impulse invariance principle and discrete-time root-locus have been used for these purposes.

Consider the block diagram shown in fig. 2.2, where there are two blocks inserted, one block to model ELD in Laplace domain, as a pure delay, and another block to model an ideal D/A converter in Laplace domain, as a pulse shaper. Quantizer is assumed to be ideal as well, i.e. it switches instantaneously. ELD block has been placed after pulse shaping because it is easy to model a delay in Laplace domain and the behavior is completely equivalent to what happen in practice.

Impulse response of feedback branch, i.e. ideal D/A converter and ELD block, is shown in fig. 2.3, where a rectangular pulse has been assumed for D/A converter. If the rectangular pulse starts on $t = 0$, D/A impulse response is

$$p_{\{\alpha,\beta\}}(t) = \begin{cases} 1, & \alpha \le \frac{t}{T_s} < \beta, \quad 0 \le \alpha < \beta \le 1 \\ 0, & rest \end{cases} \tag{2.1}$$

After applying Laplace transformation it yields

$$P_{\{\alpha,\beta\}}(s) = \frac{e^{-(\alpha \cdot T_s)\cdot s} - e^{-(\beta \cdot T_s)\cdot s}}{s} \tag{2.2}$$

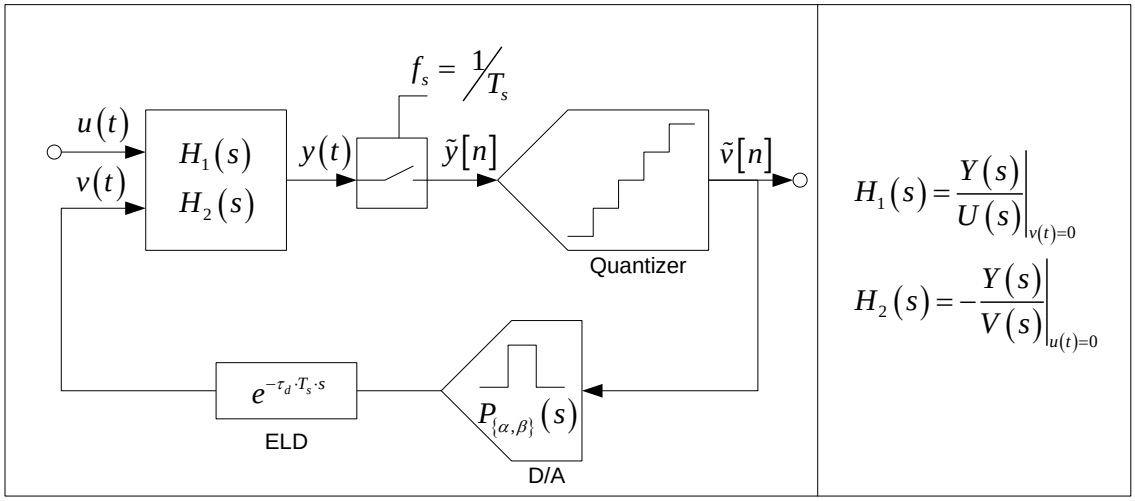

Figure 2.2 CT-SDM Extended block diagram

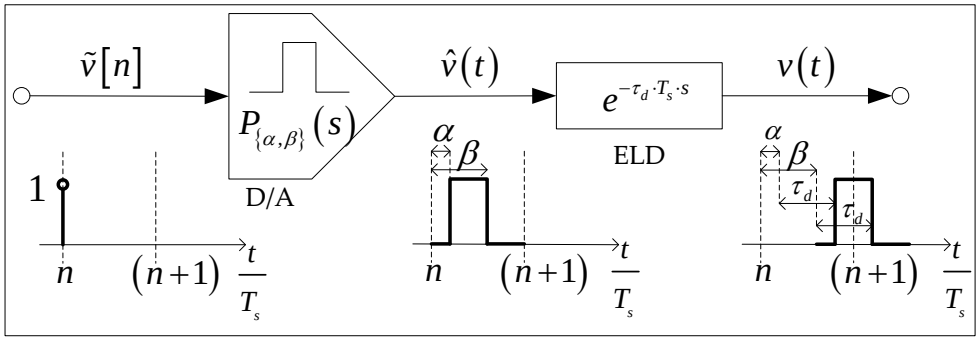

Figure 2.3 Feedback loop impulse response (D/A and ELD)

Pulse type is modeled by α and β. For instance, a Non-Return-to-Zero (NRZ) D/A may be modeled with $\alpha = 0$ and $\beta = 1$.

ELD effect on a CT-SDM may be analyzed by monitoring its equivalent discrete-time counterpart. Figure 2.4 shows the open loop block diagram corresponding to the system shown in fig. 2.2 together with a linear discrete-time system. Applying impulse invariance method on both systems yields

$$Z^{-1}\left\{\tilde{H}_2(z)\right\} = L^{-1}\left\{PD_{\{\alpha,\beta,\tau_d\}}(s)\cdot H_2(s)\right\}\Big|_{t=n\cdot T_s} \tag{2.3}$$

where

$$PD_{\{\alpha,\beta,\tau_d\}}(s) = L\left\{p_{\{a,\beta\}}(t-\tau_d\cdot T_s)\right\} = P_{\{\alpha,\beta\}}(s)\cdot e^{-(\tau_d\cdot T_s)\cdot s} \tag{2.4}$$

This equation may be split in several terms, one per each sample where $p_{\{a,\beta\}}(t-\tau_d\cdot T_s)$ is present. As long as $0 \le \alpha < \beta \le 1$, the delayed pulse

$p_{\{\alpha,\beta\}}(t-\tau_d \cdot T_s)$ will last two samples only, as is shown in fig. 2.5. According to this fact, delayed pulse is split in two samples as follows

$$PD_{\{\alpha,\beta,\tau_d\}}(s) = P_{\{\alpha',1\}}(s) + P_{\{0,\beta'\}}(s)\cdot e^{-T_s\cdot s}$$

where (2.5)

$$\begin{cases}\alpha' = \alpha + \tau_d \\ \beta' = \beta + \tau_d - 1\end{cases}$$

where an ELD lower than one sampling period has been assumed, i.e. $\tau_d \leq 1$, although the model is extensible to higher ELD.

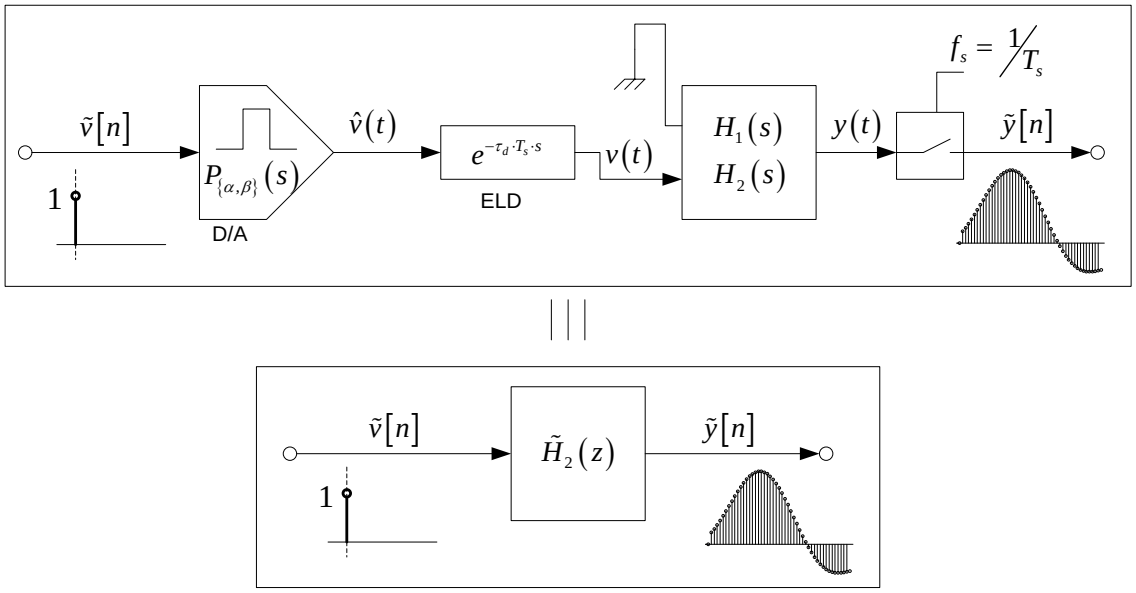

Figure 2.4 CT-SDM Open loop block diagram and its equivalent discrete-time counterpart

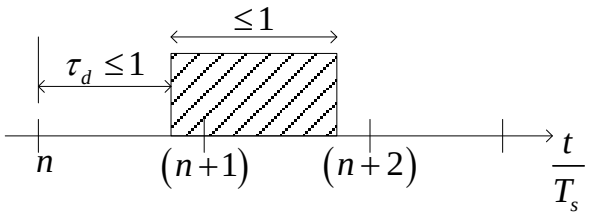

Figure 2.5 Example of a delayed D/A impulse response

Therefore, discrete-time system in fig. 2.4 is composed also of two terms, as follows

$$\tilde{H}_{2_{\{\tau_d,\alpha,\beta\}}}(z)=\tilde{H}_{2_{1\{\alpha'\}}}(z)+z^{-1}\cdot\tilde{H}_{2_{2\{\beta'\}}}(\beta',z)$$

where

$$Z^{-1}\left\{\tilde{H}_{2_{1\{\alpha'\}}}(z)\right\}=L^{-1}\left\{P_{\{\alpha',1\}}(s)\cdot H_2(s)\right\}\Big|_{t=n\cdot T_s} \tag{2.6}$$

$$Z^{-1}\left\{\tilde{H}_{2_{1\{\alpha'\}}}(z)\right\}=L^{-1}\left\{P_{\{\alpha',1\}}(s)\cdot H_2(s)\right\}\Big|_{t=n\cdot T_s}$$

This discrete-time system may be analyzed in close-loop configuration, such that discrete-time NTF yields

$$N\tilde{T}F(z)=\frac{1}{1+\tilde{H}_{2_{\{\tau_d,\alpha,\beta\}}}(z)}=\frac{1}{1+\tilde{H}_{2_{1\{\alpha'\}}}(z)+z^{-1}\cdot\tilde{H}_{2_{2\{\beta'\}}}(z)} \tag{2.7}$$

And NTF zeros z_k are given by

$$z_k=\left\{0,e^{s_k}\right\} \tag{2.8}$$

where s_k are $H_2(s)$ poles.

Zero located at $z=0$ appears because part of D/A pulse is overlapping next sample time-gap. That zero increases modulator order and modifies modulator stability, while in-band quantization-noise power is unaffected. At the same time, NTF poles are also modified as a consequence of ELD.

Consider a second-order CT-SDM as an example, like the one shown in fig. 2.6, which has been reported before in [Can85, Cha90, Che00]. According to the model shown in fig. 2.2, loop-filter turns out to be

$$H_2(s)=\frac{1}{2}\cdot\frac{2+3\cdot(T_s\cdot s)}{(T_s\cdot s)^2} \tag{2.9}$$

An equivalent discrete-time NTF may be computed by means of impulse invariance method and considering a NRZ D/A and a certain ELD, using (2.6) and (2.7). Figure 2.7 shows discrete-time root-locus of closed-loop system when ELD varies form 0 to T_s.

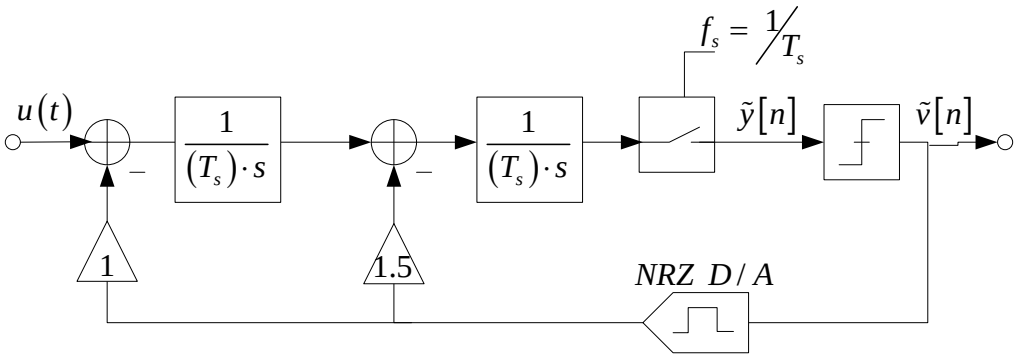

Figure 2.6 Second-order CT-SDM block diagram

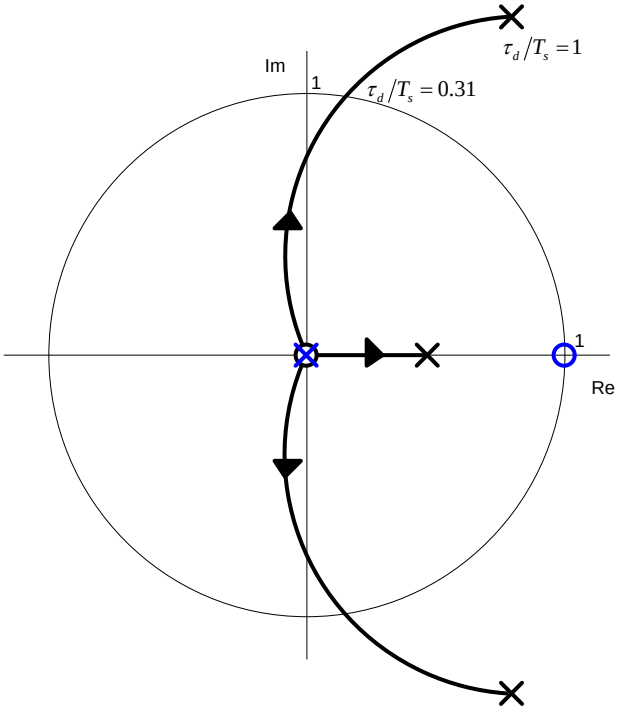

Figure 2.7 $N\tilde{T}F(z)$ *Root-locus as a function of* τ_d*, where continuous-time loop-filter is given by (2.9)*

When ELD is higher than 31% (over a sampling period), NTF poles are outside the unit circle. However, if the modulator is simulated in idle-channel, output spectrum shows limit cycles when ELD is higher than 52%.

Linear analysis does not guarantee stability, but may be improved by adding to the model the quantizer gain [Ard87].

Another example is shown in fig. 2.8, where $N\tilde{T}F(z)$ root-locus is depicted for the CT-SDM shown in fig. 2.9 and transfer functions given by (2.10). This particular case is a 3rd order 3-bit CT-SDM with OSR=64. The modulator has been designed

according to the method reported later in chapter 7. NTF zeros are spread over analog input bandwidth according to [Ada97a]. Figure 2.8 shows that NTF poles are outside the unit circle when ELD is higher than 46%. If the modulator in fig. 2.9 is simulated in idle channel, output spectrum shows limit cycles when ELD is higher than 40%. The same simulation with 1-bit quantizer instead of 3-bit quantizer shows instability for every ELD. With 2-bit or 4-bit quantizer, simulations show the same limit ELD, 40%.

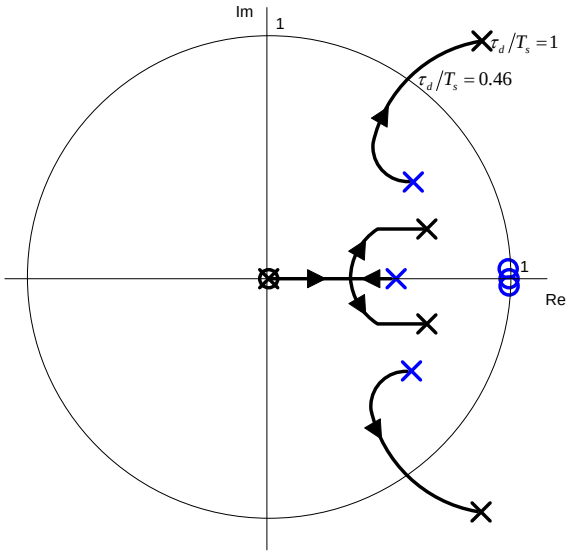

Figure 2.8 $N\tilde{T}F(z)$ *Root-locus as a function of* τ_d*, where continuous-time loop-filter is given by (2.9) and the corresponding CT-SDM is shown in fig. 2.9*

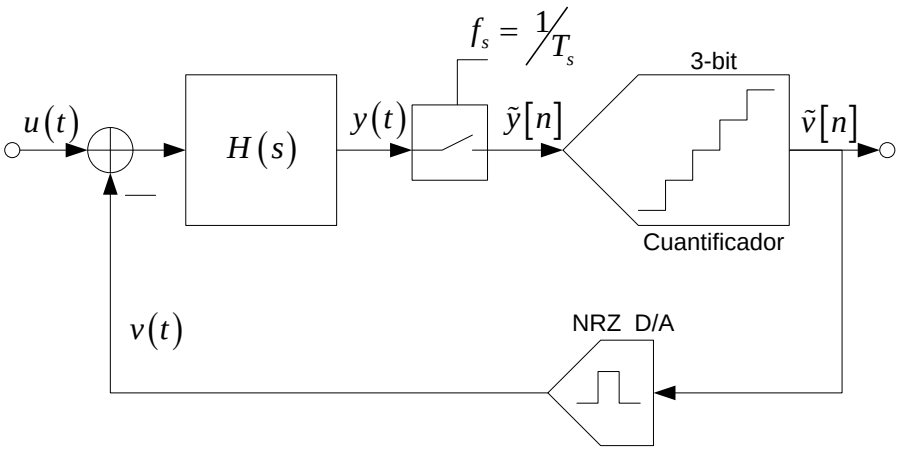

Figure 2.9 CT-SDM Block diagram corresponding to (2.10).

$$\begin{cases} Oversampling\ \ ratio = 64 \\ H(s) = \dfrac{1.013(T_s)^2 s^2 + 0.5791(T_s)s + 0.1619}{(T_s)^3 s^3 + 0.0015(T_s)s} \\ P_{\{\alpha,\beta\}}(s) = \dfrac{1 - e^{-T_s \cdot s}}{s} \end{cases} \tag{2.10}$$

The same modulator has been redesigned for an OSR of 16. Its transfer functions are given by (2.11). NTF root-locus is shown in fig. and as can be seen is approximately the same root-locus that is depicted in fig. 2.8. If the modulator in fig. 2.9 is simulated in idle-channel, output spectrum shows limit cycles when ELD is higher than 33%. The same simulation with 1-bit quantizer instead of 3-bit quantizer shows instability for every ELD. With 2-bit and 4-bit quantizer, simulations show limit ELDs of 30% and 33% respectively.

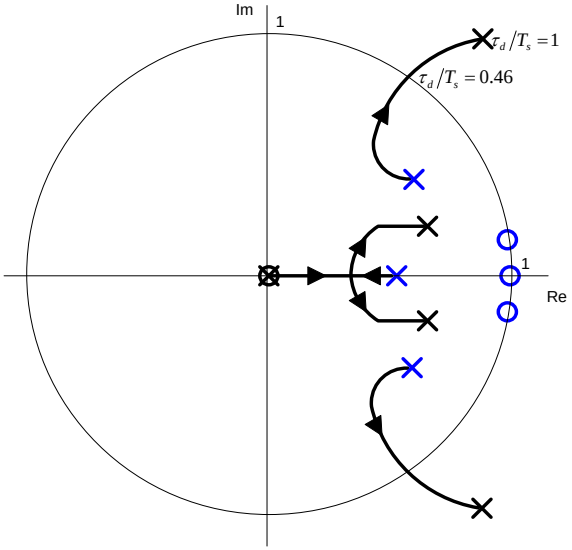

Figure 2.10 $N\tilde{T}F(z)$ *Root-locus as a function of* τ_d*, where continuous-time loop-filter is given by (2.11) and the corresponding CT-SDM is shown in fig. 2.9*

$$\begin{cases} Oversampling\ \ ratio = 16 \\ H(s) = \dfrac{1.012(T_s)^2 s^2 + 0.5653(T_s)s + 0.165}{(T_s)^3 s^3 + 0.0231(T_s)s} \\ P_{\{\alpha,\beta\}}(s) = \dfrac{1 - e^{-T_s \cdot s}}{s} \end{cases} \tag{2.11}$$

2.1.1 ELD analysis by means of analog phase margin

Root-locus gives a sufficient condition to predict stability but is not a necessary condition, as is shown above through some examples. The system may be unstable although all NTF poles are inside the unit circle. In addition, a CT-SDM with low OSR is unstable for a lower ELD than a CT-SDM with high OSR, even when both modulators has been designed using the same criteria. We need a figure of merit to, compare the sensitivity to ELD of several modulators, and at the same time, predict stability.

Consider analog phase margin of the system $H_{olp}(s) = PD_{\{\alpha,\beta,\tau_d\}}(s) \cdot H_2(s)$ as a parameter useful to compare ELD sensitivity.

When NRZ D/A is used, i.e. $\alpha = 0$ and $\beta = 1$, then

$$H_{olp}(s) = H_2(s) \cdot \frac{1 - e^{-T_s \cdot s}}{s} \cdot e^{-(\tau_d \cdot T_s) \cdot s} \tag{2.12}$$

And therefore

$$\begin{cases} \left|H_{olp}(j\omega)\right| = \left|H_2(j\omega)\right| \cdot \mathrm{sinc}\left(\dfrac{\omega}{2}\right) \\ \phi\left\{H_{olp}(j\omega)\right\} = \phi\left\{H_2(j\omega)\right\} - \left(\tau_d + \dfrac{1}{2}\right) \cdot \omega \\ \omega \in [0, 2\pi] \end{cases} \tag{2.13}$$

where

$$H_{olp}(jw) = \left|H_{olp}(jw \cdot T_s)\right|_{\phi\{H_{olp}(jw \cdot T_s)\}} \tag{2.14}$$

According to above equations, analog phase margin seems to be a good indicator of modulator sensitivity to ELD and, even, to any phase shift in general terms. If we consider again the examples shown in previous section, there is 1 degree difference in analog phase margin between the modulator with OSR 64 and the modulator with OSR 16. Analog phase margin increases with OSR.

The connection between analog phase margin and CT-SDM stability for low OSRs is an original contribution of this dissertation.

2.1.2 Compensation methods

Several researchers have looked for compensation techniques, since ELD increases instability.

There are two main compensation methods reported in technical literature. The former and most extended method is to force a pole-zero cancellation in discrete-time domain [Che00]. According to (2.8), ELD in continuous-time adds an extra zero in discrete-time NTF, i.e. $N\tilde{T}F(z)$. The aim of the method is to cancel out this extra NTF zero by adding another extra zero to the continuous-time loop-filter $H_2(s)$, such that NTF zero is cancelled by a pole. The most extended implementation of this method is an additional feedback loop around the quantizer [Ben97], [Luh00]. In the family of architectures described in chapter 0, this additional feedback loop is represented by coefficient fbe. The main advantage of this implementation is the high tolerance to the non-linearity of this extra D/A converter. Another implementation may be a different feedback loop as is reported in [Che00].

The disadvantage of this discrete-time pole-zero cancellation method is the high sensitivity to process variations and other non-idealities not taken into account in the impulse response.

The latter method consists also of adding an extra zero to $H_2(s)$ but in a different frequency. Instead of looking for pole-zero compensation, the zero is placed at $f_s/2$ [Luh00]. This helps to stability without imposing a high penalty on resolution and is more robust than previous solution. However, if ELD is high and OSR is low, this technique is not helping anymore.

2.2 Clock Jitter

CT-SDMs have a high sensitivity to uncertainty of sampling instant, i.e. to clock jitter [Che00, chapter 5]. Usually there is some noise in output signal as a consequence of clock jitter. This noise has an in-band power that may be higher than in-band quantization noise power, and/or thermal noise power, such that modulator resolution is limited by clock jitter.

In essence, clock jitter noise is of a random nature and uncorrelated with the input signal. However the mechanism for which it couples to the modulator output is intricate and has forced designers to resort to time consuming simulations to define the jitter specifications of the clock source.

There are two blocks that require a precise clock signal, the sampler before the quantizer and the D/A that generates the feedback pulse, as is shown in fig. 2.11. D/A converter is clocked to avoid signal dependant jitter, which is a consequence of quantizer metastability [Che00, chapter 5].

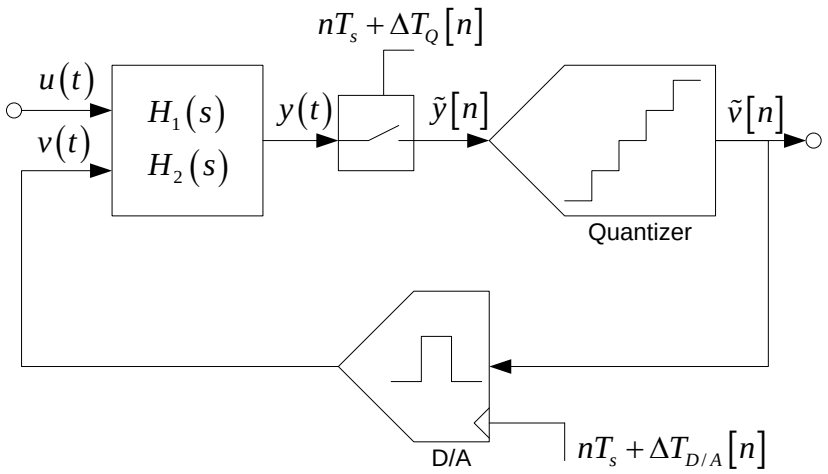

Figure 2.11 CT-SDM with clock jitter.

In general terms, clock signal for the DAC may not have the same timing errors $\Delta T_{D/A}$ than the sampling clock ΔT_Q.

2.2.1 Analysis of timing errors in the sampler

The sampler operates at points $t = nT_s + \Delta T_Q[n]$. As long as $\Delta T_Q[n]$ is a finite power sequence, the sampling error caused by the sampler will be shaped by the modulator loop. For moderate jitter levels, this error at the quantizer has smaller influence in the SNR than the error introduced by the feedback D/A, which is the main responsible of the SNR degradation.

2.2.2 Analysis of timing errors in D/A converters

The contribution of feedback D/A converters to the whole sensitivity to clock jitter in a CT-SDM depends on specific D/A location. D/A influence on SNR degradation is smaller for locations closer to the quantizer. Therefore, for the following analysis first (or main) D/A converter is only considered, i.e. the D/A whose output signal is subtracted form modulator input signal, because it is the main contributor for SNR degradation.

In general, DAC timing uncertainties $\Delta T_{D/A}[n]$ result in a wrong position of the feedback pulses and also in an error in its duration. In [Che00], several estimations of the SNR degradation are made for both Return-to Zero (RZ) and Non Return-to-Zero (NRZ) feedback pulses. A conclusion that may be drawn in both cases for lowpass modulators is that what is meaningful is the error in the area of the feedback pulses for every sampling period. A reason for this is that the feedback pulse is at least integrated once in the loop filter, as is shown in fig. 2.12. This integrated value corresponds with the area of the pulses, and hence, only the area is significant at the sampling instants at sampler, instead of the actual shape of the pulse.

For a NRZ feedback pulse, the expression of the area error is [Che00]:

$$\Delta A[n] = \left(\tilde{v}[n] - \tilde{v}[n-1]\right) \cdot \Delta T_{D/A}[n] \tag{2.15}$$

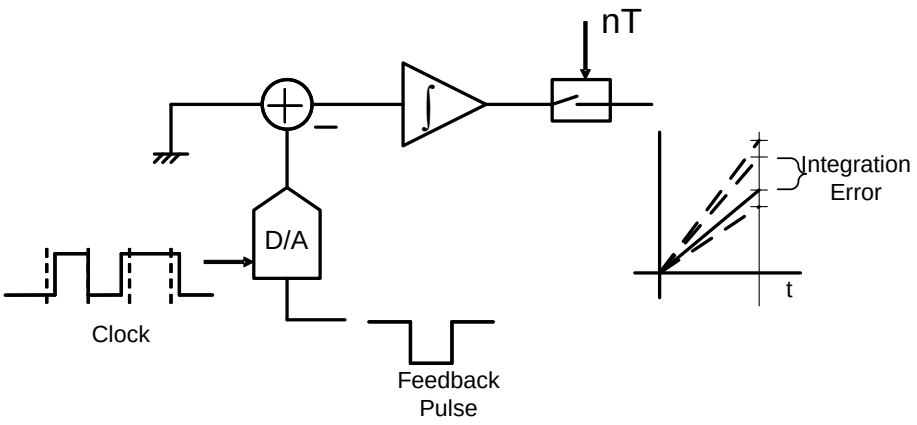

Figure 2.12 Integration errors as a consequence of clock jitter

Time dependency of the area error may be translated to an amplitude dependency, as is shown in fig. 2.13. Therefore, we may find the equivalent additive error sequence $e_j[n]$ that produces the same area error in a feedback pulse train with the ideal temporization:

$$e_j[n] = \frac{\Delta A[n]}{T_s} = \left(\tilde{v}[n] - \tilde{v}[n-1]\right) \cdot \frac{\Delta T_{D/A}[n]}{T_s} \tag{2.16}$$

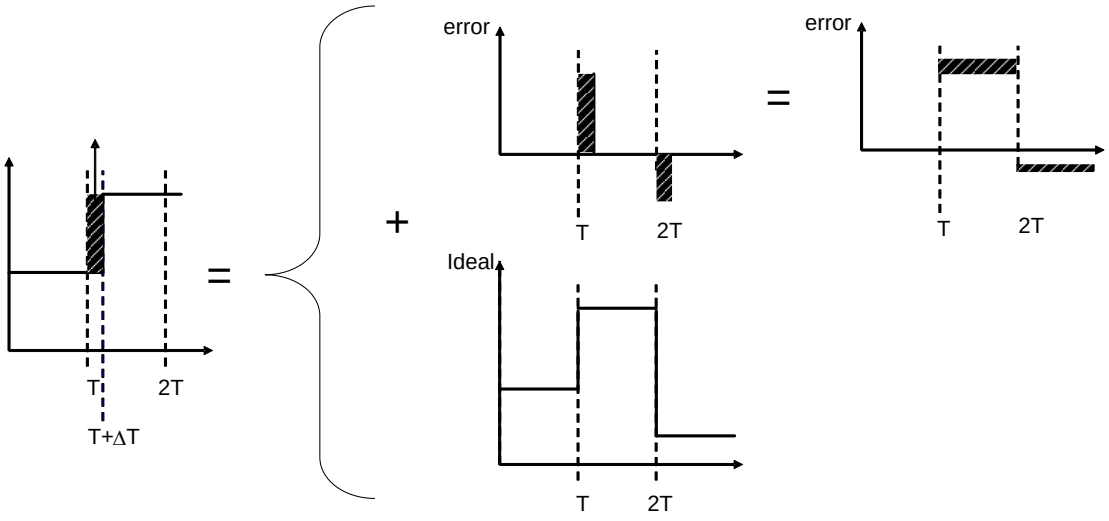

Figure 2.13 Area error equivalency between a time dependant model and an amplitude dependant model.

According to above, output of the modulator and clock jitter may be considered statistically independent, such that, variance of $e_j[n]$ may be computed as in [Che00].

$$\sigma_{ej}^2 = \frac{1}{T_s^2} \cdot \sigma_{D/A}^2 \cdot \sigma_{dv}^2 \tag{2.17}$$

where

$$d\tilde{v}[n] = \frac{\tilde{v}[n] - \tilde{v}[n-1]}{T_s} \tag{2.18}$$

The output of the modulator can be approximated by the addition of two components in order to compute (2.18). One component is the input signal filtered by STF, and the other component is the quantizer noise filtered by NTF.

2.2.3 Fast simulation model

One of the main bottle-neck of CT-SDM simulation is CPU time. Simulating timing errors implies very small and accurate integration steps to solve partial derivative equations of the modulator.

However, equation (2.16) suggests a simplified model, as is shown in fig. 2.14.

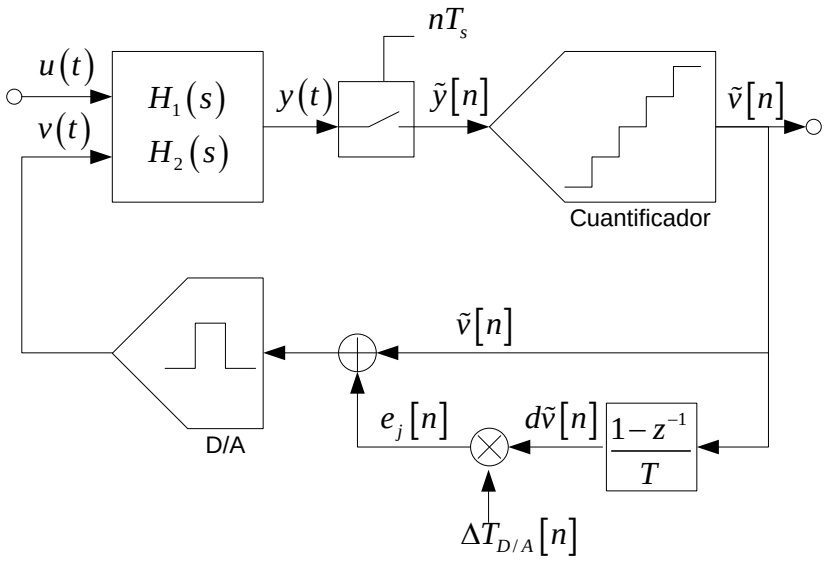

Figure 2.14 Simplified model of clock jitter influence on a CT-SDM

This model can be implemented in Simulink. The main advantage is that sequence $e_j[n]$ needs to be updated only at sampling instants, such that integration step may be increased and therefore CPU time may be decreased. As an application example, a 4th order CT-SDM has been selected. The Simulink model for this modulator is shown in fig. 2.15.

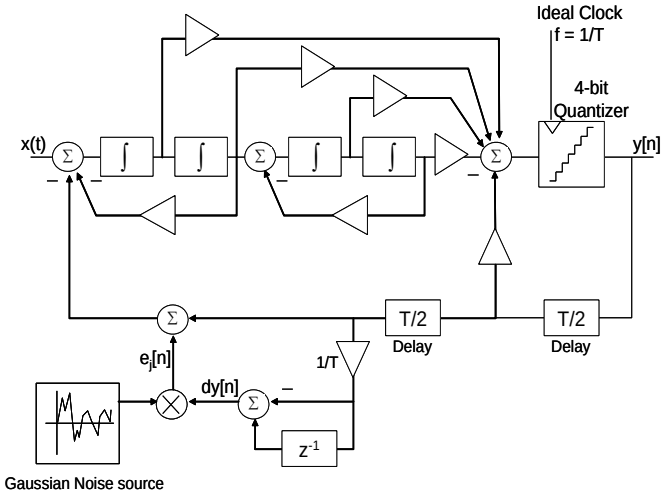

Figure 2.15 Simulink model of a 4th order CT-SDM.

To compare the precision of the simulation model, SNR versus jitter variance is plotted in fig. 2.16, for the proposed model and for an equivalent Simulink model which uses a clock generator with time varying edges. The maximum difference between both curves is 1.5 dB. However, the simulation times for the same number of samples and jitter level of the proposed model are 7 times faster on the average than the conventional model.

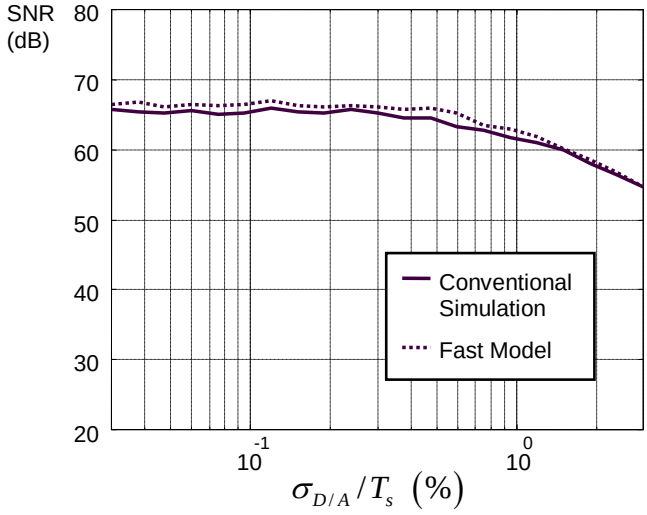

Figure 2.16 Comparison between proposed model and conventional model.

2.2.4 Jitter sensitivity optimization by NTF modification

The power of error sequence $e_j[n]$ depends on jitter power and the power of a fictitious signal $d\tilde{v}[n]$. The latter depends on signal power and quantization noise power.

Assuming the linear model of the modulator, in-band quantization noise power should be considered independent of signal. Even more, it may be computed through NTF. Therefore jitter sensitivity of the modulator may be split in two terms, one signal dependant, and another NTF or design dependant.

Consider a CT-SDM in idle-channel in order to evaluate the design dependant term. Under these conditions, the modulator is busy because of thermal noise, and the output signal depends on modulator architecture. Therefore, computation of σ_{dv}^2 may be approximated by the output of a filter with a white noise input, as follows

$$\sigma_{dv}^2 \approx \sigma_Q^2 \cdot \frac{1}{2\pi}\int_0^{2\pi}\left|\left(1-e^{-j\omega}\right)\cdot N\tilde{T}F\left(e^{j\omega}\right)\right|^2 d\omega \tag{2.19}$$

where σ_Q^2 is the variance of quantization noise and $\omega = 2\pi f \cdot T_s$

Above expression suggests a design criterion to minimize the variance of σ_{dv}^2, by modifying NTF.

In fig. 2.17.a the total area A1 of a conventional NTF design is shown, when multiplied by the modulus of the digital differentiation function ($1-z^{-1}$). In high order modulators, we may use some of the NTF zeros to reduce the gain close to half of the sampling rate, such that the area after the differentiation function, A2, is reduced but NTF still keeps its stability and SNR properties.

It may be defined a figure of merit to select the optimum NTF in terms of jitter sensitivity:

$$A_{jit}^2 = \frac{1}{\pi}\int_0^{\pi}\left|\left(1-e^{-j\omega}\right)\cdot N\tilde{T}F\left(e^{j\omega}\right)\right|^2 d\omega \tag{2.20}$$

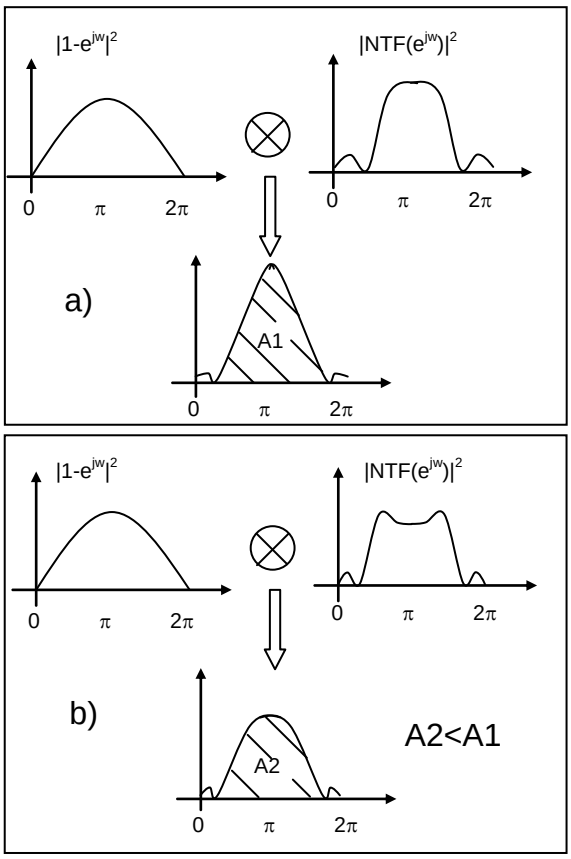

Figure 2.17 Graphical example of the jitter optimization process of a CT-SDM.

In [Her04] an application example of the proposed optimization process is shown. This method was also applied to the modulator reported in [Pat04b].

The proposed fast simulation model and figure of merit are original contributions of this dissertation.

Chapter 3

Contributions to CT-SDM design methodology

This chapter proposes a five-step design methodology, valid for CT-SDM with low OSR. First section describes the motivation of the new design method. Second section describes the method from a formal point of view. In third section some algorithms are given to implement the proposed methodology. Last section shows a Matlab tool, which has been developed to evaluate the methodology.

The proposed methodology and the Matlab tool are original contributions of this dissertation.

3.1 Using analog phase margin to stabilize and optimize a CT-SDM

Existing design methodologies have some problems that were described in chapter 0. This work is intended to solve part of these problems by finding a new design methodology.

On one hand, the design method proposed first in [Ada97a] and developed later on in [Che00] has difficulties to translate system-level specifications to circuit-level specifications. The modulator designed with this method has a high sensitivity to ELD, process variations and clock jitter.

On the other hand, the design methodology reported in [Bre01] is based on a root-locus analysis in Laplace domain, which is not sufficient to predict stability and/or robustness.

This work proposes a mixed methodology, which tries to combine the advantages of each method and to overcome the difficulties. This has been accomplished by defining two objectives. First aim is to use parameters and/or figures of merit that are common use in analog circuits design, or at least, to define some parameters and/or figures of merit that are easy to translate between system-level and circuit-level models. Second aim is that the method may be able to find an optimum modulator in terms of robustness against process variations and other effects, and resolution.

Analog phase margin has been considered a figure of merit that indicates the optimum modulator against process variations and ELD, for example. System-level design is accomplished in Laplace domain, although stability is checked on discrete-time domain.

3.2 Proposed design methodology

A five-step design method is proposed in this section. The start point of the methodology is the setting of certain specifications, namely, dynamic range, maximum SNR, maximum SNDR, maximum clock frequency, technology and maximum power consumption.

During the first step, oversampling ratio OSR, modulator order n, and number of quantizer levels M are set, in order to guarantee a certain resolution (computed form maximum SNR and dynamic range) and supposed that the modulator is feasible, taking into account the technology and power consumption. In this step it has to be decided also if NTF zeros should be all at DC or spread over analog bandwidth. Nominal amount of ELD has to be set also in this step, taking into account the clock frequency and the number of clock phases that are intended to be used in the circuit.

During the second step, the method finds a continuous-time filter that stabilizes the linear model shown in fig. 3.1. This model is computed by applying impulse invariance method on a n-th order CT-SDM with oversampling OSR and

null ELD. Quantizer gain is considered 1. The found filter is the start point of the optimization process that is carried out in next step.

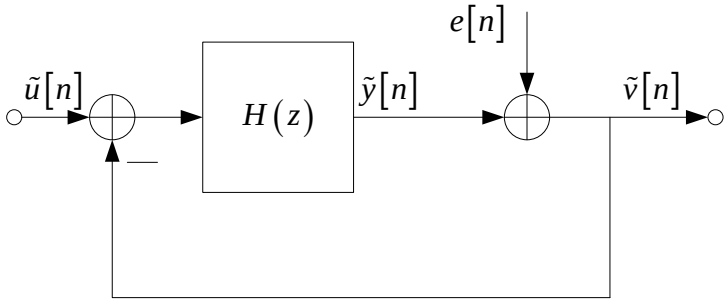

Figure 3.1 Discrete-time linear model.

The third step is an optimization process. One or several quality indicators are considered during the optimization. These quality indicators depend on the targeted optimization objectives. Analog phase margin is the selected indicator of modulator tolerance to ELD and process variations. Output average step size is the selected indicator of modulator tolerance to clock jitter. After the end of the optimization process, a transient simulation is done, to verify predicted stability and resolution.

The forth step is dedicated to topology selection. During this step, architecture coefficients are computed.

The fifth and last step consists of exhaustive verifications of modulator behavior. In this step several non-linearities and non-idealities are taken into account and are simulated, in order to release a final set of circuit specifications.

The main novelty of the proposed methodology is the optimization process. Optimization problem is formulated such that, first, a set of stable modulators are found, and later on, the optimum modulator is selected among them by using several figures of merit. In particular, the optimum is found in terms of ELD and clock jitter sensitivity. However, analog phase and/or gain margin may be used to include in the optimization other linear influences. Non-linear influences may have another figure of merit, which needs to be extracted for each particular case.

A detailed description of each design step is given in following sections.

3.2.1 Step 1: Initial parameters setting

Considering a DT-SDM with n feedback loops and assuming the linear model, dynamic range can be computed as follows, where M is the number of quantizer levels and OSR is the oversampling ratio.

$$Dynamic\ Range = \frac{3}{2}\cdot\left(\frac{2n+1}{\pi^{2n}}\right)\cdot\left(M-1\right)^2\cdot OSR^{2n+1} \tag{3.1}$$

Above equation is a theoretical limit of achievable dynamic range, because not all parameters combinations yield on stable modulators. However, if the modulator is stable, the method described in [Ada97a] produces a similar dynamic range value for the same set of parameters. Error margin is around 1 bit. The method reported in [Ada97a] allows to set NTF infinity norm, such that the modulator gets all the benefit form a multibit quantizer. However, it is usual to let a margin for stability, i.e. setting a lower NTF infinity norm than the corresponding to maximum dynamic range.

For single-bit modulators Lee rule imposes 1.5 maximum value of NTF infinity norm [Ada97a]. A conservative criterion may be setting NTF infinity norm to the average between 1.5 and the limit that corresponds to maximum dynamic range on a stable n-th order modulator with oversampling OSR and M quantizer levels. This limit value should be obtained by simulation only.

3.2.2 Step 2: Start point search

A continuous-time filter is computed during this step. This filter is the starting point for the optimization process that is carried out in next step.

Consider the general block diagram of a CT-SDM, which is shown in fig. 3.2. Its open-loop transfer function (see fig. 3.3) is given by

$$H_{olp}\left(s\right) = H_2\left(s\right)\cdot P_{\{\alpha,\beta\}}\left(s\right)\cdot e^{-\tau_d\cdot T_s\cdot s} \tag{3.2}$$

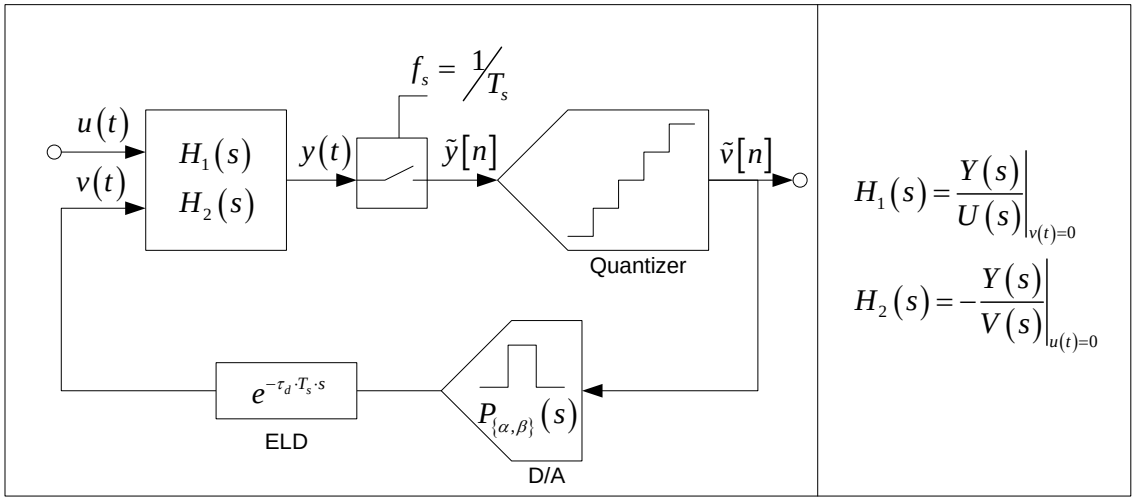

Figure 3.2 CT-SDM Block diagram

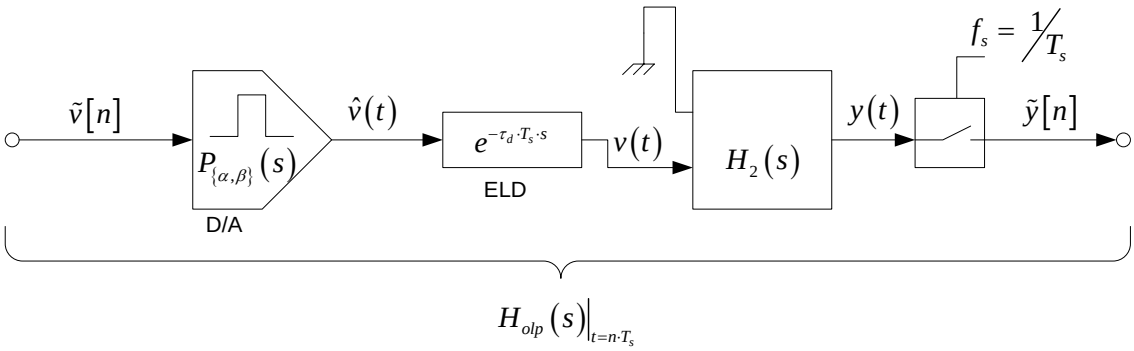

Figure 3.3 Open-loop block diagram

The starting point corresponds to null ELD, i.e. $\tau_d = 0$. The aim is to find a filter $H_2(s)$ such that $1/(1+H_2(s))$ is causal and stable.

Loop filter $H_2(s)$ poles are usually located either at DC or spread over the analog bandwidth in order to minimize in-band quantization noise power.

Loop-filter gain G_{H_2} is set at low frequency, far away from the end of analog bandwidth.

$$G_{H_2} = \left|H_2(jw_o)\right| \tag{3.3}$$

where $w = 2\pi f$.

In order to compute this gain, another useful gain may be computed before. That is the rms gain value that is needed to get a certain resolution at the outout of the modulator.

$$G_{rms} = \frac{2^{\frac{DR[dB]-1.72}{6.01}-M}}{\sqrt{OSR}} \tag{3.4}$$

G_{H_2} may be computed from G_{rms} by using an iterative method or an asymptotic approximation.

Stability of closed-loop system depends on $H_2(s)$ zero locations. They are intended to be at certain locations such that the following conditions are satisfied.

$$\lim_{w\to\infty}\left|\frac{1}{1+H_2(jw)}\right| = 1 \tag{3.5}$$

$$\left\|\frac{1}{1+H_2(s)}\right\|_\infty = 1 \tag{3.6}$$

$$s_k < 0 \;/\; 1+H_2(s_k) = 0 \tag{3.7}$$

The result of this design step is a vector $\vec{c}$ whose elements c_k are $H_2(s)$ zeros.

$$c_k \;/\; H_2(c_k) = 0 \tag{3.8}$$

3.2.3 Step 3: Optimization process

This step consists of two sub-steps:

- Design and parameterize a geometric locus ξ that contains the set of points c_k. This geometric locus is a characteristic function that defines c_k locations in Laplace domain. In this way, every $H_2(s)$ zero may be moved in Laplace domain, without changing location ratios between zeros, by modifying certain parameters of the characteristic function. The formulation proposed reduces the solution space that has to be explored during the optimization process.

- Find the parameters of ξ that locate $H_2(s)$ zeros such that the modulator is optimum against resolution and certain effects that usually degrades resolution and/or stability.

Consider the characteristic function ξ defined on the complex plane and dependant on λ_1 and λ_2 parameters.

$$\xi:\ f(\lambda_1,\lambda_2,x,y)=0\ /\ x=\mathrm{Re}(s);\ y=\mathrm{Im}(s);\ c_k\in\xi \tag{3.9}$$

In order to find the optimum modulator, we should define a figure of merit. This figure of merit may be modified depending on designer criterion. In this dissertation, it is proposed a figure of merit that takes into account:

- Modulator tolerance to phase and/or gain shifts.
- Modulator tolerance to clock jitter

This selection includes the main contributors to SNR degradation in CT-SDMs, namely, ELD and clock jitter.

Modulator tolerance to phase shifts is evaluated by means of analog phase margin of $H_{olp}(s)$. Modulator tolerance rises with phase margin.

$$\varphi\ /\ e^{-\varphi j}\cdot H_{olp}(jw)=1 \tag{3.10}$$

Modulator tolerance to clock jitter is evaluated by the area of the NTF. Modulator tolerance rises when this area decreases.

$$A_{jit}=\sqrt{\frac{1}{\pi}\int_0^{\pi}\left|\left(1-e^{-j\omega}\right)\cdot N\tilde{T}F\left(e^{j\omega}\right)\right|^2 d\omega} \tag{3.11}$$

where $\omega=w\cdot T_s=2\pi f\cdot T_s$

This area is related with average step size of the output signal of the modulator when is operated in idle-channel.

The result of this design step is the solution of the following optimization problem.

$$
\begin{aligned}
&Objective: \left(\lambda_1, \lambda_2\right)_{opt} \ / \begin{cases} \max\left(\varphi\right) \\ \min\left(A_{jit}\right) \end{cases} \\
&Restrictions: \\
&z_k < 1-\varepsilon \ / \ 1+\tilde{H}_2\left(z_k\right) = 0 \\
&\left\| N\tilde{TF}\left(e^{j\omega}\right) \right\|_\infty \le C_z \\
&\left\| \frac{1}{1+H_{olp}\left(jw\right)} \right\|_\infty \le C_s
\end{aligned}
\tag{3.12}
$$

where ε, C_z and C_s are constants depending on quantizer levels.

The considered restrictions are stability constraints. The first one corresponds to the stability condition of the linear discrete-time system $N\tilde{TF}\left(z\right)$, where ε is a security margin. The rest of restrictions correspond to experimental criteria, where C_z and C_s should be set by simulations.

There are two options when there is no solution inside the feasible region, defined by the restrictions:

- Going back to design step 2, entering with a lower resolution for the modulator,
- Or adding a real zero on $H_2\left(s\right)$, located outside the analog bandwdith. Its location, w_{fbe}, has to be considered inside the optimization process, such that the formulation may be rewritten as

$$
Objetivo: \left(\lambda_1, \lambda_2, w_{fbe}\right)_{opt} \ / \begin{cases} \max\left(\varphi\right) \\ \min\left(A_{jit}\right) \end{cases}
\tag{3.13}
$$

3.2.4 Step 4: Architecture selection

This step is dedicated to select a certain architecture for the filters $H_1\left(s\right)$ and $H_2\left(s\right)$, and to compute a set of coefficients.

Transfer function $H_2(s)$ has been defined in previous design steps, while transfer function $H_1(s)$ has to be defined in this step. Transfer function $H_1(s)$ depends on STF specification.

Consider the family of architectures described in chapter 3. The architectures included in this family have been classified in three categories:

- MFF or Multiple FeedForward branches
- MFB or Multiple FeedBack branches
- MFF&FB or Multiple FeedForward and FeedBack branches

The features of each category are described in next subsections. In every category, an initial set of coefficients needs to be specified. This set of coefficients will be scaled after in order to meet a certain state space.

3.2.4.1 MFF topology

This topology has the following ABCD matrix:

$$ABCD_{n\,even} = \left(\begin{array}{ccccc:cc} 0 & -g_1\cdot c_1 & & \cdots & 0 & b_1\cdot c_1 & c_1 \\ c_2 & 0 & 0 & & \vdots & b_2\cdot c_2 & 0 \\ & \ddots & 0 & \ddots & & \vdots & \vdots \\ \vdots & & \ddots & 0 & -g_{(n/2)}\cdot c_{(n-1)} & & \\ 0 & \cdots & & c_n & 0 & b_n\cdot c_n & 0 \\ \hdashline d_1 & & \cdots & & d_n & b_{(n+1)} & fbe \end{array}\right) \tag{3.14}$$

$$ABCD_{n\,odd}^{1R} = \left(\begin{array}{ccccc:cc} 0 & -g_1\cdot c_1 & & \cdots & 0 & b_1\cdot c_1 & c_1 \\ c_2 & 0 & 0 & & \vdots & b_2\cdot c_2 & 0 \\ & \ddots & 0 & \ddots & & \vdots & \vdots \\ \vdots & & \ddots & 0 & 0 & & \\ 0 & \cdots & & c_n & 0 & b_n\cdot c_n & 0 \\ \hdashline d_1 & & \cdots & & d_n & b_{(n+1)} & fbe \end{array}\right) \tag{3.15}$$

$$ABCD_{n\,odd}^{1I}=\left(\begin{array}{ccccc|cc} 0 & 0 & & \cdots & 0 & b_1\cdot c_1 & c_1 \\ c_2 & 0 & -g_1\cdot c_2 & & \vdots & b_2\cdot c_2 & 0 \\ & \ddots & 0 & \ddots & & \vdots & \vdots \\ \vdots & & \ddots & 0 & -g_{(n-1)/2}\cdot c_{(n-1)} & & \\ 0 & \cdots & & c_n & 0 & b_n\cdot c_n & 0 \\ \hline d_1 & & \cdots & & d_n & b_{(n+1)} & fbe \end{array}\right) \tag{3.16}$$

Feedback coefficients a_i has been removed except for $a_1=1$. Input feedforward coefficients b_i define STF according to the following rules:

$$\begin{cases} b_i=a_i \;\; y \;\; b_{n+1}=1 \Rightarrow STF=1 \\ b_i=a_i \;\; y \;\; b_{n+1}=0 \Rightarrow STF=1^{st}\;\; order\;\; low-pass \\ b_i\neq a_i\neq 0 \Rightarrow STF=all-pass \end{cases} \tag{3.17}$$

The initial set of coefficients is computed by setting c_i to 1. Once feedforward coefficients d_i are computed (and g_i if $H_2(s)$ poles are complex conjugate pairs), STF may be set by specifying coefficients b_i.

3.2.4.2 MFB Topology

This topology has the following ABCD matrix:

$$ABCD_{n\,even}=\left(\begin{array}{ccccc|cc} 0 & -g_1\cdot c_1 & & \cdots & 0 & b_1\cdot c_1 & a_1\cdot c_1 \\ c_2 & 0 & 0 & & \vdots & & \\ & \ddots & 0 & \ddots & & \vdots & \vdots \\ \vdots & & \ddots & 0 & -g_{(n/2)}\cdot c_{(n-1)} & & \\ 0 & \cdots & & c_n & 0 & b_n\cdot c_n & a_n\cdot c_n \\ \hline 0 & & \cdots & 0 & 1 & b_{(n+1)} & fbe \end{array}\right) \tag{3.18}$$

$$ABCD_{n\,odd}^{1R}=\left(\begin{array}{ccccc|cc} 0 & -g_1\cdot c_1 & & \cdots & 0 & b_1\cdot c_1 & a_1\cdot c_1 \\ c_2 & 0 & 0 & & \vdots & & \\ & \ddots & 0 & \ddots & & \vdots & \vdots \\ \vdots & & \ddots & 0 & 0 & & \\ 0 & \cdots & & c_n & 0 & b_n\cdot c_n & a_n\cdot c_n \\ \hline 0 & & \cdots & 0 & 1 & b_{(n+1)} & fbe \end{array}\right) \tag{3.19}$$

$$ABCD_{n\,odd}^{1I}=\left(\begin{array}{ccccc|cc} 0 & 0 & & \cdots & 0 & b_1\cdot c_1 & a_1\cdot c_1 \\ c_2 & 0 & -g_1\cdot c_2 & & \vdots & & \\ & \ddots & 0 & \ddots & & \vdots & \vdots \\ \vdots & & \ddots & 0 & -g_{(n-1)/2}\cdot c_{(n-1)} & & \\ 0 & \cdots & & c_n & 0 & b_n\cdot c_n & a_n\cdot c_n \\ \hline 0 & & \cdots & 0 & 1 & b_{(n+1)} & fbe \end{array}\right) \tag{3.20}$$

Feedforward coefficients d_i has been removed except for $d_n=1$. Input feedforward coefficients b_i define STF according to the following rules:

$$\begin{cases} b_i=a_i \;\; y \;\; b_{n+1}=1 \Rightarrow STF=1 \\ b_i=a_i \;\; y \;\; b_{n+1}=0 \Rightarrow STF=1^{st} \;\; order \;\; low-pass \\ b_i=0 \Rightarrow STF=n^{th} \;\; order \;\; low-pass \\ b_i\neq a_i\neq 0 \Rightarrow STF=all-pass \end{cases} \tag{3.21}$$

With this topology it can be designed an antialiasing filter, i.e. STF, up to n-th order.

The initial set of coefficients is computed by setting c_i to 1. Once feedback coefficients a_i are computed (and g_i if $H_2(s)$ poles are complex conjugate pairs), STF may be set by specifying coefficients b_i.

3.2.4.3 MFF&MFB Topology

This topology has the following ABCD matrix:

$$ABCD_{n\,even}=\left(\begin{array}{ccccc|cc} 0 & -g_1\cdot c_1 & & \cdots & 0 & b_1\cdot c_1 & a_1\cdot c_1 \\ c_2 & 0 & 0 & & \vdots & & \\ & \ddots & 0 & \ddots & & \vdots & \vdots \\ \vdots & & \ddots & 0 & -g_{(n/2)}\cdot c_{(n-1)} & & \\ 0 & \cdots & & c_n & 0 & b_n\cdot c_n & a_n\cdot c_n \\ \hline d_1 & & \cdots & & d_n & b_{(n+1)} & fbe \end{array}\right) \tag{3.22}$$

$$ABCD_{n\,odd}^{1R}=\left(\begin{array}{ccccc:cc} 0 & -g_1\cdot c_1 & & \cdots & 0 & b_1\cdot c_1 & a_1\cdot c_1 \\ c_2 & 0 & 0 & & \vdots & & \\ & \ddots & 0 & \ddots & & \vdots & \vdots \\ \vdots & & \ddots & 0 & 0 & & \\ 0 & \cdots & & c_n & 0 & b_n\cdot c_n & a_n\cdot c_n \\ \hdashline d_1 & & \cdots & & d_n & b_{(n+1)} & fbe \end{array}\right) \tag{3.23}$$

$$ABCD_{n\,odd}^{1I}=\left(\begin{array}{ccccc:cc} 0 & 0 & & \cdots & 0 & b_1\cdot c_1 & a_1\cdot c_1 \\ c_2 & 0 & -g_1\cdot c_2 & & \vdots & & \\ & \ddots & 0 & \ddots & & \vdots & \vdots \\ \vdots & & \ddots & 0 & -g_{(n-1)/2}\cdot c_{(n-1)} & & \\ 0 & \cdots & & c_n & 0 & b_n\cdot c_n & a_n\cdot c_n \\ \hdashline d_1 & & \cdots & & d_n & b_{(n+1)} & fbe \end{array}\right) \tag{3.24}$$

Both feedforward and feedback coefficients d_i and a_i are assumed to be non-null. In this topology, every coefficient d_i, a_i and b_i defines STF, although only input feedforward coefficients b_i do not have influence on NTF.

The initial set of coefficients is computed by setting c_i to 1, and at the same time, by specifying STF.

3.2.4.4 State space scaling

Loop-filter state-space defines dynamic range of every integrator outputs such that it has a strong influence on distortion. State-space scaling may helps to reduces distortion on modulator output. The best state-space is the one that minimizes distortion on modulator output.

There is a scaling procedure reported in [Nor97], which is usual in DT-SDMs. The procedure is as follows:

1) Do several transient simulations with an initial set of coefficients to realize of maximum stable input amplitude.
2) Register maximum stable state-space.
3) Scale ABCD matrix such that desired state-space is set.

This procedure guarantees a limited dynamic range of every integrator output, such that distortion is kept well below a certain level. For some applications it is interesting to find the best state-space in terms of distortion, not only one possible solution. In this case, it is necessary to define a scaling criterion.

When a linear model for $H_1(s)$ and $H_2(s)$ is considered, state-space is different than that of a non-linear model, that is, considering more accurate models for integrators. But scaling procedure is defined on the linear description of the filters.

In addition, the range of feasible values for the architecture coefficients is limited by technology.

Above restrictions and problems are solved by doing 3) iteratively, inside of an optimization loop [Fru04]. There is an objective function and a set of restrictions that defines a feasible region. An evolutive algorithm [Gol89] is used to search the optimum solution inside the feasible region. The algorithm starts the search from a random point inside the feasible region and evaluates the objective function in all neighbor points. Next point corresponds to that of maximum increment of objective function. The algorithm ends when there is no increment in any direction inside the feasible region.

The objective function is the third harmonic, measured on modulator output spectrum. The output spectrum is obtained by transient simulation of the modulator with a test tone at the input, and considering non-linear integrators. To reduce CPU time in the simulations the quantizer is removed. Although the behavior of the system is completely different when the quantizer is removed, the model is useful to evaluate distortion.

The formulation of the optimization problem is the following.

$$
\begin{aligned}
&Objetive: \left(x_i\right)_{opt} \ / \ \max\left(HD3\right) \\
&Restrictions: \\
&x_{i\min} \le x_i \le x_{i\max} \\
&a_{i\min} \le a_i \le a_{i\max} \\
&b_{i\min} \le b_i \le b_{i\max} \\
&c_{i\min} \le c_i \le c_{i\max} \\
&d_{i\min} \le d_i \le d_{i\max} \\
&g_{i\min} \le g_i \le g_{i\max} \\
&\sum_{i=1}^{n} a_i \le A_{\max} \\
&\sum_{i=1}^{n} b_i \le B_{\max} \\
&\sum_{i=1}^{n} c_i \le C_{\max} \\
&\sum_{i=1}^{n} d_i \le D_{\max} \\
&\sum_{i=1}^{n} g_i \le G_{\max} \\
&b_{n1\min} \le b_{n+1} \le b_{n1\max} \\
&i = 1, 2..n
\end{aligned}
\tag{3.25}
$$

3.2.5 Step 5: Linear and non-linear effects simulation

The last step in system-level design is to characterize the system against non-idealities, among which there are some linear and some other non-linear effects. The influence of these effects on stability and resolution has to be investigated. The output of this step is a set of predicted features for the modulator and another set of circuit-blocks specifications.

Most common simulations include:

- Finite bandwidth of active elements
- Finite linearity of D/A converters
- Clock jitter
- Process variations (Montecarlo analysis)

3.3 Development of a software tool for CT-SDMs design

In order to evaluate the proposed design methodology, a software tool has been developed. This tool covers design steps 2 and 3 completely, and part of some other steps.

This section describes some algorithms that help to implement the proposed methodology. Next section shows a Matlab graphic interface that includes these algorithms.

3.3.1 Algorithm for $H_2(s)$ pole placement (Step 2)

The algorithm for NTF zero placement is the same that is reported in [Ada97a]. There are some functions inside *delsig toolbox* [Sch03] that may be used to compute NTF zero locations. These functions uses table 3.1 to spread NTF zeros over the analog bandwidth.

Table 3.1 Normalized NTF zero locations that minimize in-band quantization noise power

n	Zero locations (normalized to $f_s/2\cdot OSR$)
1	0
2	±0.57735
3	0, ±0.77460
4	±0.11559, ±0.74156
5	0, ±0.28995, ±0.82116
6	±0.23862, ±0.66121, ±0.93247

Once NTF zero locations are computed (in discrete-time domain), $H_2(s)$ pole frequencies may be obtained by applying (3.26), where ntf_c_k arte NTF zeros, and f_s is the sampling frequency.

$$p_k = \ln(ntf\_c_k) \cdot f_s \tag{3.26}$$

3.3.2 Algorithm for initial point search (Step 2)

The geometric locus ξ of $H_2(s)$ zeros has been defined and parameterized even before the initial point search. Several analog filter prototypes have been studied as geometric locus, namely, butterworth, chebysheb type I and elliptic. Table 3.2 shows a comparative between them. Every design has been done with the proposed methodology from the following data: is a 4th order modulator, with a 2-bit quantizer, an OSR of 12 and 20% ELD without compensation. The best resolution with best phase margin is the modulator designed with elliptic characteristic function.

Table 3.2 Comparative of several characteristic functions

Characteristic function	Butterworth	Chebysheb I	Elliptic
Cut-off frequency (MHz)	16	17.5	16.5
Band-pass ripple (dB)	-	0.5	0.5
Stop-band ripple (dB)	-	-	25
Dc Gain (dB)	40	40	40
Phase margin (°)	10.5	21.3	23.7
$\left\|N\tilde{T}F\left(e^{j\omega}\right)\right\|_\infty$	5.1	2.8	2.6
SNR (dB) (-2dB tone at BW/2)	0 (Unstable)	59	61

The characteristic function of an elliptic filter depends on three parameters, namely, cut-off frequency, bandpass ripple and stop-band ripple. These parameters

define how is the 0dB crossing of $\left|H_{olp}\left(jw\right)\right|$. In general terms it is desired to be a first-order shape.

The initial point search for the optimization process of next step uses one of the described characteristic functions. This search starts from a cut-off frequency equal to the analog bandwidth of the modulator, continue increasing cut-of frequency by a certain step, and ends when (3.5), (3.6) and (3.7) are fulfilled. If the cut-off frequency reaches half of the sampling frequency without success, the search is restarted with a lower step and inside the analog bandwidth, close to the end of the band.

In practice, small shifts from conditions (3.5) and (3.6) are allowed. These shifts should be reduced if search step is reduced.

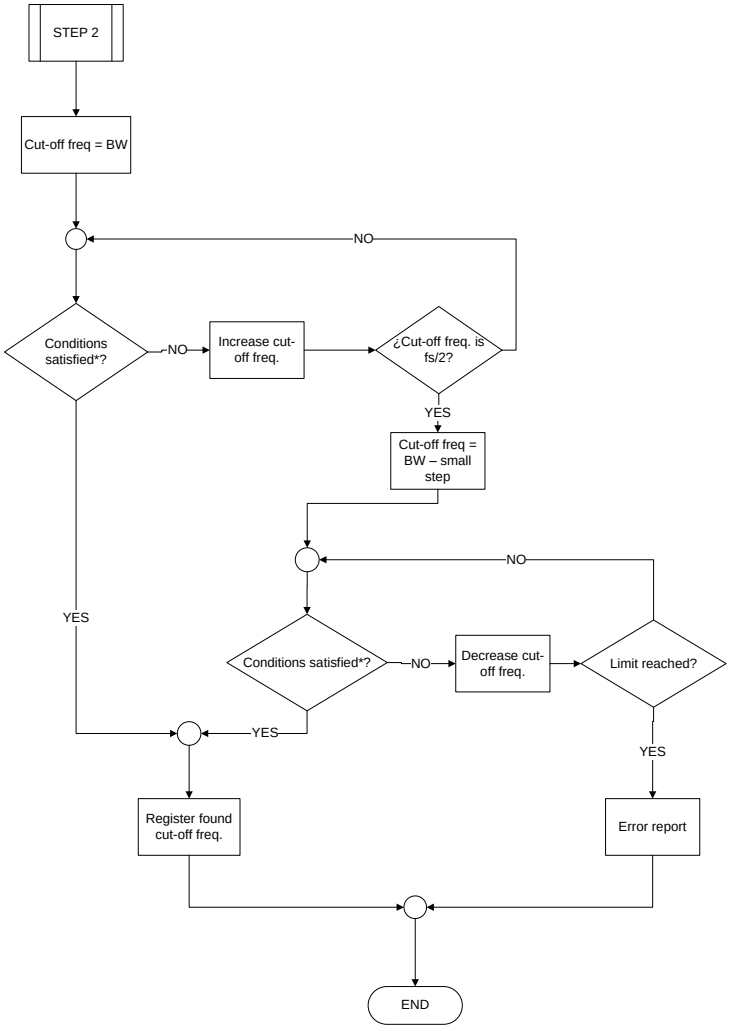

Figure 3.4 Step 2 Flow diagram. (*) Conditions are (3.5), (3.6) and (3.7)

3.3.3 Algorithm for optimum search (Step 3)

The optimization problem formulated in section 3.2.3 has been implemented as a simple search. The simplifications are:

- The objective function is a figure of merit that is evaluated in each iteration step. This figure of merit has been defined as

$$FOM = \varphi - A_{jit} \tag{3.27}$$

- To force entering inside the feasible region, $H_2(s)$ have added a zero at half of the sampling rate.
- This high frequency zero is shifted to lower frequencies in each iteration step, up to the end of analog bandwidth.
- The search ends when the figure of merit remains unaffected or becomes smaller.

A flowchart is shown in fig. 3.5

3.3.4 Considered topologies (Step 4)

Among the topologies described in design step 4, there has only been implemented the following:

- MFF topology with $b_1 = 1$ and $b_i = 0$ for $i = 2..n+1$
- MFB topology with $b_1 = 1$ and $b_i = 0$ for $i = 2..n+1$
- MFB topology with $b_{n+1} = 1$ and $b_i = a_i$ for $i = 1..n$, and named *MFB(bi)* inside the tool
- MFF&MFB topology with $b_1 = 1$ and $b_i = 0$ for $i = 2..n+1$, and named *MFBMFF* inside the tool

Every set of coefficients is computed setting $c_i = 1$ for each topology. This set is scaled afterwards in the optimization (against distortion) tool that is named *Optool* [Fru04].

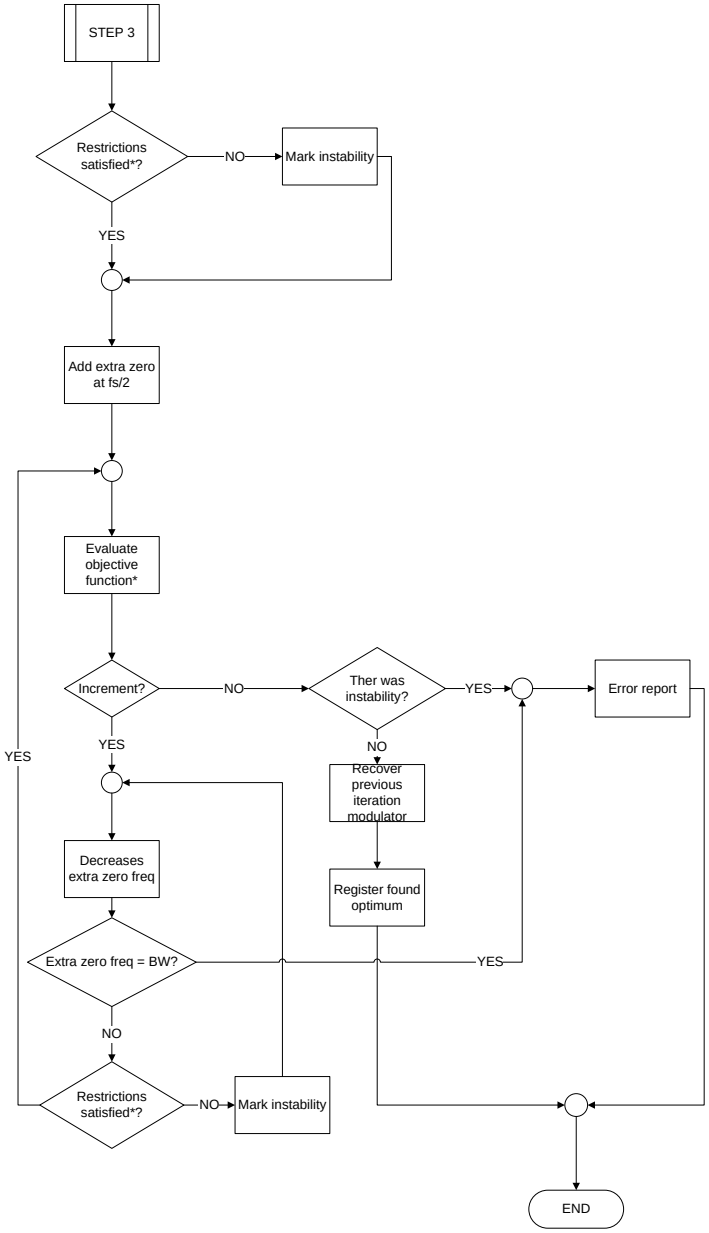

Figure 3.5 Step 3 Flow diagram. (*) Objective function is the figure of merit (3.27) and the restrictions are (3.13)

3.3.5 Algorithm for state-space scaling (Step 4)

The evolutive algorithm that solves (3.25) has been programmed in Matlab. The graphic interface is shown in fig. 3.6.

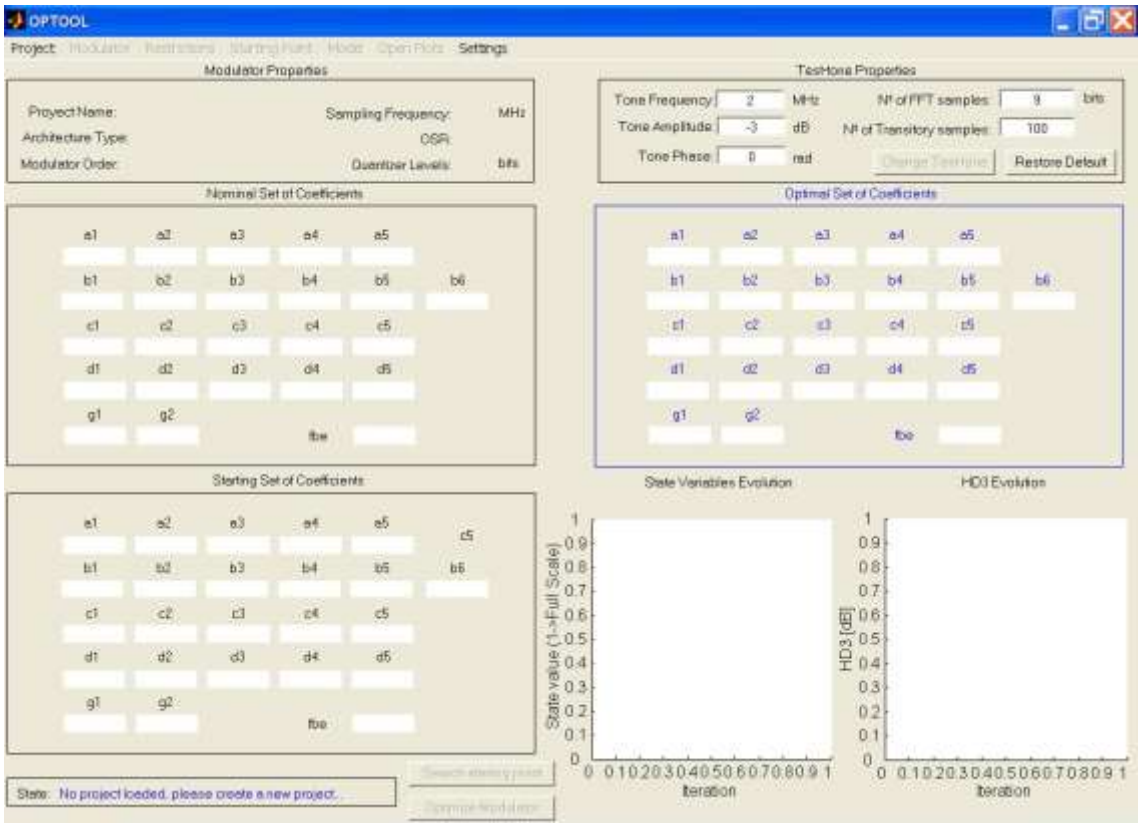

Figure 3.6 Screen capture of the graphic interface of OPTOOL: A tool for optimum state-space scaling [Fur04]

3.4 Development of a Matlab tool: ANATEST

All the algorithms described in section 3.3 have been implemented in Matlab. They may be run from a graphic interface that is shown in fig. 3.7. The purpose of the tool is non-commercial. It was targeted to evaluate, debug and improve the proposed design methodology. For this reason, there is more information in the graphic interface than what should be needed.

Source code of the tool has been developed in modules, such that design steps and algorithms can be modified and/or replaced easily. There are available several characteristic functions for the design of $H_2(s)$.

There are four sections or blocks in the graphic interface, as is shown in fig. 3.7, namely, Menu, Control, Data Entry and Output Linear Analysis.

Figure 3.8 shows which elements of the tool have to be used in order to follow the proposed design methodology. Each one of the blocks of the graphic interface is shown in fig. from 3.9 to 3.15.

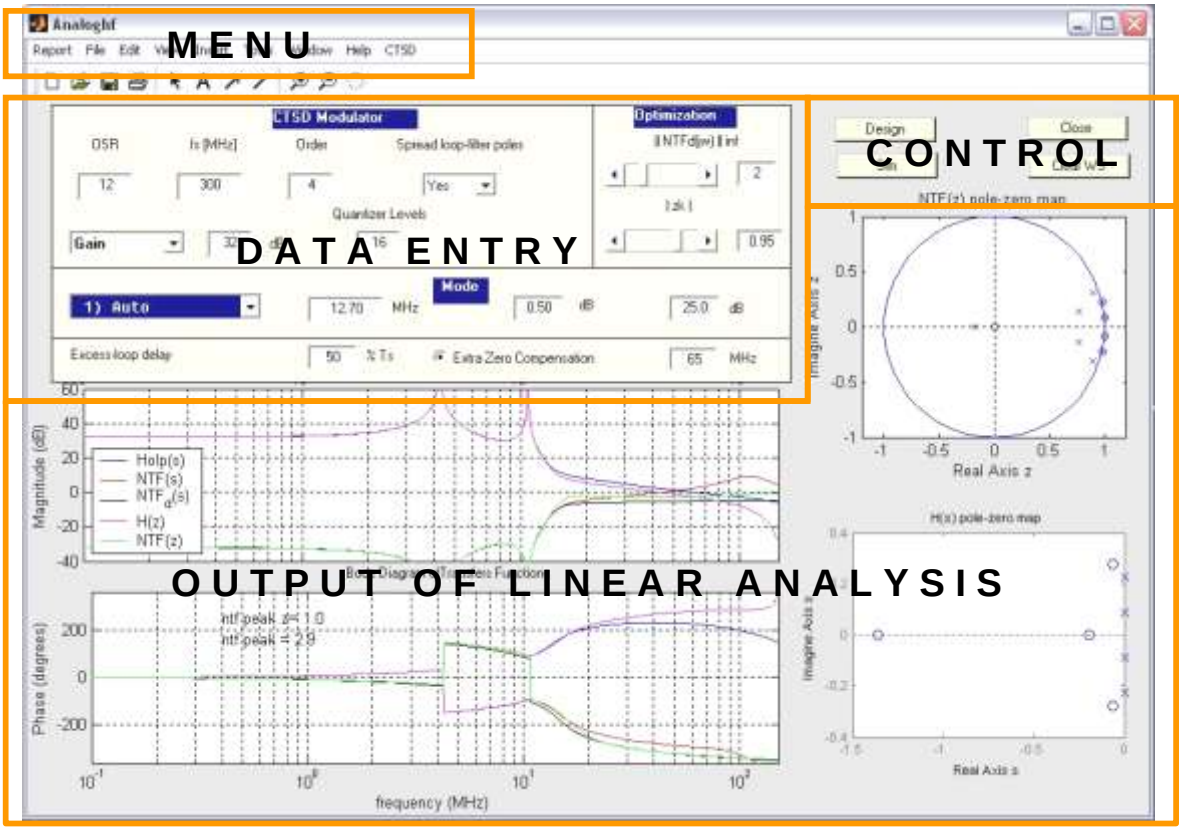

Figure 3.7 Graphic interface of ANATEST

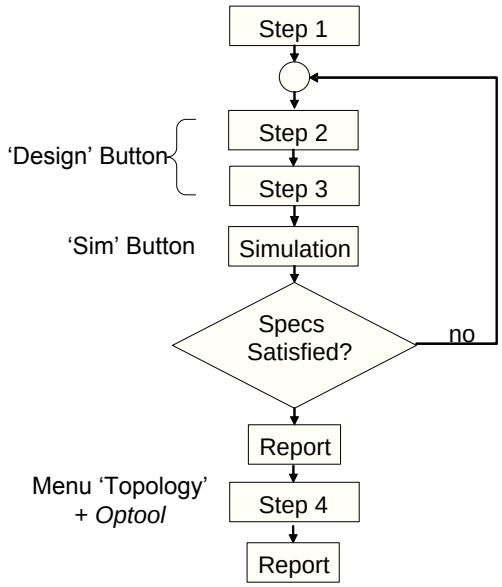

Figure 3.8 Flowchart of design process and how to follow it with ANATEST

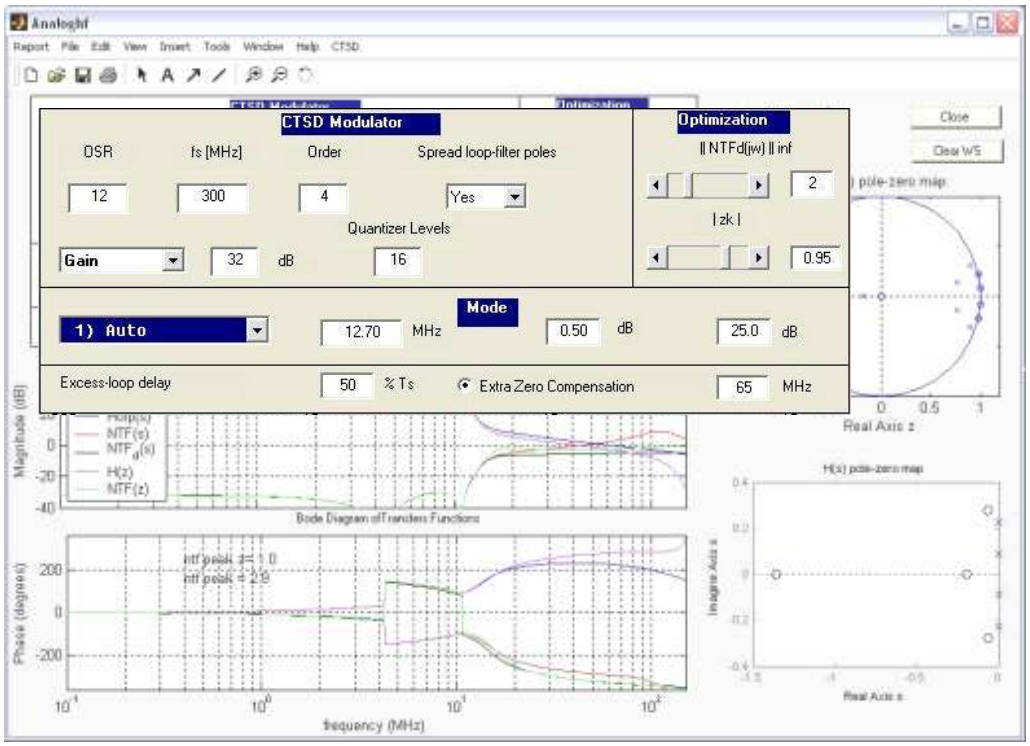

Figure 3.9 Data Entry block.

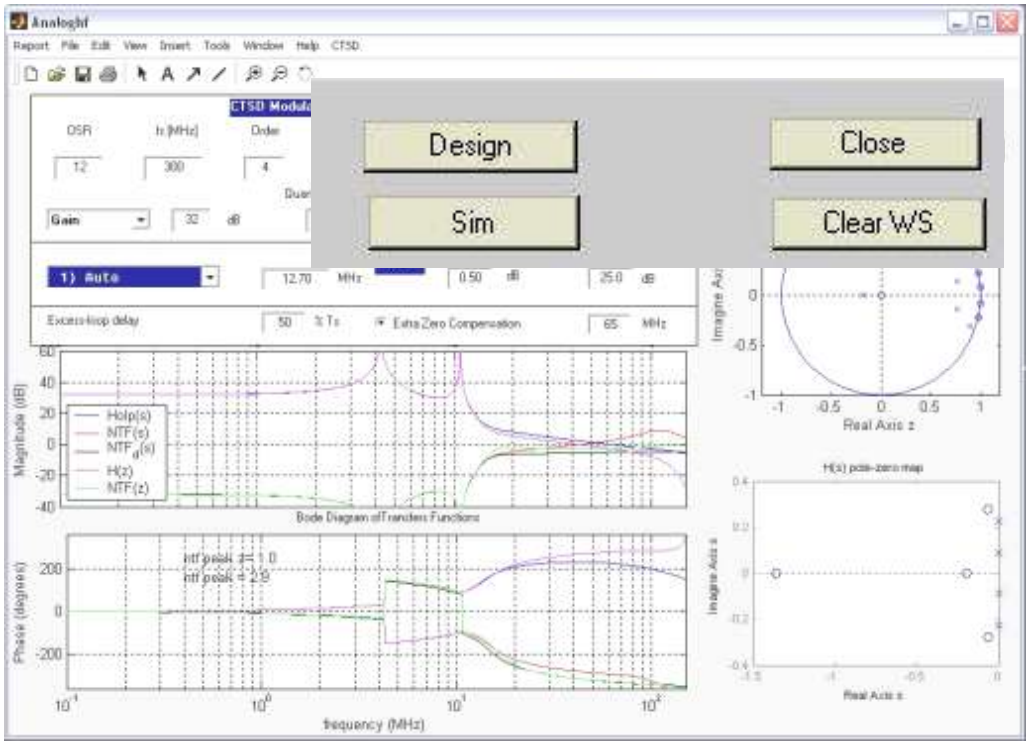

Figure 3.10 Control block

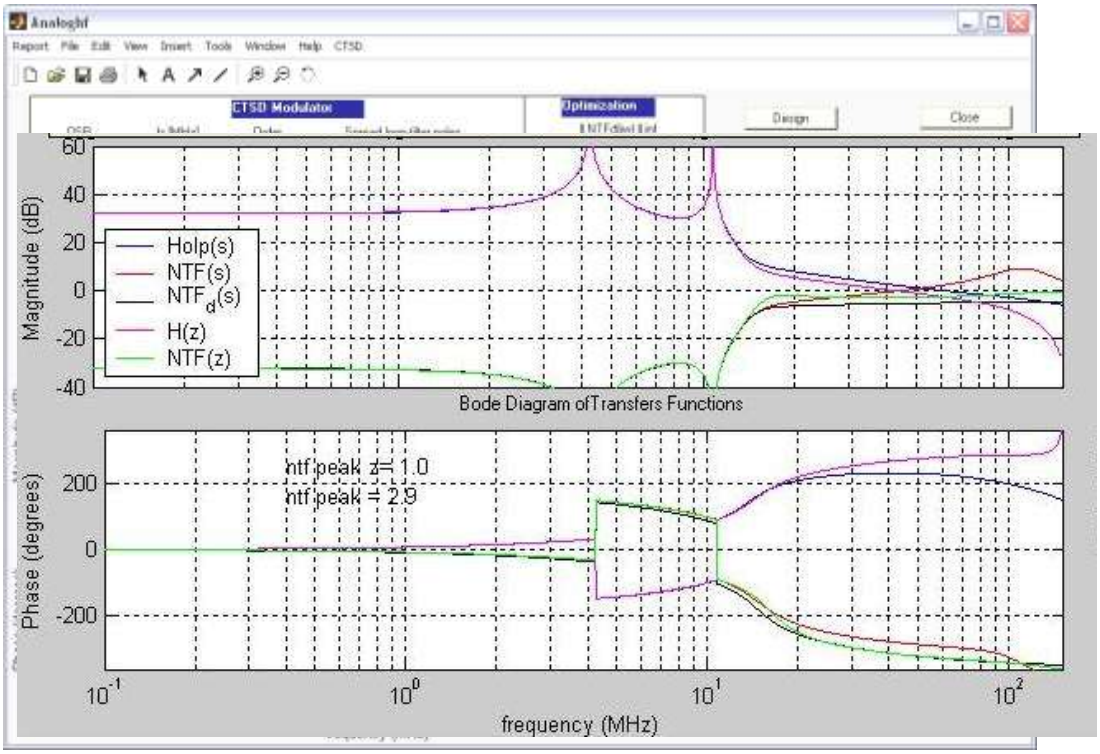

Figure 3.11 Output linear analysis block: Bode diagrams.

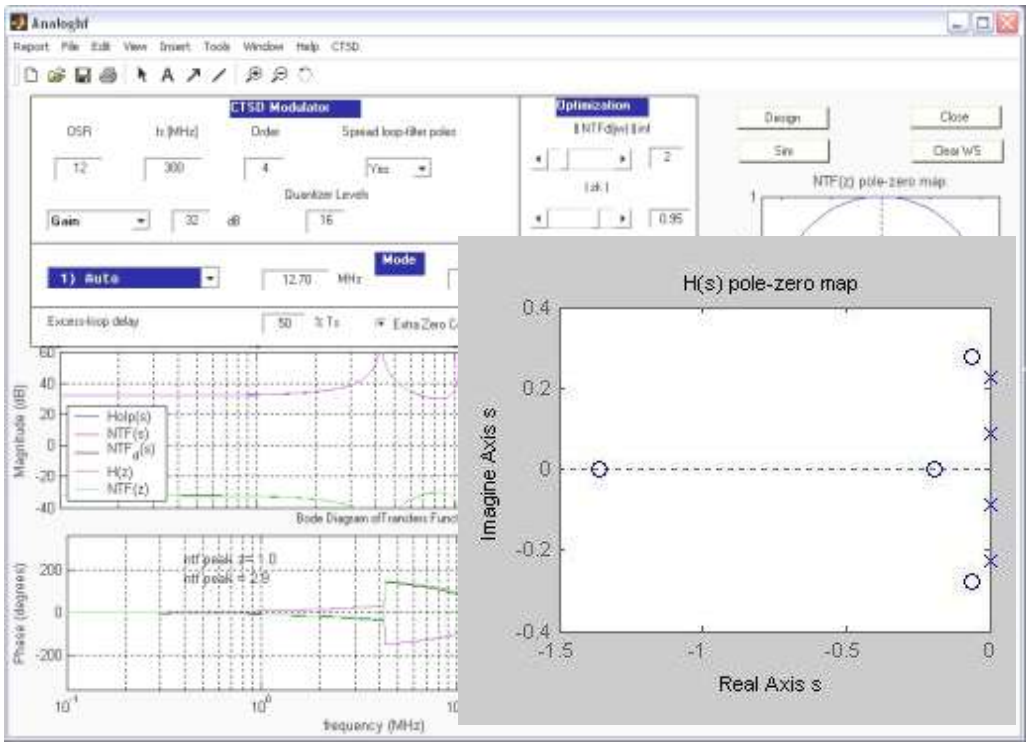

Figure 3.12 Output linear analysis block: pole-zero map of $H_2(s)$

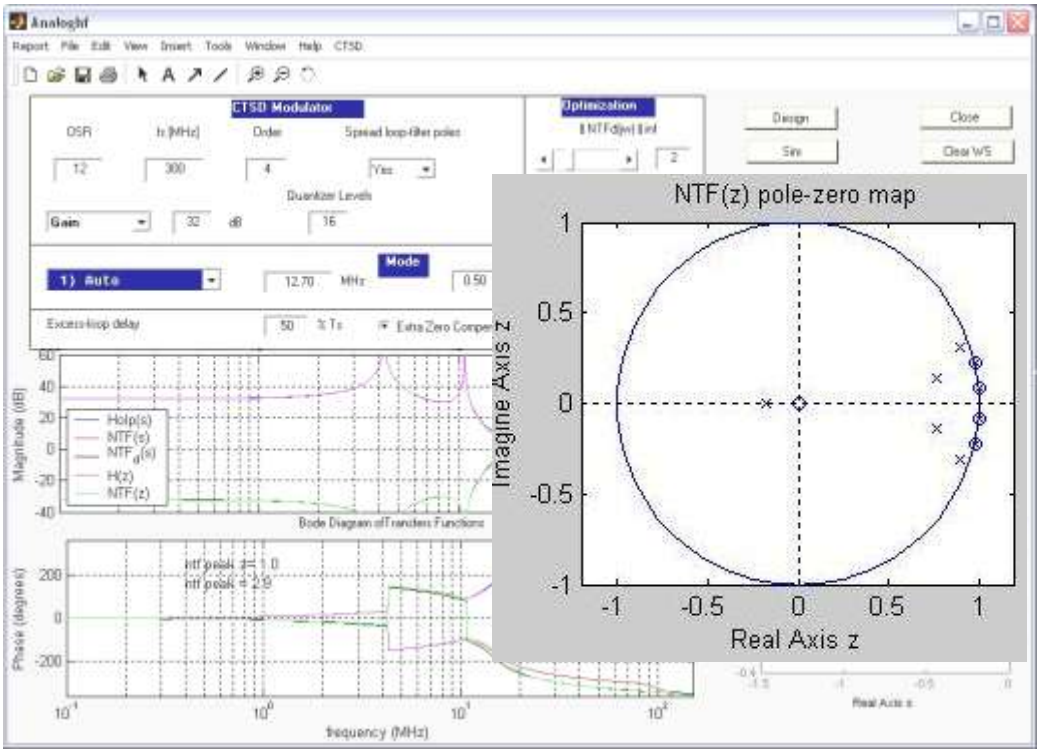

Figure 3.13 Output linear analysis block: pole-zero map of $N\tilde{T}F(z)$

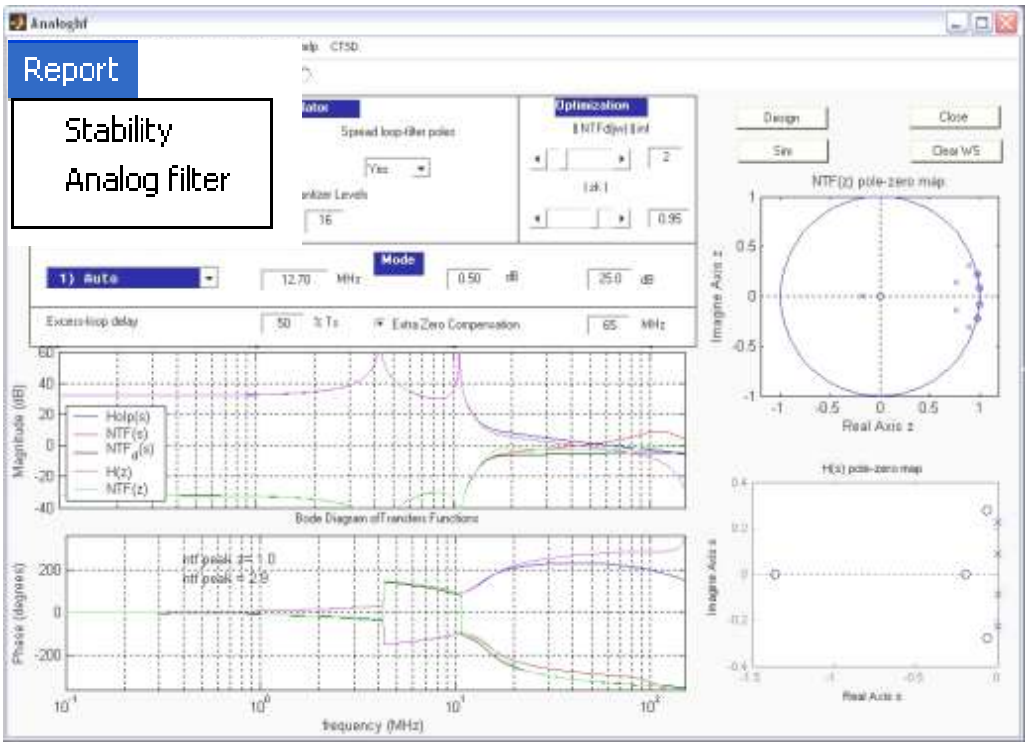

Figure 3.14 Menu block: Report menu

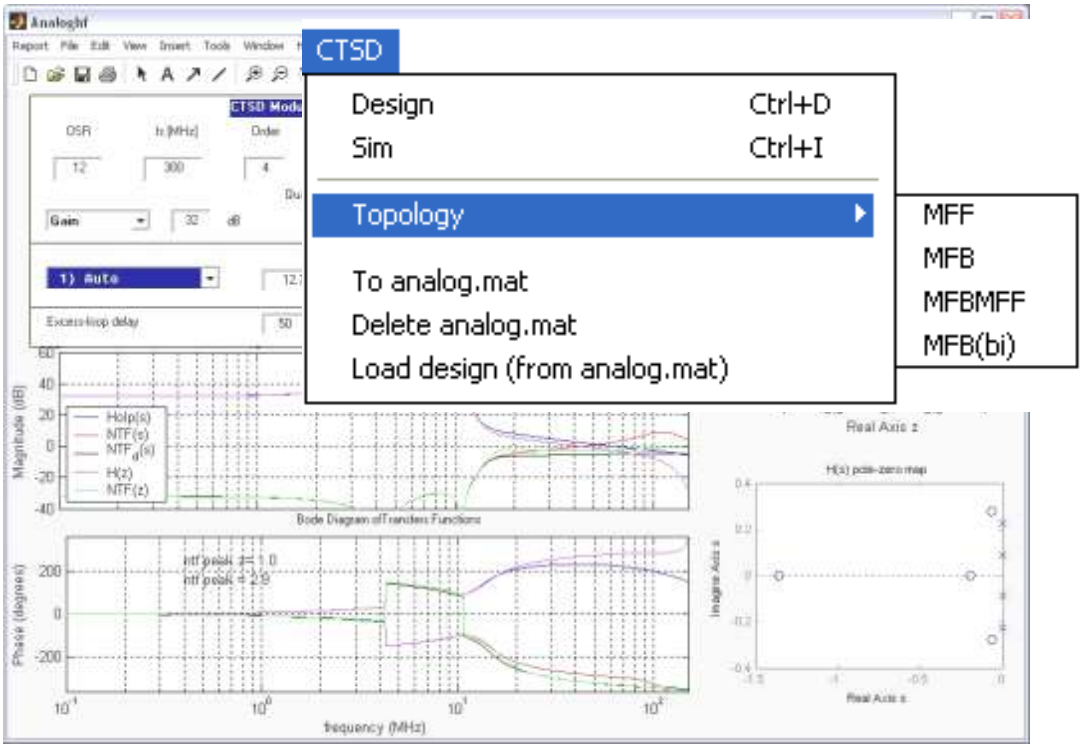

Figure 3.15 Menu block: general menu[1]

There has been considered three main design modes inside the tool, namely, *Automatic*, *Manual* and *Custom*. *Automatic* mode performs design steps 2 and 3 and a transient simulation without user interaction. It uses an elliptic characteristic function to place $H_2(s)$ zeros. *Manual* mode is not available with this name. In fact, a variety of characteristic functions is available to place $H_2(s)$ zeros. It does not use any algorithm. In this mode, 'Design' button computes all transfer functions, evaluates φ and A_{jit}, plots pole-zero maps and Bode diagrams, and fills the reports. *Custom* mode is dedicated to research. It can be used to test new characteristic functions or new algorithms.

A detailed description of every mode and some examples may be found in [Ber04].

[1] See section 3.3.4

Chapter 4

Application example: a 4th order CT-SDM

The application example has been developed in a collaboration project between Infineon Technologies Design center of Villach, Austria and Carlos III University, Madrid, Spain. The target of the project was to find a CT-SDM competitive in resolution and power with pipeline solutions for high-speed applications. At the time of writing this document, there are three generations of high-speed CT-SDM fabricated and tested within the scope of this project. The results obtained from first generation were good enough for the purpose of pipeline comparison. This generation has been disclosed in [Gia03a] and [Pat04b].

The design of modulator has been split in two main blocks: system-level design (architecture, coefficients, some circuit-block specifications) that was done by Microelectronics group in Carlos III University, and circuit-level design (all actives stages at transistor level, layout) that was done at Infineon Technologies. The fabrication of the integrated circuit and subsequent test was also done at Infineon Technologies, although some measurements were done by Microelectronics group during summer stays at Infineon Technologies in Villach, Austria.

System-level design has been the motivation of this dissertation, while circuit-level design has been the motivation of the dissertation presented by Antonio Di Giandomenico for his PhD degree [Gia03b].

4.1 Design Specifications

Table 4.1 shows the specifications. Analog bandwidth and OSR are not completely defined because the target was to look for a competitive solution. Anyhow, the maximum clock frequency is set to 400MHz.

At the end, there were two designs in this generation. The former has the lowest bandwidth but the highest OSR [Pat04a], and the latter has the highest bandwidth and the lowest OSR [Gia03a], [Pat04b]. The former has higher SNR than that of the latter because of the higher OSR, but is more unstable because 400MHz clock is used and circuit blocks were at the limit oh their nominal conditions.

The chapter is focused on the design with highest bandwidth.

Table 4.1 Design specifications

Analog interface	
Input analog bandwidth	12MHz ~ 15MHz
Input	Differential
Digital Interface	
Output	Serial
Output/Input Levels	3.3 V CMOS
Test Interface	SPI
OSR	10 ~ 16
Sampling clock	External
ELD	1 sampling period
Power supply	
Core	1.2V
Digital Input/Outputs	3.3 V
Power consumption	<80mA 11bits effective
Technology	
Process	0.13μm digital CMOS
Performance	
SNR	>68dB
SFDR	60dBc for 0dBFS input 66dBc for -6dBFS 72dBc for -12dBFS

4.2 Technology

The modulator has been implemented in 6-metal 0.13μm CMOS process without any digital special option. All MOS transistors have regular threshold voltages.

Capacitors are of type "Grid-cap" and the resistors are polisilicon resistors.

4.3 Setting of modulator order, quantizer resolution and OSR

These parameters have been selected after a wide set of discrete-time simulations. The simulations were targeted for feasibility analysis and do not guarantee hat the final CT-SDM has the same SNR. As it was discussed in previous chapters it is preferred to obtain a robust modulator rather than an exact continuous-time counterpart.

Several NTFs have been designed. Every NTF has been simulated (assuming STF=1) with a certain quantizer and a -4dB input tone, and after SNR has been computed. NTF design depends on the following parameters:

- Modulator order ,
- Choice between spreading or not NTF zeros over analog bandwidth, in order to minimize in-band quantization noise power.
- OSR, and
- NTF infinity norm. Quantizer resolution defines a limit for this value that is of experimental nature.

A subset of the results has been depicted in fig. 4.1 and 4.2. In first figure (fig. 4.1), all considered combinations have been designed such that NTF infinity norm is optimized for the employed quantizer. This means that the modulator is optimal in resolution. In second figure (fig. 4.2), all the considered combinations have 1.5 NTF

infinity norm. Modulators with high-resolution quantizers have a certain margin for stability but they have sub-optimal resolution.

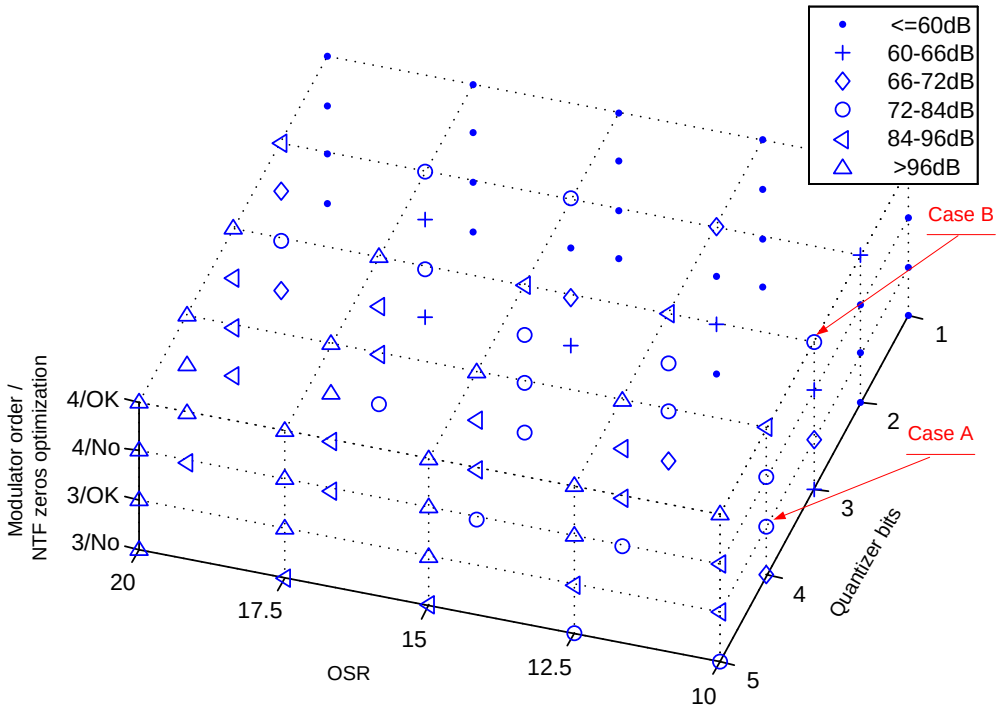

Figure 4.1 DT-SDMs classified by SNR. NTF infinity norm is optimized en each combination for the quantizer resolution.

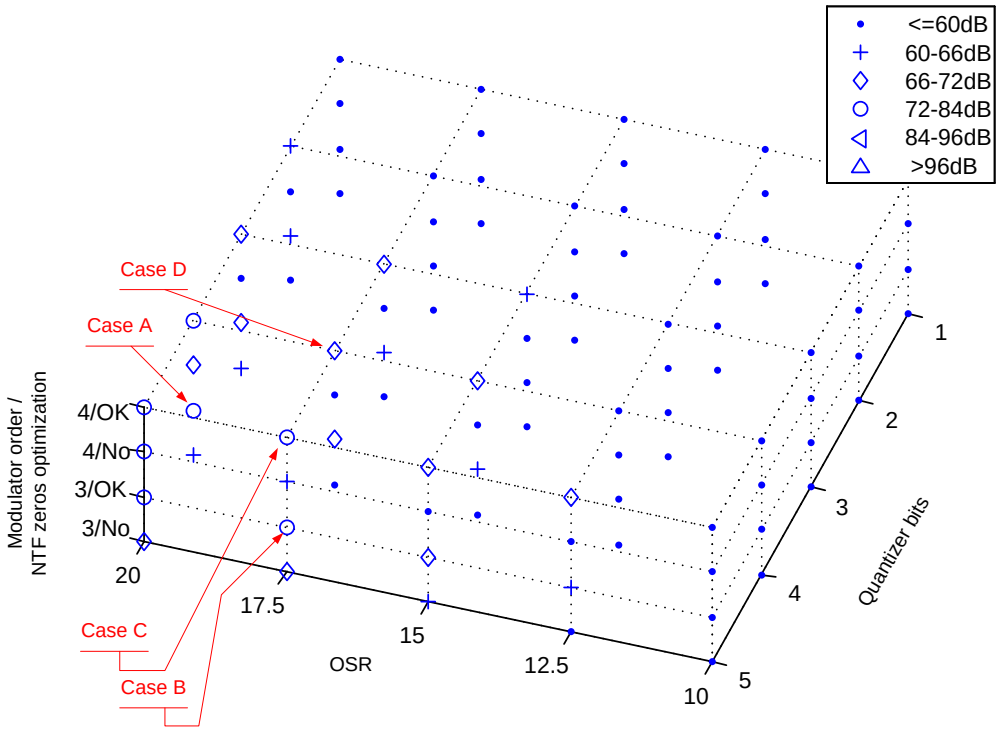

Figure 4.2 DT-SDMs classified by SNR. NTF infinity norm is 1.5 in every combination.

Multibit modulators in fig. 4.2 have a very conservative design criterion, by setting NTF infinity norm to 1.5. In contrast, all modulators in fig. 4.1 has low stability margin and will need of accurate calibration techniques.

Averaging NTF infinity norm values obtained form both methods would result in a more reasonable solution.

Average SNR is shown in fig. 4.3 Cases A and B are 4th-order, 4-bit with low OSR values. These seem to be feasible solutions.

The final selection is OSR=10 to enlarge analog bandwidth.

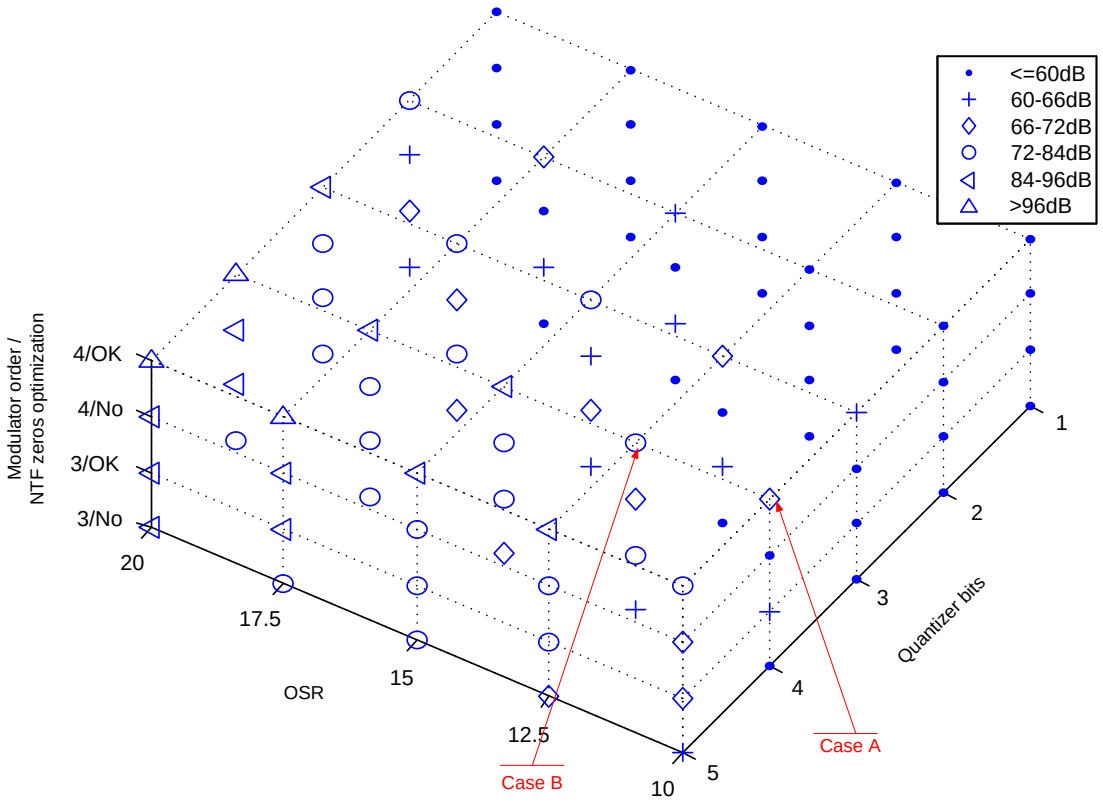

Figure 4.3 DT-SDMs classified by SNR. SNR is averaged between modulators designed with 1.5 and optimized NTF infinity norm.

4.4 Continuous-time loop filter

Continuous-time filter has been obtained by using a preliminary version of ANATEST tool with 75% ELD.

The result is shown in table 4.2. A screen capture of the tool is shown in fig. 4.4 and transient simulations are shown in fig. 4.5 and 4.6.

Table 4.2 Design summary

Analog bandwidth	15MHz	DC gain	31 dB
Clock frequency	300MHz	Phase margin φ	22.6°
Quantizer resolution	4 bits	0dB crossing	58.0 MHz
Modulator order	4	A_{jit}	1.18
ELD	0.75-1.25 Ts	Dynamic range	68 dB
Loop-filter poles (MHz)	±5.1j ±12.9j	Maximum SNR	66dB
Loop-filter zeros (MHz)	-3.8±16.3j -11.5 -72.0		

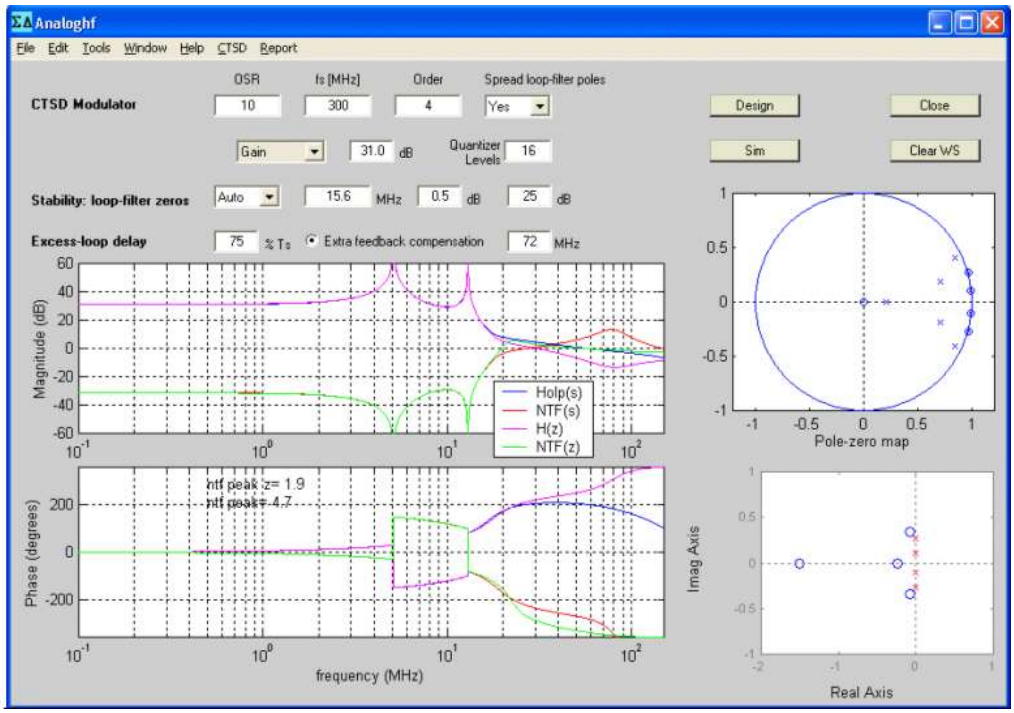

Figure 4.4 Screen capture of a preliminary version of ANATES tool

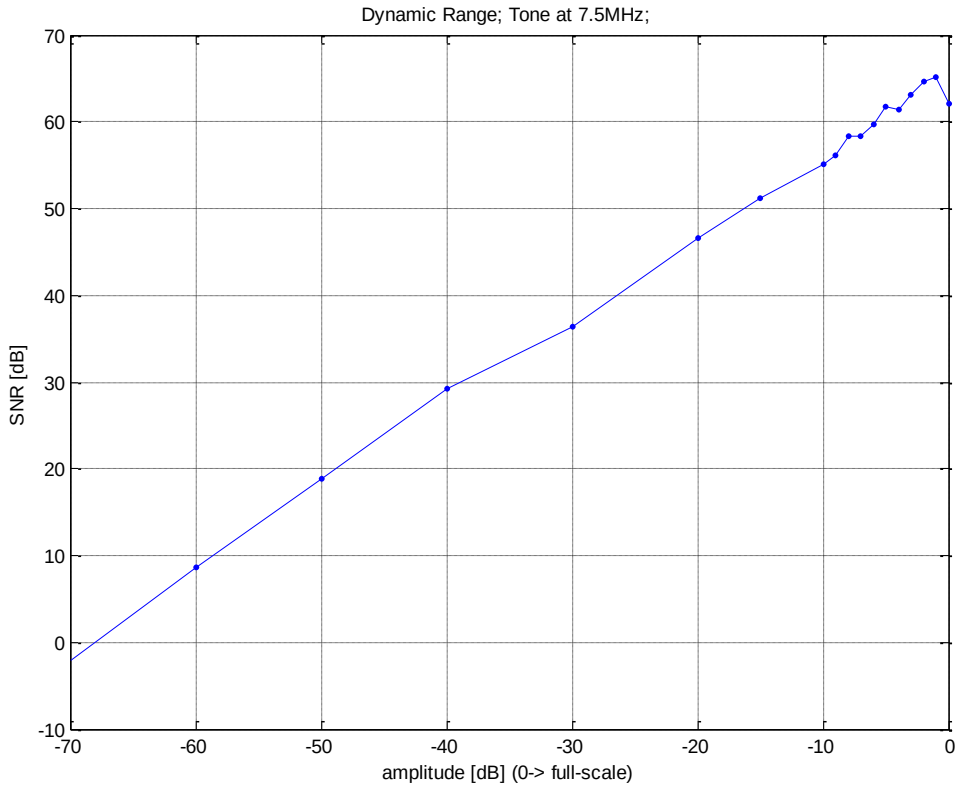

Figure 4.5 Dynamic Range (from preliminary version of ANATEST)

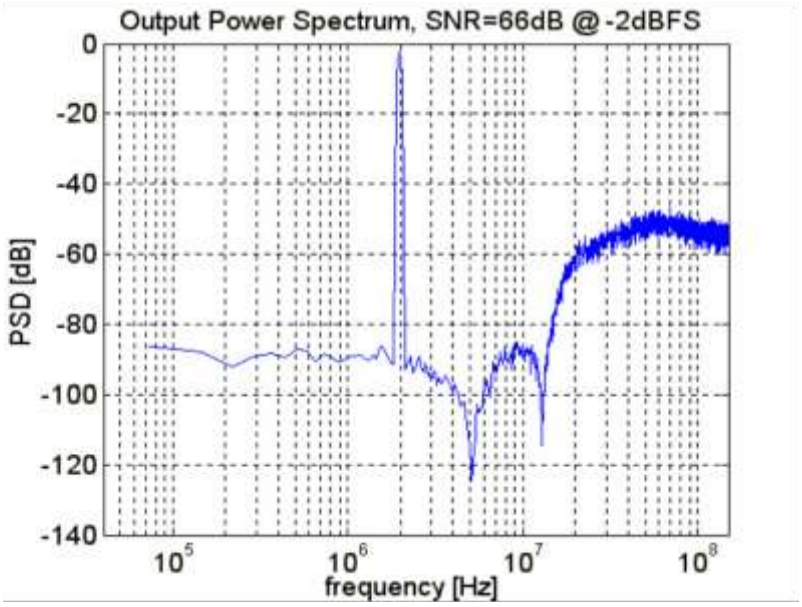

Figure 4.6 Power spectral density of the output signal when the CT-SDM is simulated with a -2dB tone at 2MHz (from preliminary version of ANATEST)

4.5 Architecture selection

The designed continuous-time loop-filter corresponds to $H_2(s)$ in fig. 4.7. $H_1(s)$ depends on architecture selection and STF specification.

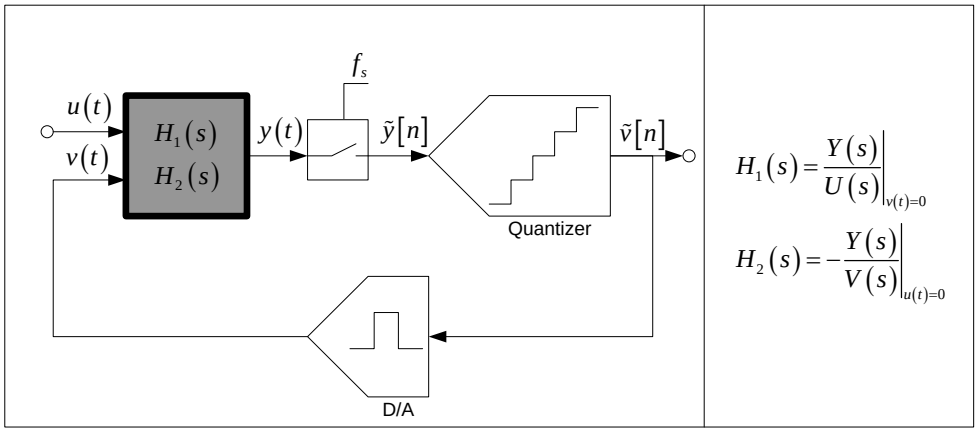

Figure 4.7 CT-SDM Block diagram

The following restrictions have been taken into account in order to select an adequate architecture:

- The architecture should be included in the family described in chapter 0.
- For multibit quantizers $y(t)$ should be a voltage, such that A/D flash may be used.
- Signal may be added in current mode to simplify the circuit. That means that a_i and *fbe* coefficients are current steering D/As.
- A resistor placed on op-amp vritual ground is a more linaer solution for v-i conversion than transconductances.
- State-space defines distortion on active stages.
- Input feedforward coefficients b_i modify state-space. Usually they help to decrease distortion, but then STF is modified and anti-aliasing function may be lost.
- Distortion level and bandwidth of active stages depends on the allowed power consumption.

- Active stages added in front of the quantizer are the least restrictive in terms of noise and distortion.
- Due to multibit quantizer, a dynamic element matching technique may be needed to linearize D/A
- Digital circuitry of dynamic element matching logic may increases ELD.

According to above restrictions, the following decisions have been taken:

- The integrators are implemented with op-amps of 600MHZ gain-bandwidth product.
- The architecture should be MFF or MFB but not both in order to decreases power consumption.
- A MFF architecture is preferred because it uses a lower number of D/A converters than MFB.
- The feedforward coefficients are transconductances, such that state-space addition is placed in front of the quantizer.

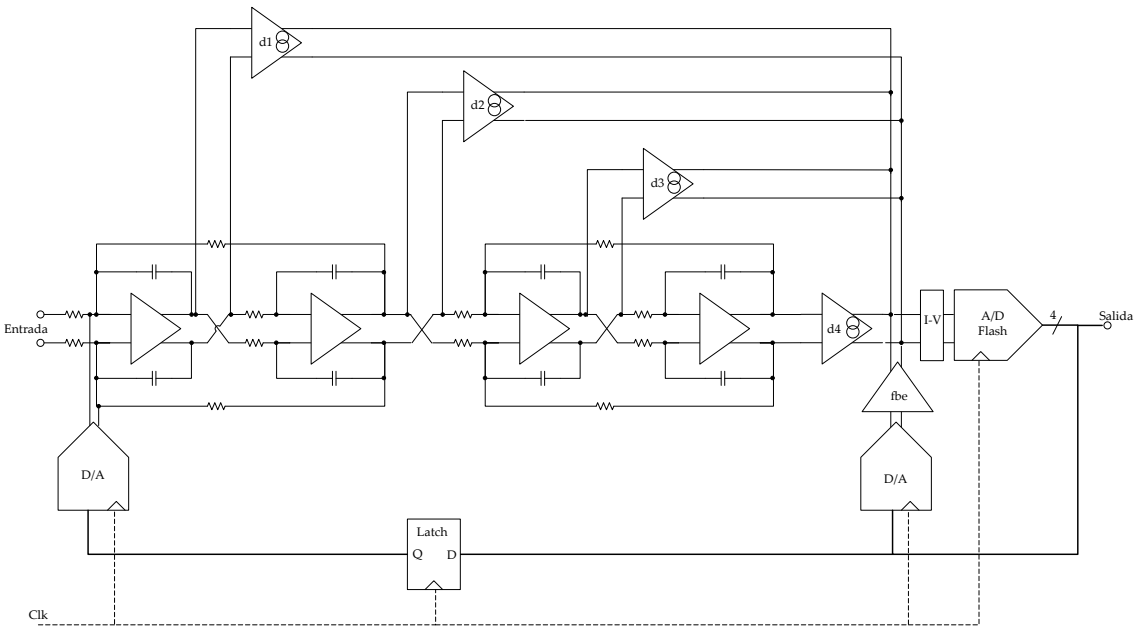

Figure 4.8 Selected architecture.

The selected architecture is shown in fig. 4.8. ABCD matrix is given by (4.1), where c_i corresponds to the gain of integrator i divided by the sampling period, and

g_i corresponds to the ratio between local feedback resistor and input resistor of resonator i.

$$ABCD = \left(\begin{array}{cccc|cc} 0 & -g_1 \cdot c_1 & 0 & 0 & c_1 & c_1 \\ c_2 & 0 & 0 & 0 & 0 & 0 \\ 0 & c_3 & 0 & -g_2 \cdot c_3 & 0 & 0 \\ 0 & 0 & c_4 & 0 & 0 & 0 \\ \hline d_1 & d_2 & d_3 & d_4 & 0 & fbe \end{array}\right) \tag{4.1}$$

4.6 Coefficients setting

According to ABCD matirx in (4.1), there are 4 degrees of freedom in the system. Integrator gains have been selected as parameters, with unity initial value.

The tool and algorithm described in section 3.2.4 were developed after the development of this design. Therefore, the procedure described in [Nor97] was applied.

Results are shown in tables 4.3 and 4.4.

Table 4.3 Initial coefficients set

Coefficients			
c_1	c_2	c_3	c_4
1	1	1	1
d_1	d_2	d_3	d_4
1.27	0.45	0.17	0.02
g_1	g_2		fbe
0.073	0.011		0.7
Maximum stable amplitude (test tone at 2MHz)			
-2dB			

Maximum state-space			
x_1	x_2	x_3	x_4
0.18	0.72	2.37	44.74

Table 4.4 Coefficient set after scaling

Scaled Coefficients			
c_1	c_2	c_3	c_4
1.82	0.36	0.26	0.10
d_1	d_2	d_3	d_4
0.7	0.7	1.0	1.4
g_1	g_2		fbe
0.125	0.394		0.7
Maximum state-space (computed form ABCD matrix)			
x_1	x_2	x_3	x_4
0.324	0.463	0.395	0.765
Maximum state-space (simulated with a -2dB tone at 2MHz)			
x_1	x_2	x_3	x_4
0.331	0.394	0.398	0.783

4.7 Sensitivity to process variations.

Analog phase margin is the selected indicator for stability. Partial derivatives of phase margin may indicate tolerance to process variations. Every coefficient has been evaluated with nominal value to simplify the expressions. Some derivatives are expanded in Taylor series around nominal value. The analysis is valid for around $\pm 20\%$ coefficient variation.

$$\frac{\partial \varphi}{\partial c_1} \approx -11.64 \cdot c_1^2 + 61.20 \cdot c_1 - 92.08 \tag{4.2}$$

$$\frac{\partial \varphi}{\partial c_2} \approx 187.66 \cdot c_2^4 - 122.41 \cdot c_2^3 - 11.44 \cdot c_2^2 - 63.68 \cdot c_2 - 38.23 \tag{4.3}$$

$$\frac{\partial \varphi}{\partial c_3} \approx 9.84 \cdot c_3^3 + 4.93 \cdot c_3^2 + 9.29 \cdot c_3 + 8.13 \tag{4.4}$$

$$\frac{\partial \varphi}{\partial c_4} \approx 2.11 \cdot c_4 + 12.61 \tag{4.5}$$

$$\frac{\partial \varphi}{\partial d_1} = \frac{-11.28}{1.82 \cdot d_1^2 - 0.35 \cdot d_1 + 0.04} \tag{4.6}$$

$$\frac{\partial \varphi}{\partial d_2} = \frac{-114.09}{1.20 \cdot d_2^2 - 2.39 \cdot d_2 + 4.50} \tag{4.7}$$

$$\frac{\partial \varphi}{\partial d_3} = \frac{21.7}{0.34 \cdot d_3^2 - 5.0 \cdot d_3 + 18.22} \tag{4.8}$$

$$\frac{\partial \varphi}{\partial d_4} = \frac{1221.74}{0.34 \cdot d_4^2 - 6.70 \cdot d_4 + 1355.62} \tag{4.9}$$

$$\frac{\partial \varphi}{\partial g_1} \approx 1.11 \cdot g_1^3 + 3.11 \cdot g_1^2 - 4.26 \cdot g_1 - 22.91 \tag{4.10}$$

$$\frac{\partial \varphi}{\partial g_2} \approx 0.07 + 0.005 \cdot g_2 \tag{4.11}$$

$$\frac{\partial \varphi}{\partial fbe} = \frac{156.62}{2.26 \cdot fbe^2 - 2.18 \cdot fbe + 3.83} \tag{4.12}$$

Coefficient *fbe* has special influence on stability. Figure 4.9 shows simulated SNR versus *fbe* variation. Transient simulations were done with a -3dB tone at 7.5MHz.

Figure 4.10 shows simulated SNR versus ELD variation. Transient simulations were also done with a -3dB tone at 7.5MHz.

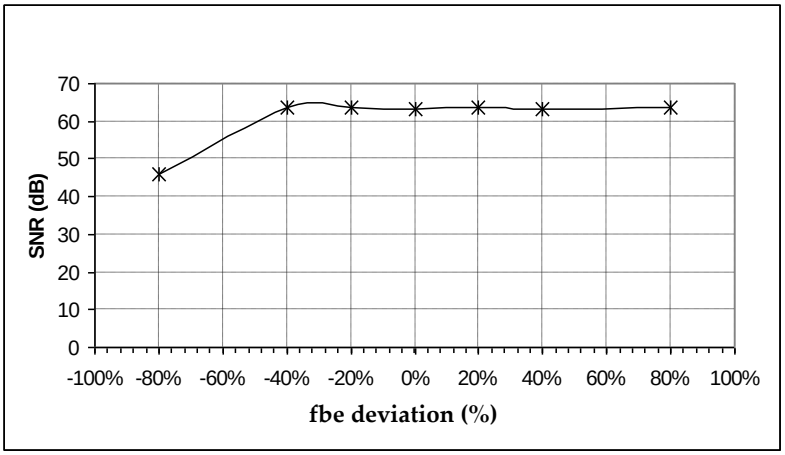

Figure 4.9 Simulated tolerance to fbe variation.

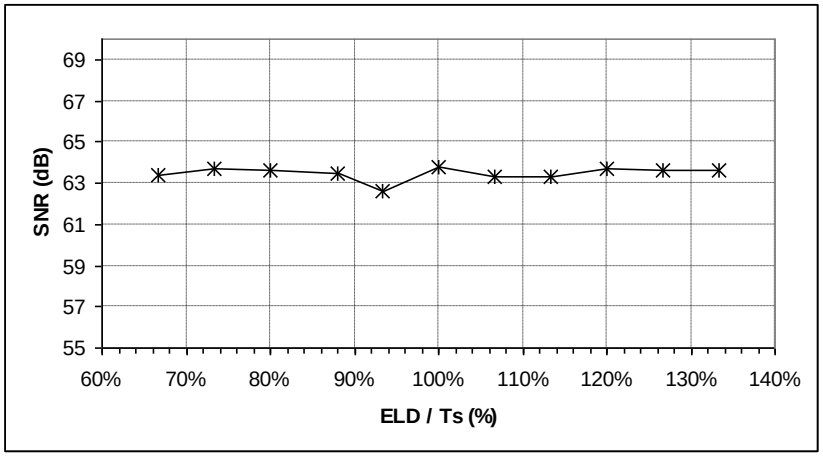

Figure 4.10 Simulated tolerance to ELD

4.8 Sensitivity to D/A non-linearity

The target of this analysis is to specify the linearity of the main D/A converter and decide if a dynamic element matching algorithm is needed.

4.8.1 Behavioral model

D/A converter model consists of $M-1$ unit elements, where M is the number of levels of input code. Each element has a weight w composed of a unitary value with an additive error. The errors are generated by a random variable with a normal distribution $N(0,\sigma)$. D/A uses a selection vector that accomplishes the element

addressing for each one of the input codes. This selection vector may be generated in two ways:

- Linear addressing. This means that D/A has not memory and therefore, it always uses the same element pattern to generate analog output for every possible input-code. The element selection logic is a conventional Thermometer Decoder.
- Data Weighted Averaging. D/A generates analog output using the element addressing algorithm described in [Her03]. This technique implements a first order shaping over the D/A error.

A Simulink model is shown in fig. 4.11.

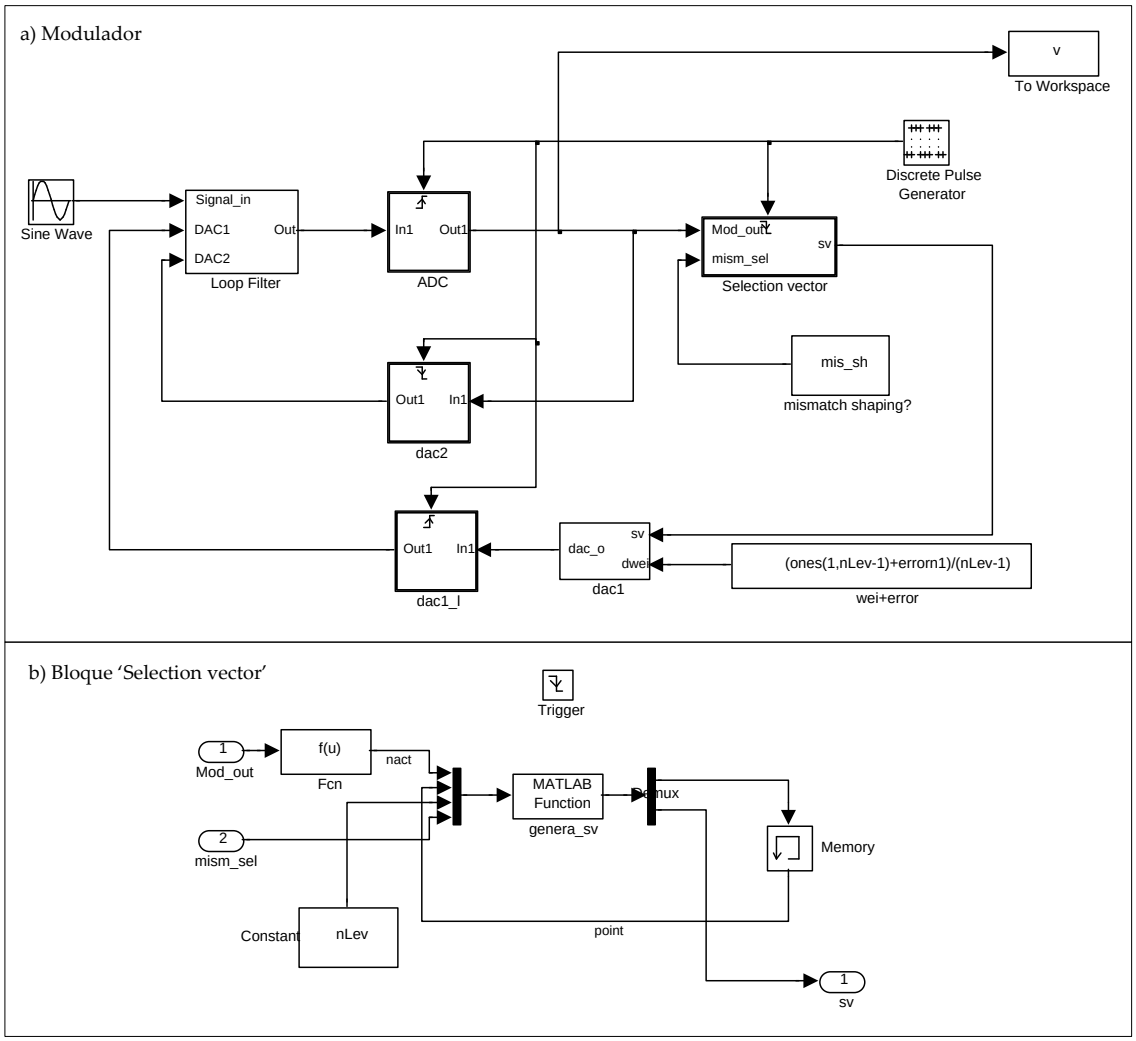

Figure 4.11 Behavioral model with non-linear D/A and dynamic element matching technique.

4.8.2 Simulation results

Some of the results of transient simulations are shown in fig. 4.12. Matching error corresponds to the prediction of the circuit.

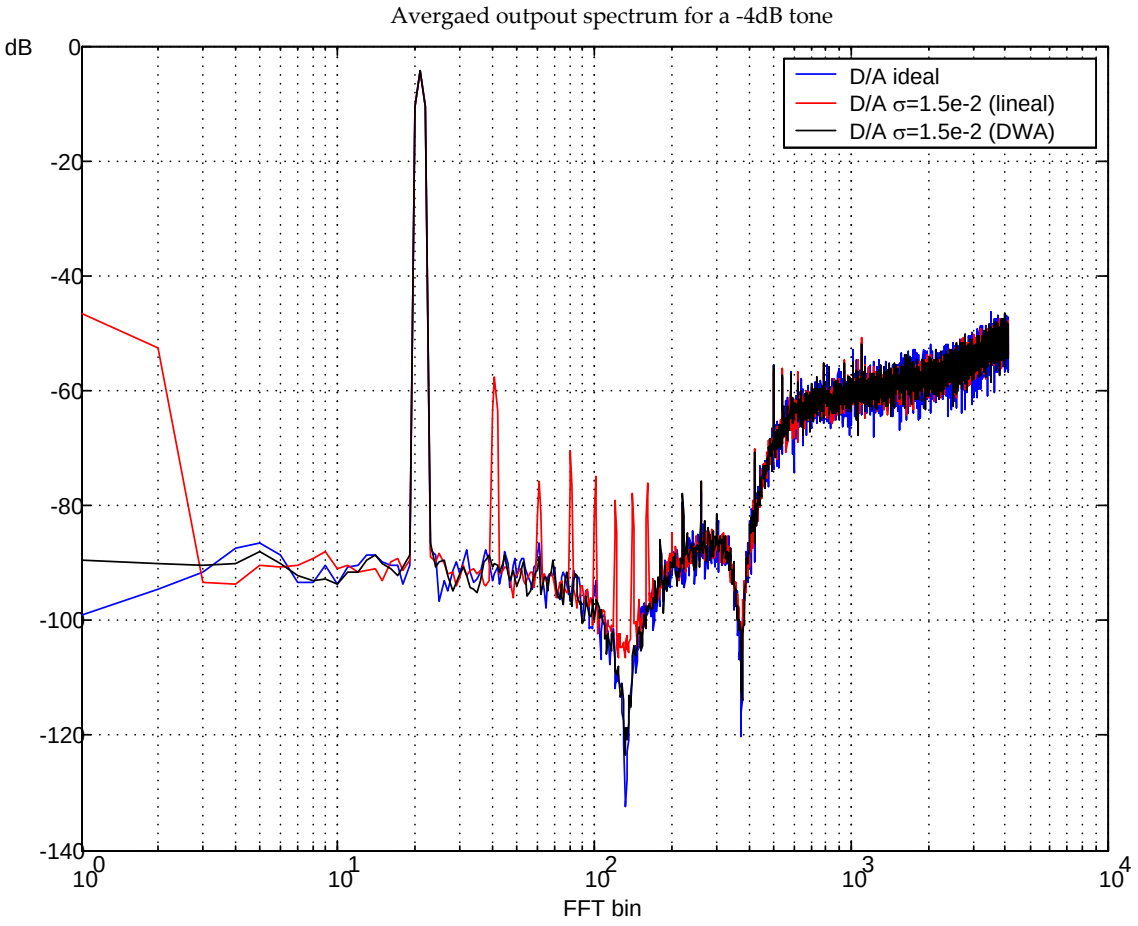

Figure 4.12 Averaged output spectra among 10 8192-points simulations.

4.9 Sensitivity to clock jitter.

The simplified model described in section 2.2.3 has been used to investigate sensitivity to jitter. The model has been simulated with a -3dB test tone at 7.5MHz. SNR decreases 3dB with rms standard deviations around 30ps, as is shown in fig. 4.13.

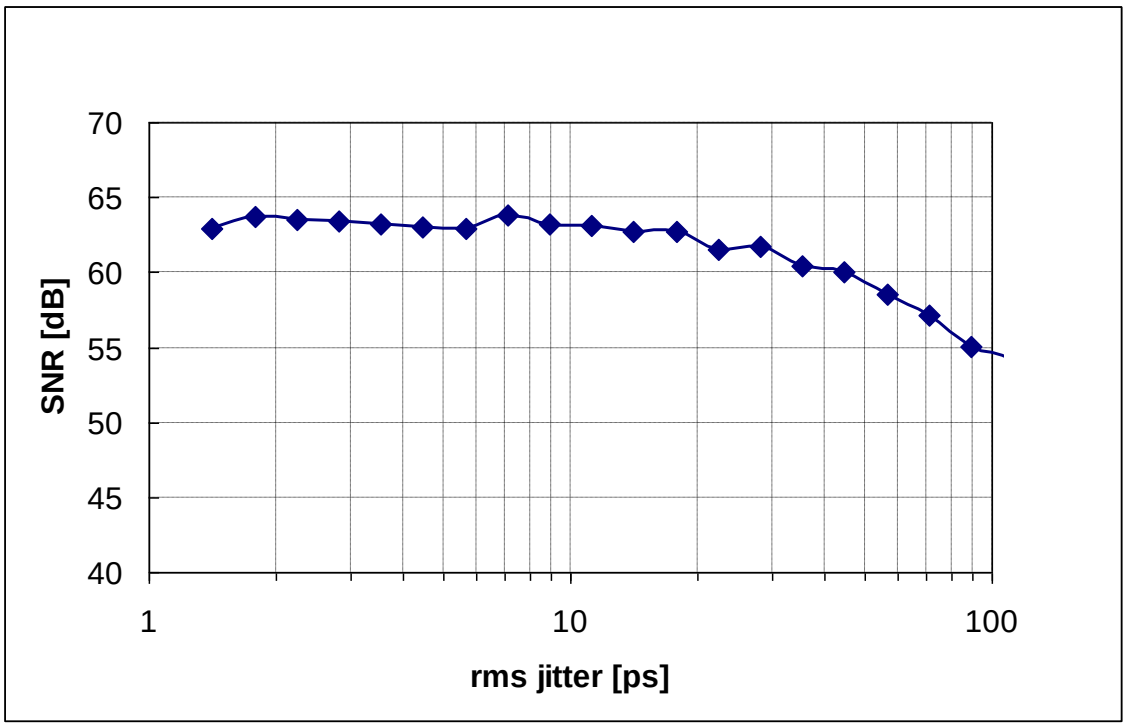

Figure 4.13 Simulated tolerance to clock jitter.

4.10 Circuit blocks

Circuit blocks are described in [Gia03a] and [Gia03b].

Chapter 5

Experimental results

5.1 Chip architecture

The CT-SDM designed as is described in previous chapter has been fabricated in 0.13µm CMOS technology at Infineon Technologies. In order to help the testing of the chip, some programmable and/or auxiliary blocks have been added, as is shown in fig. 5.1.

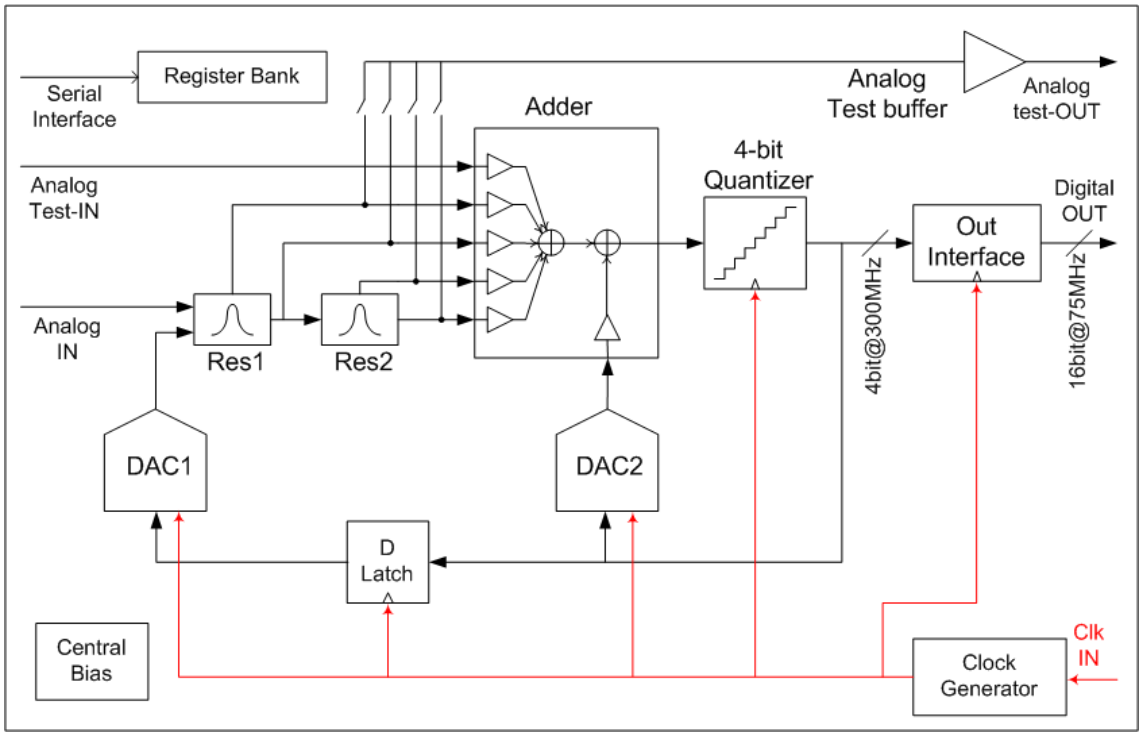

Figure 5.1 Testchip architecture [Gia03a]

Testchip lay-out is shown in fig. 5.2

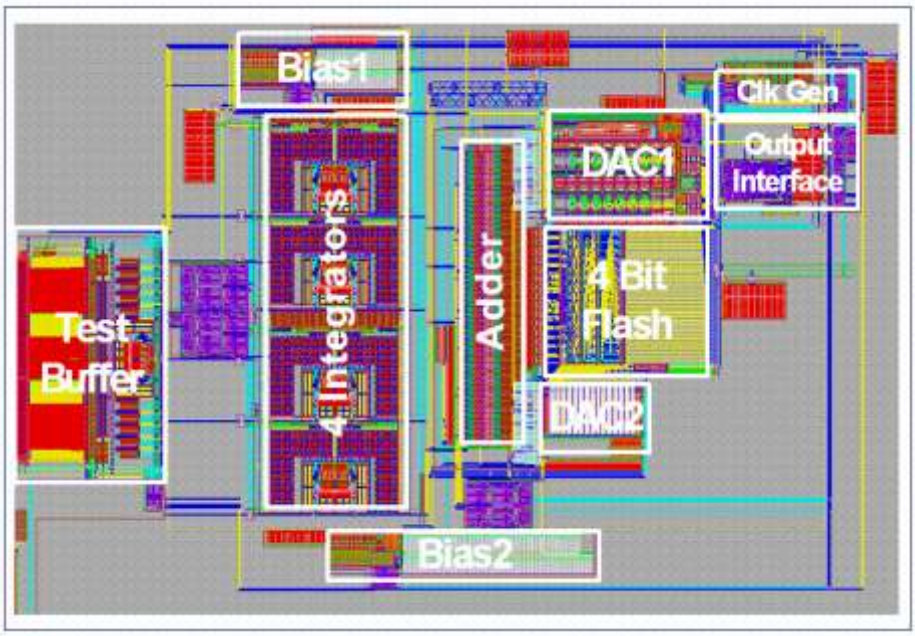

Figure 5.2 Lay-out

5.2 Measurements

The PCB reproduced in fig. has been used for experimental evaluation.

Figure 5.3 PCB photo.

There was a logic analyzer to register modulator output. Measurement data were post-processed in Matlab.

The fabricated CT-SDM is stable when power supply is connected. After that, tuning resonant frequencies of loop-filter is accomplished, and under these conditions the following measurements have been taken.

The measurements included in this chapter are only a proof of concept for the proposed design methodology.

5.2.1 Dynamic Range and SNR

There are several measurements under different conditions in this section.

Figure 5.4 shows the output spectrum for a -10dBFS test tone located at 2MHz. SNR is limited by quantization noise rather than thermal noise. SNDR is 57.2dB, and therefore ENOB is 9.2 bits.

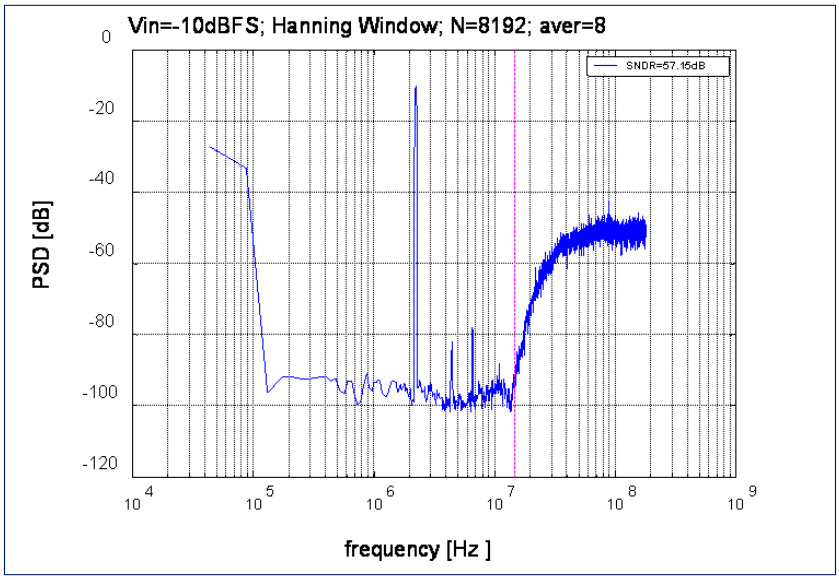

Figure 5.4 Output spectrum with single-tone input

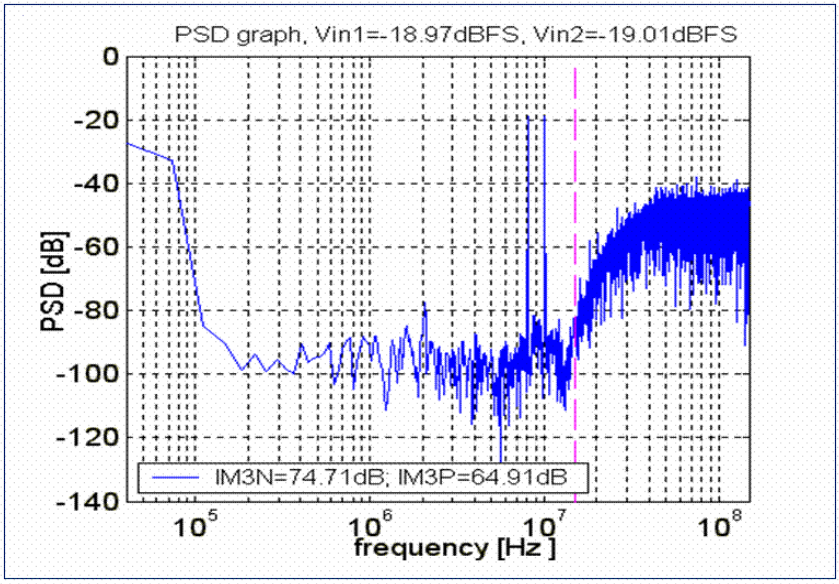

Figure 5.5 Output spectrum with two-tones input

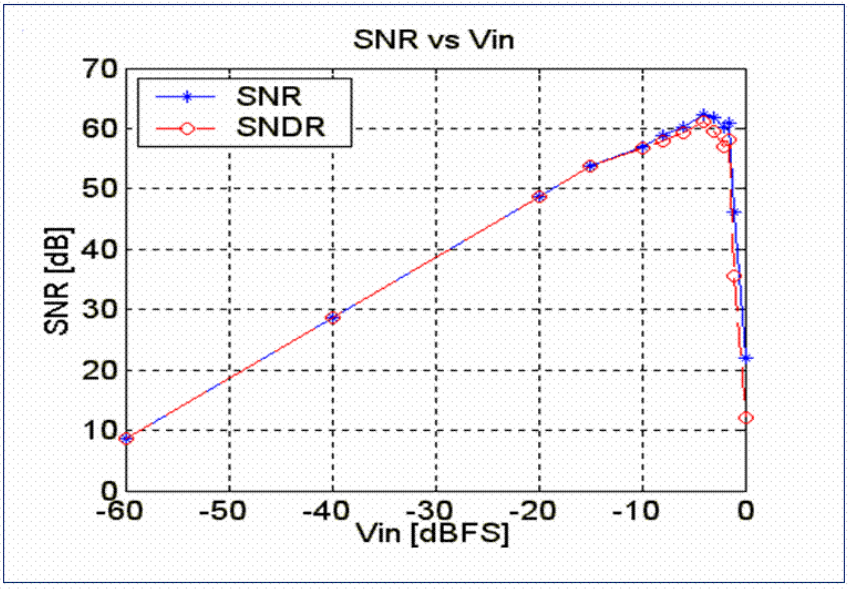

Figure 5.6 Measured Dynamic Range

Figure 5.5 shows the output spectrum for a two-tones input. Intermodulation products are not symmetric.

Figure 5.6 shows the measured dynamic range for a tone located at 7.5MHz. Maximum SNR is 62.5dB and maximum SNDR is 61dB. Dynamic range is 67.5dB.

A summary of the measurements is shown in table 5.1.

Table 5.1 Summary

Analog bandwidth	15MHz
Sampling frequency	300MHz
Dynamic Range	67.5dB
Maximum SNR	62.5dB
Maximum SNDR	61dB
Power Consumption (analog / digital)	65mW / 5mW
Technology	1.5V 0.13μm CMOS

5.2.2 Sensitivity to coefficient variation

Stability against coefficient *fbe* variation has been measured as an example of sensitivity to coefficient variation.

The input of the modulator has been grounded for the measurements. The modulator shows activity on its output due to thermal noise. A stable behavior is considered when output spectrum shows noise shaping and does not show limit cycles. A theoretical dynamic range is also computed on idle-channel output spectrum, as a full-scale tone power divided by the in-band noise power present in the spectrum.

Measurements are shown in fig. 5.7 on grey trace, together with simulated results, on black trace. Simulations models have input cancelled out and a random signal added in front of the quantizer. Random signal has a uniform distribution between $\pm 1/15$. Dynamic range values have been computed in the same way than that of measurements.

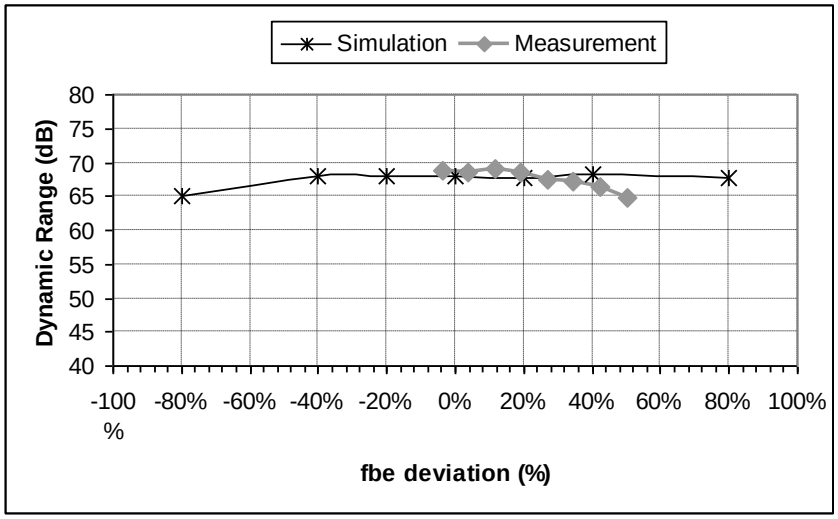

Figure 5.7 Dynamic range of stable modulators against fbe variation

5.2.3 Sensitivity to excess-loop delay

The same kind of measurements than that of previous section has been performed to evaluate ELD impact on stability.

Measurements have been taken on idle-channel output spectrum and plotted in fig. 5.8 on grey trace. Black trace corresponds to simulated values.

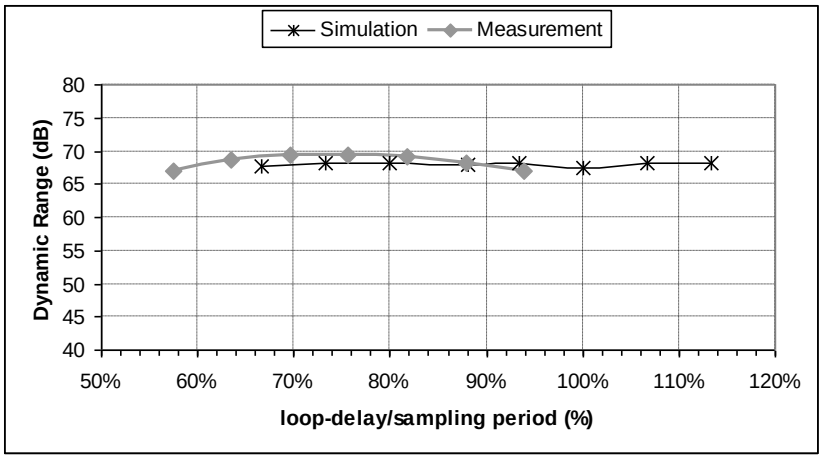

Figure 5.8 Dynamic range of stable modulators against excess-loop delay variation.

It has to be pointed out that the modulator becomes unstable for lower ELD values than that of simulation predictions. Even so, the modulator remains stable and holds a certain dynamic range for a wide range of ELD values.

5.2.4 Sensitivity to clock jitter

Phase noise has been added to clock by means of a transformer and a variable voltage source. The amount of phase noise introduced has been measured with a jitter analyzer and a spectrum analyzer.

The measurements have been taken in idle-channel mode, such that the modulator is in the same conditions described in 2.2.2. Theoretical dynamic range has been computed from idle-channel output spectrum as was described in previous sections.

The result is shown in fig. 5.9. Pink trace corresponds to the measurements. Blue trace corresponds to simulated values with the fast model reported in 2.2.3. Black trace corresponds to the computation of the theoretical maximum dynamic range of the output of a 300MHz sampler when a full-scale tone at 15MHz is at the input of the sampler. A modulator with the same input cannot be placed above this curve. The same modulator in idle-channel mode should be placed as closer as possible to this curve.

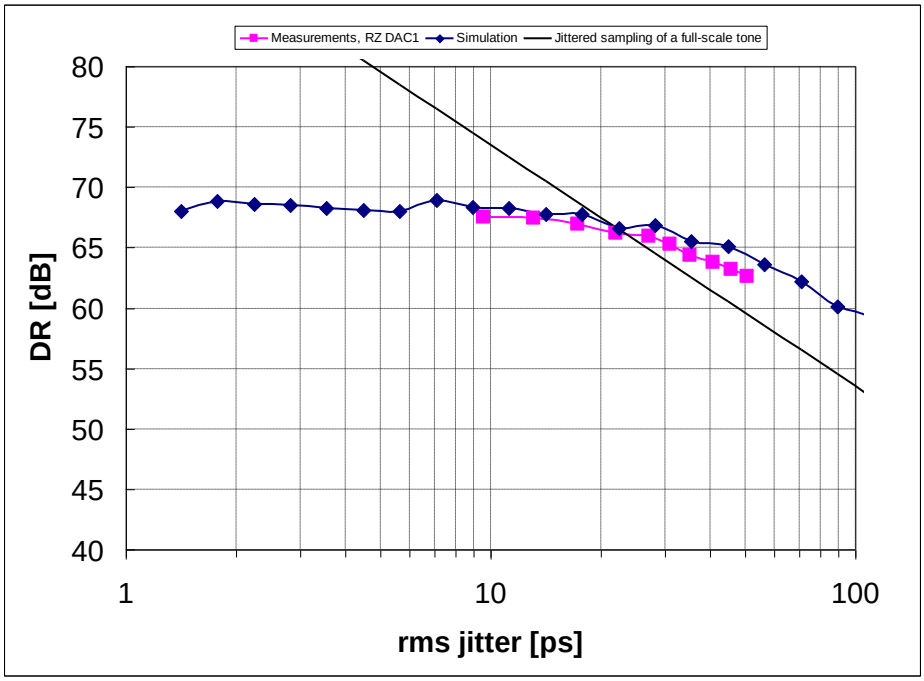

Figure 5.9 Clock Jitter sensitivity

It has to be pointed out that simulated and measured curves are very close, with differences between 1 and 2 dB, and are also very close to the theoretical limit. Dynamic range decreases 3dB for 30ps rms jitter.

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• Publications of the author connected with this dissertation

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- S. Paton, A. Di Giandomenico, L. Hernandez, A. Wiesbauer, T. Pötscher and M. Clara. "A 70mW 300MHz CMOS continuous-time ΣΔ ADC with 15MHz bandwidth and 11 bits of resolution". *IEEE J. Solid-State Circ.*, pp 1056-1063, Jul 2004

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