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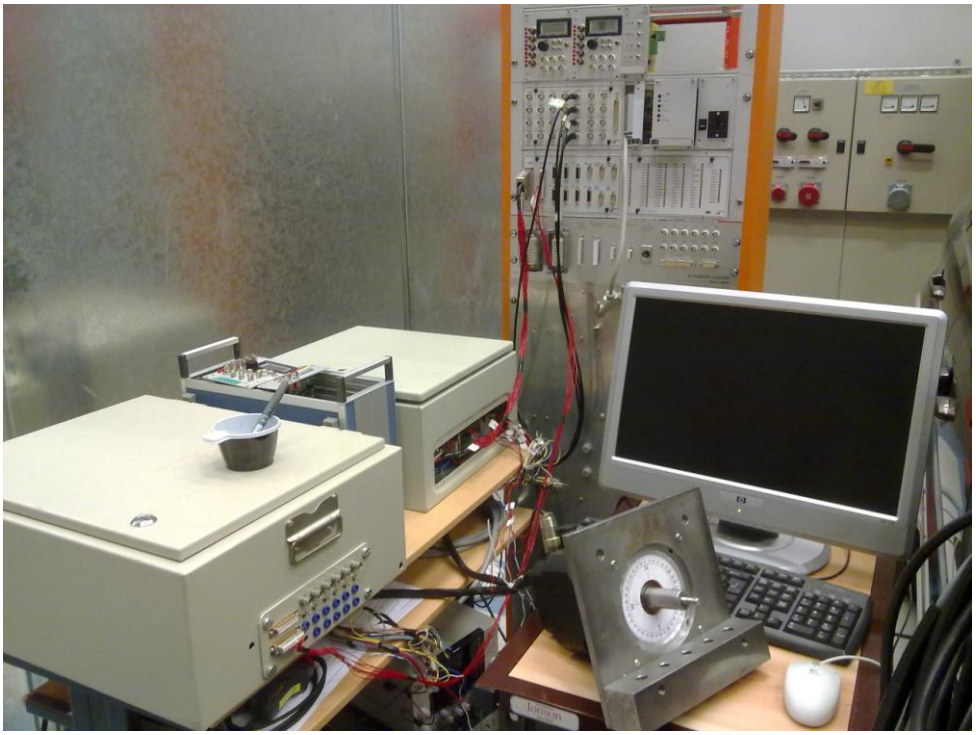

Design, Simulation and Implementation of a PMSM Drive System

Thesis for the Degree of Master of Science in Engineering

DAVID VINDEL MUÑOZ

Division of Electric Power Engineering
Department of Energy and Environment
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Cover:
Picture of the experimental drive system setup

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Somehow, I have to express here my acknowledgement to so many people in Spain. To all these special people, with whom I have spent my life, thanks for all the unforgettable moments we have lived together.

Finally, thank my family because they make this real. An entire life support is priceless. Love you Padres!

Göteborg, May 2011

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ABSTRACT

Field oriented control (FOC) of permanent magnet synchronous motor (PMSM) is one of the widely used methods for the speed control of the motor. A PMSM drive system based on FOC is designed, simulated and implemented.

The whole drive system is simulated in Matlab/Simulink based on the mathematical model of the system devices including PMSM and inverter. The aim of the drive system is to have speed control over wide speed range. Simulation results show that the speed controller has a good dynamic response.

A lab setup is designed and implemented based on a six-pole 2 *kW* PMSM. The measurement devices, voltage transducers, current transducers and resolver, are explained in this report. For the system control dSpace is used and Matlab/Simulink is used for the program development and implementation.

Experimental results show that the drive system has a good dynamic response in terms of speed response and torque ripple. The drive system will be extended to serve as an isolated high power battery charger.

Key words: PMSM, FOC, Drive System, Isolated Charger.

Table of Contents

1 Introduction

The project background, objective of the project and the thesis outline is described in this introductory chapter.

1.1 Background of the study

Many types of electric motors have been used in the industry for different purposes: cranes, spinning machines, public transportation and so on [3]. AC motors are widely used and ac drives are subject of study for many researchers [4, 13]. Recently, ac drives in vehicle applications are gaining attention due to pollution and fuel price problems.

In the electrical system of an electric or hybrid electric vehicle based on an ac motor, the motor is producing torque from the battery through the inverter. To charge the battery the grid power is utilized in some vehicles called grid-connected version. Since the battery charging and traction power is not happening simultaneously it is possible to use inverter and motor in charger circuit to reduce the price, volume, weight and space of the charger. This is called integrated charger.

An isolated high power integrated charger is proposed in [9] that is based on a special ac motor winding configuration. To implement a practical system of the proposed integrated charger, this current subproject is defined to be extended later on.

1.2 Objectives of the study

The goal of this thesis is to design and implement a normal drive system of a permanent magnet synchronous machine (PMSM). The stator has double set of winding as explained in [12]. Later on the system will be used as an integrated charger.

The drive system simulation and the hardware implementation is explained in this thesis.

The simulations are conducted in Matlab/Simulink software. Based on the simulation results, a practical system is designed and implemented that is explained in the report. dSpace control system is used to control the whole drive system.

1.3 Outline of the thesis

After this introduction chapter, the mathematical model of PMSM and the field oriented method is explained in chapter 2. Chapter 3 includes design and description of the practical system. Conclusion and future works are presented in chapter 4.

Several appendices are added to the report as a part of the thesis. Reference frame theory, Matlab code used for the simulations, as well as the Simulink blocks of every subsystem, the lab setup diagrams and components datasheets and dSpace programming are presented in appendices.

2 Modelling and field oriented control of permanent magnet synchronous machine

Permanent magnet synchronous motors (PMSM) have attracted increasing interest in recent years for industrial drive applications [3]. The high efficiency, high steady state torque density and simple controller of the PM motor drives compared to the induction motor drives make them a good alternative in certain applications.

Other advantages of the PMSM are low inertia, high efficiency, reliability and low cost of the power electronic converters required for controlling the machine [1]. All these facts make the PMSM an excellent candidate for being used in many applications.

We can distinguish between two main kinds of PMSM: internal-mounted magnets (with saliency, IM) or surface-mounted magnets (without saliency, SM). The main difference is that the IM machine has a variable reluctance which varies with the rotor angle, while the SM machine has quite a fixed reluctance for any rotor angle. That leads in a uniform air gap, and thus, an equal magnetizing inductance for the direct and quadrature axis (L_d and L_q) [2].

Field oriented control of PMSM is one of the widely used methods in drive applications [14] that is considered in this thesis. A mathematical model of PMSM is introduced in this chapter first. Then the FOC method is explained. Finally Matlab/Simulink based simulation results are presented for this scheme.

2.1 Mathematical model of PMSM

A surface-mounted synchronous machine is used in this project, so the mathematical model of the PMSM is presented for this kind of machine.

Figure 2.1 show a cross section of the rotor and stator of a PMSM.

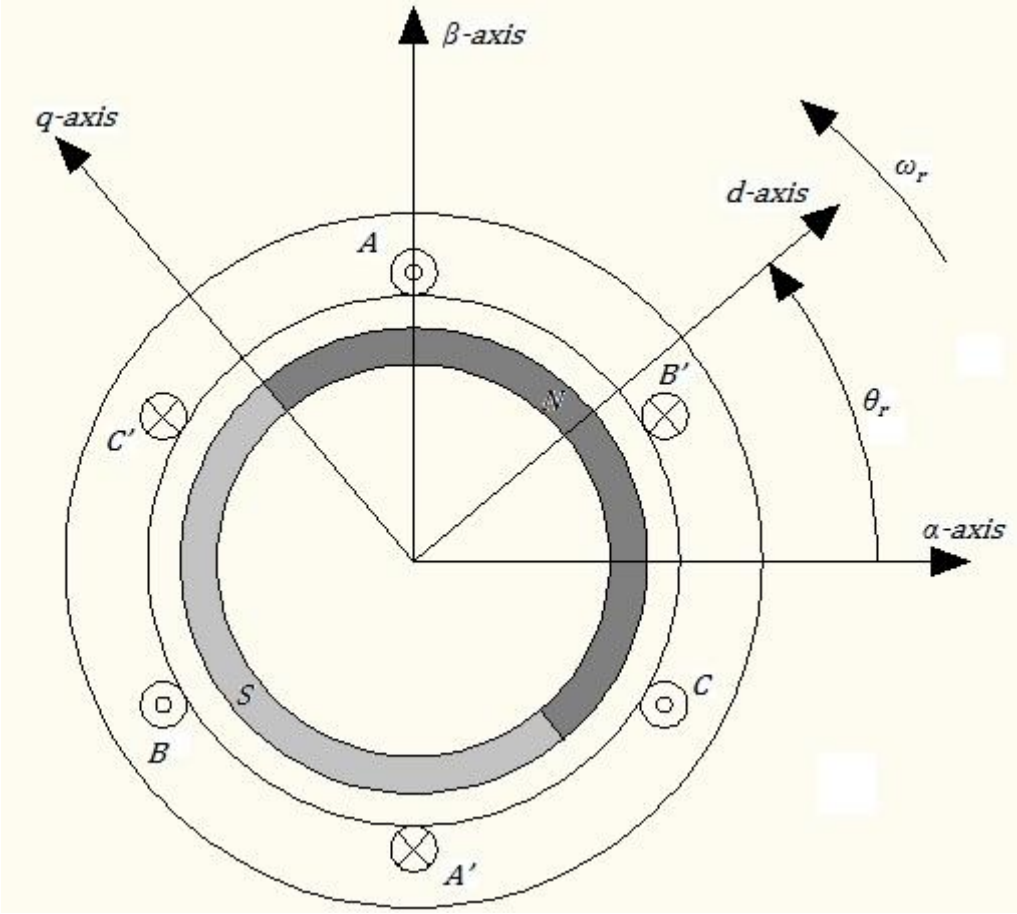


Figure 2.1: View of a three phase, two-pole PMSM.

Considering a two-pole three phase PMSM, the voltage equation in the dq domain (reference frame transformation is explained in *Appendix A. Reference frame conversion*) is expressed as follows [2]:

$$\overrightarrow{u_{dq0s}} = R_s\overrightarrow{\imath_{dq0s}} + p\overrightarrow{\lambda_{dq0s}} \tag{2.1}$$

Where p is the differentiating operator d/dt. The indexes *d*, *q* and *0* denote direct axis, quadrature axis and zero component of the variables respectively. The flux linkage in the *dq* frame can be calculated as follows:

$$\overrightarrow{\lambda_{dq0s}} = L_{dq0}\overrightarrow{\imath_{dq0s}} + \overrightarrow{\lambda_{dq0,m}} \tag{2.2}$$

Where the inductance matrix is expressed:

$$\mathrm{L}_{dq0} = \begin{bmatrix} L_d & 0 & 0 \\ 0 & L_q & 0 \\ 0 & 0 & L_0 \end{bmatrix} = \begin{bmatrix} L_s & 0 & 0 \\ 0 & L_s & 0 \\ 0 & 0 & L_0 \end{bmatrix} \tag{2.3}$$

For SMPM, the *d* and *q* components of the inductances are the same. The notation *dq* is change for *s*, which refers to the stator. The magnetizing flux has the following expression:

$$\lambda_{dq0,m} = \begin{bmatrix} \lambda_{pm} & 0 & 0 \end{bmatrix}^T \tag{2.4}$$

A usual way to write the equation (2.1) is in its expanded form. As far as the stator windings are wye-connected (with a neutral point) and supplied with balanced three phase currents, the zero-axis components are neglected [2]. The voltage equations for d and q axes are:

$$u_{ds} = R_s i_{ds} + L_s \frac{di_{ds}}{dt} - \omega_r L_s i_{qs} \tag{2.5}$$

$$u_{qs} = R_s i_{qs} + L_s \frac{di_{qs}}{dt} + \omega_r \left(L_s i_{ds} + \lambda_{pm} \right) \tag{2.6}$$

Where R_s is the stator resistance, L_s the stator inductance, ω_r the rotor rotational speed and λ_{pm} the permanent magnet flux.

The electromagnetic torque of the machine can be expressed, in the *dq* reference frame, as follows:

$$T_e = \left(\frac{3}{2}\right)\left(\frac{P}{2}\right)\left(\lambda_{ds} i_{qs} - \lambda_{qs} i_{ds}\right) \tag{2.7}$$

If the equation (2.2) is substituted in the torque equation, it is obtained:

$$T_e = \left(\frac{3}{2}\right)\left(\frac{P}{2}\right)\left(\lambda_{pm} i_{qs} - \left(L_q - L_d\right) i_{qs} i_{ds}\right) \tag{2.8}$$

Considering a non-salient rotor, where the inductances are equal, the final expression of the electromagnetic torque is:

$$T_e = \left(\frac{3}{2}\right)\left(\frac{P}{2}\right)\lambda_{pm} i_{qs} \tag{2.9}$$

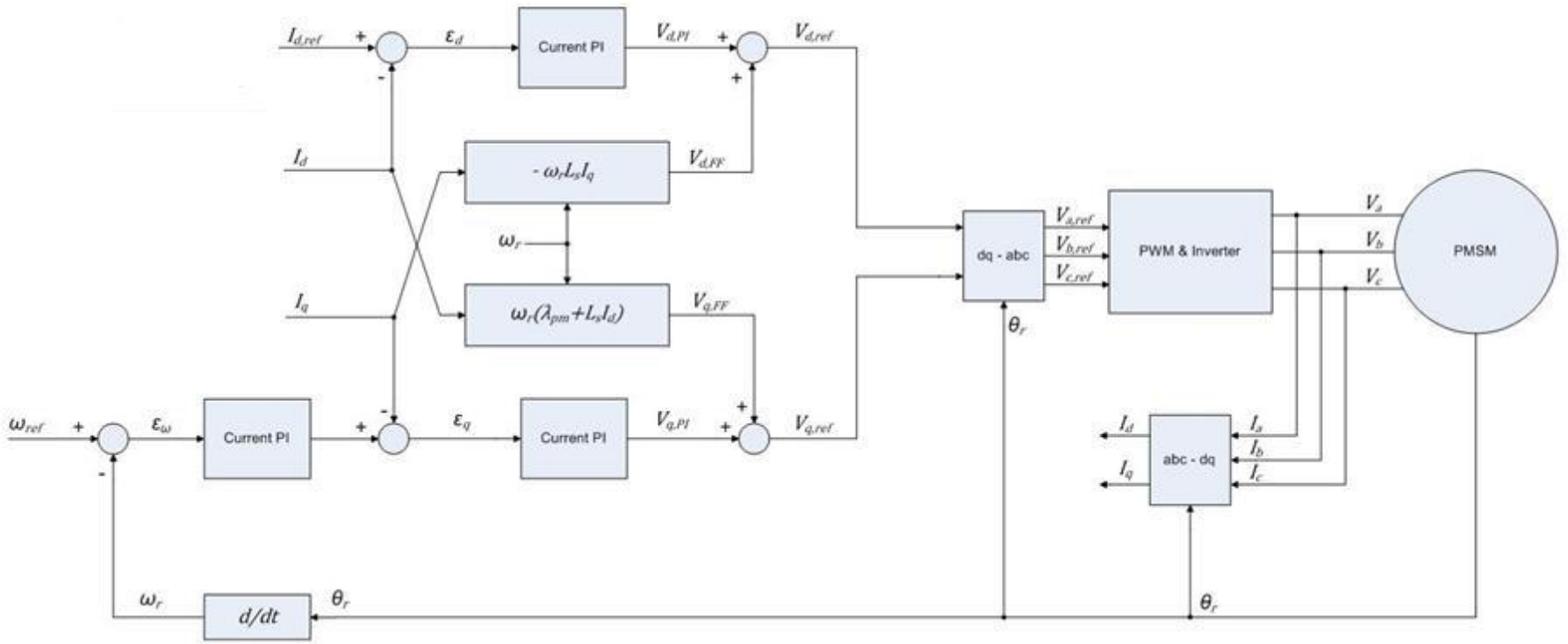
This result is quite interesting. It shows that the only component involved in torque production in a PMSM without saliency is the stator q-axis current.

2.2 Field oriented control of PMSM

Field oriented control of PMSM is one important variation of vector control methods [14]. The aim of the FOC method is to control the magnetic field and torque by controlling the d and q components of the stator currents or relatively fluxes.

With the information of the stator currents and the rotor angle a FOC technique can control the motor torque and the flux in a very effective way. The main advantages of this technique are the fast response and the little torque ripple [5].

The implementation of this technique will be carried out using two current regulators, one for the direct-axis component and another for the quadrature-axis component, and one speed regulator. Figure 2.2 shows a block diagram of the FOC method.



CHALMERS ELTEKNIK Department of Energy and Environment Division of Electric Power Engineering	TITLE Design, simulation & implementation of a PMSM drive system	DESCRIPTION Diagram of FOC for PMSM	FULL FILENAME Diagram of FOC for PMSM.vsd					
			DRAWN BY David Vindel	CHECKED BY	SCALE 1:1	DATE 2011-03-31	REVISED	PAGE 1 OF 1

Figure 2.2: Diagram of the implemented FOC with feedforward compensation.

As shown in the figure, there are three PI regulators in the control system. One is for the mechanical system (speed) and two are for the electrical system (d and q currents).

At first, the reference speed, ω_{ref}, is compared with the measured speed, ω_r, and the error signal, ε_ω, is fed to the speed PI controller. This regulator compares the actual and reference speed and outputs a torque command. The torque is related to the speed by the mechanical equation of the motor:

$$\frac{d\omega_r}{dt} = \frac{1}{J}(T_e - T_m - B\omega_r) \tag{2.10}$$

Where J is the inertia of the motor, B is the viscous coefficient, T_m is the mechanical torque applied in the shaft (load) and T_e is the electrical torque developed by the motor.

Once is obtained the torque command, with the equation (2.9) can be turned into the quadrature-axis current reference, $I_{q,ref}$ [2].

There is a PI controller to regulate the d component of the stator current. The reference value, $I_{d,ref}$, is zero in this thesis since there is no flux weakening operation. The d component error of the current, ε_d, is used as an input for the PI regulator. Moreover, there is another PI controller to regulate the q component of the current. The reference value is compared with the measured and then fed to the PI regulator.

Feedforward compensation is used in d and q PI regulators according to equations (2.5) and (2.6), to enhance the system performance.

The PI outputs, $V_{d,ref}$ and $V_{q,ref}$, are first transformed to *abc* domain by the use of inverse Park and Clark transformations (see *Appendix A. Reference frame conversion*). Then, those reference voltages are used by the PWM unit to generate the inverter's command signals.

The tuning of the PI's (setting the P and I parameters) has been carried out with the following method proposed by [7].

$$\alpha_{current} = {}^{2\pi f_s}/_{10} \tag{2.11}$$

$$\alpha_{speed} = {}^{\alpha_{current}}/_{10} \tag{2.12}$$

$$K_{Pd} = \alpha_{current} \cdot L_d \tag{2.13}$$

$$K_{Id} = \alpha_{current} \cdot R_s \tag{2.14}$$

$$K_{Pq} = \alpha_{current} \cdot L_q \tag{2.15}$$

$$K_{Iq} = \alpha_{current} \cdot R_s \tag{2.16}$$

$$K_{P\omega} = \alpha_{speed} \cdot J \tag{2.17}$$

$$K_{I\omega} = \alpha_{current} \cdot B \tag{2.18}$$

Where $\alpha_{current}$ amd α_{speed} are the controller's bandwith and f_s is the switching frequency of the inverter (same as the sampling frequency of the system).

All the current and speed regulators have been implemented taking care of the torque and voltage limits. A saturation block has been included to avoid exceeding the maximum torque and voltages allowed in the machine. When these limits are reached, the regulators control that the torque or voltage values do not overpass their maximum values. This causes a problem, a large overshoot of the current values caused by the integrator windup. The integral term of the regulator keeps accumulating the error during the time of maximum voltage output, and when the value of the current reaches its maximum, the integrator has wound up so that the voltage remains large [7].

To prevent this problem, anti-windup technique is used in the controllers. The reference value of torque or voltage is used to update the integral term of the regulator. As it can be seen in the Simulink block diagram, as far as the voltage command is below its maximum value, the anti-windup loop returns a zero value to the integrator. But whenever this value is overcome, a proportional value of the difference is added to the integrator, so the response of the regulator is faster [7].

To conclude with this chapter, the performance of the FOC block diagram can be summarized in the following steps [6]:

1. The stator currents are measured as well as the rotor angle.
2. The stator currents are converted into a two-axis reference frame with the Clark Transformation.
3. The $\alpha\beta$ currents are converted into a rotor reference frame using Park Transformation. This *dq* values are invariant in steady-state conditions.
4. With the speed regulator, a quadrature-axis current reference is obtained (the direct-axis reference is zero for operation below rated speed). The d-current controls the air gap flux, the q-current control the torque production.
5. The current error signals are used in controllers to generate reference voltages for the inverter.
6. The voltage references are turned back into *abc* domain.
7. With these values are computed the PWM signals required for driving the inverter.

2.3 Simulation results

Once reviewed all the theoretical aspects involved in this thesis, an implementation of the whole system is be done using the software tool Matlab and Simulink.

Each subsystem such as motor, inverter, PWM generation, speed controller...etc, have its own model in Simulink, according to their fundamental equations. Finally, the motor parameters, as well as other needed parameters to run the PI's or the inverter is set in a Matlab file that runs before starting the simulation (see *Appendix B. Matlab code and Simulink diagram blocks*).

The whole system is composed of the controller block, the motor block, the inverter and the reference frame transformation blocks. The control parameters are presented in Table 2.1 and the motor parameters are shown in Table 2.2.

Inverter model

Figure 2.3 shows the inverter's Simulink model. One switch per phase is used to set Vdc or –Vdc on the phase. As an activation signal for each switch is used the PWM signal.

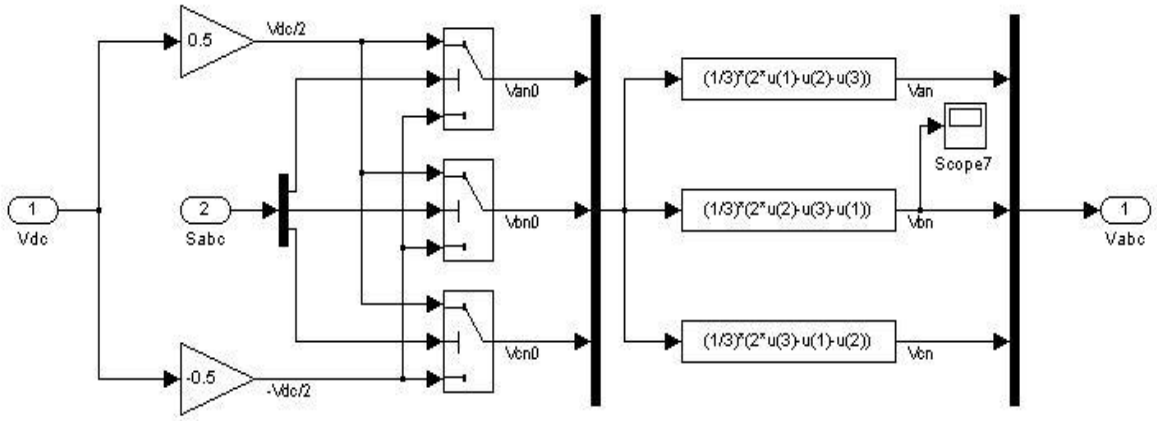


Figure 2.3: Simulink model of the inverter.

Motor model

The motor equations explained before are used to establish the motor model in Simulink. Figure 2.4 shows the motor model used.

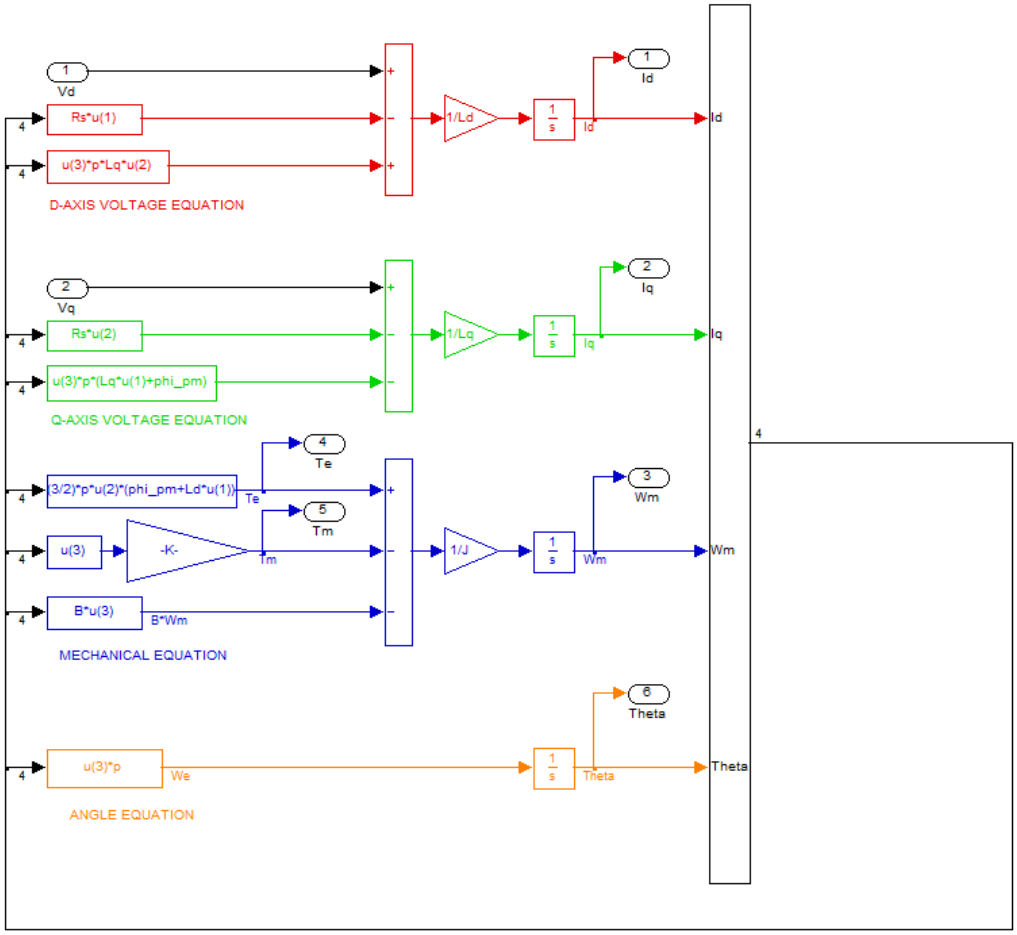


Figure 2.4: Simulink model of the PMSM.

Controller model

In Figure 2.5 the whole controller system is presented. The proportional, integral and anti windup parts as well as a saturation blocks for the torque limit are shown in the figure.

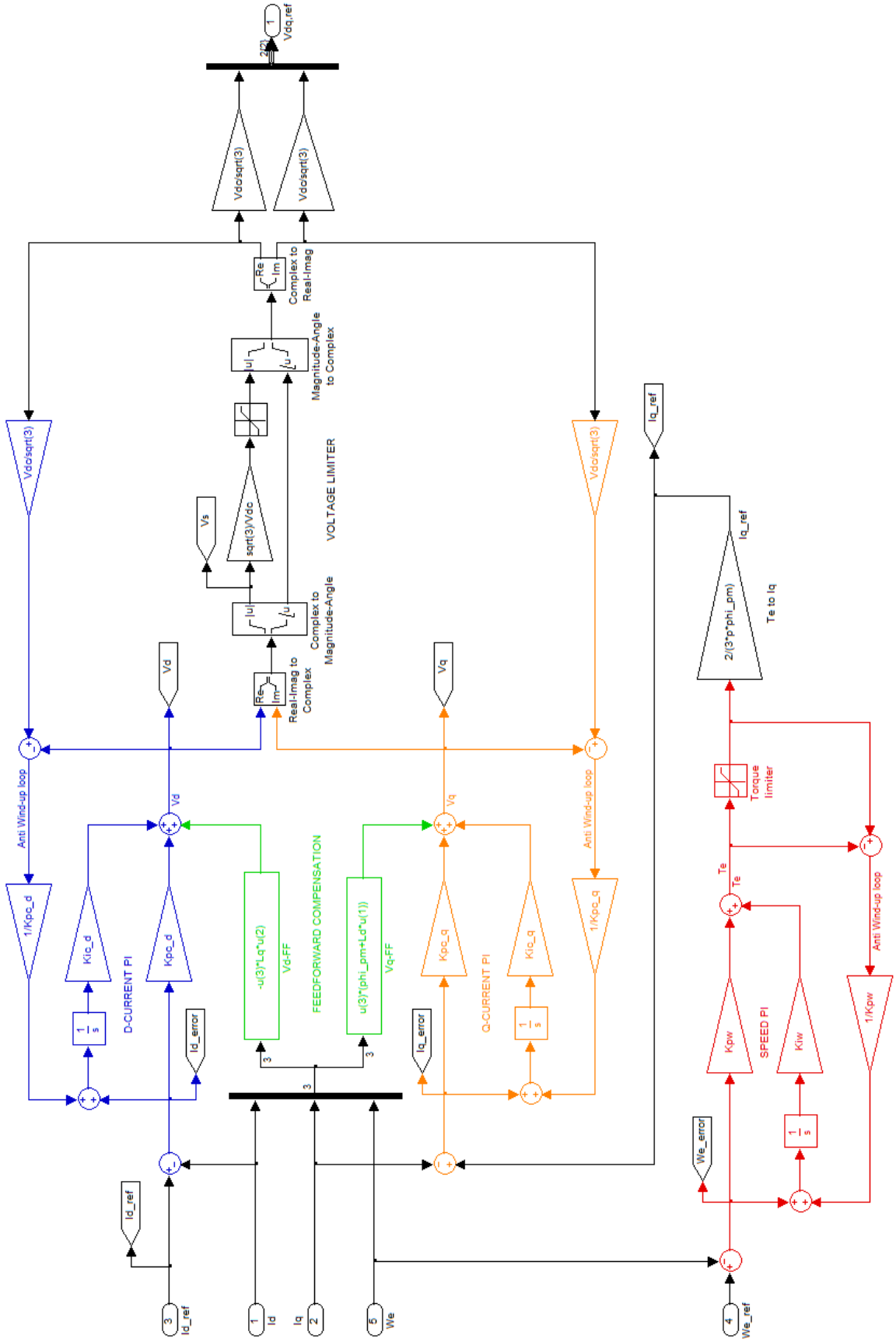


Figure 2.5: Control diagram for FOC of PMSM.

Table 2.1: Control parameters

Parameter	Unit	Value	Description
fs	Hz	5.000	Switching frequency
Vdc	V	400	DC bus voltage
Kpc_d	--		Proportional constant of d-axis current regulator
Kic_d	--		Integral constant of d-axis current regulator
Kpc_q	--		Proportional constant of q-axis current regulator
Kic_q	--		Integral constant of q-axis current regulator
Kpw	--		Proportional constant of speed regulator
Kiw	--		Integral constant of speed regulator
Id_ref	A	0	d-axis current command
1st step.value	rad/s	34,906	Speed reference for the first step
1st step.time	s	0	Time when first step happens
2nd step.value	rad/s	17,453	Speed reference for the second step
2nd step.time	s	3	Time when the second step happens
***Variable step, max step size of 5e-5 s, solver ode45**			

Table 2.2: Motor parameters.

Parameter	Unit	Value	Description
Rs	Ω	7,1	Stator resistance
Ld	H	30e-3	Direct-axis inductance
Lq	H	30e-3	Quadrature-axis inductance
p	--	3	Pole pairs
phi_pm	Vs	0,12	Permanent magnet flux
B	Ns/m	0,002	Viscous coefficient
J	kgm^2	5,8e-4	Inertia

Simulation Results

Now, the results of the simulation are presented.

Figure 2.6 shows the speed response of the system due to a step change in the command. The electrical torque and the stator currents are shown in Figure 2.7, Figure 2.8 and Figure 2.9 respectively.

As it is shown in these figures, the system has a good dynamic response.

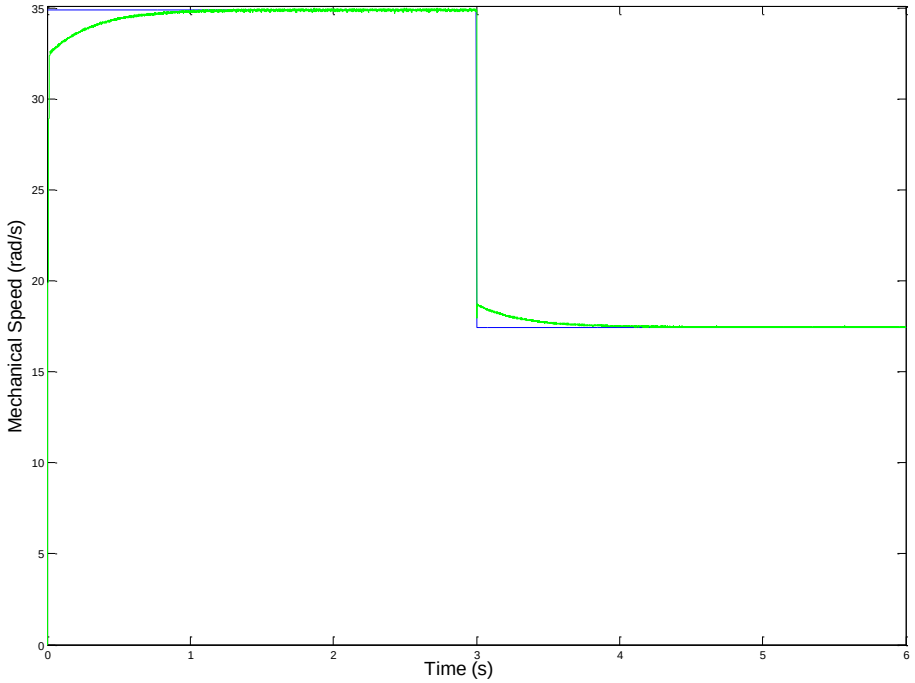


Figure 2.6: Mechanical speed (command in blue, actual in green).

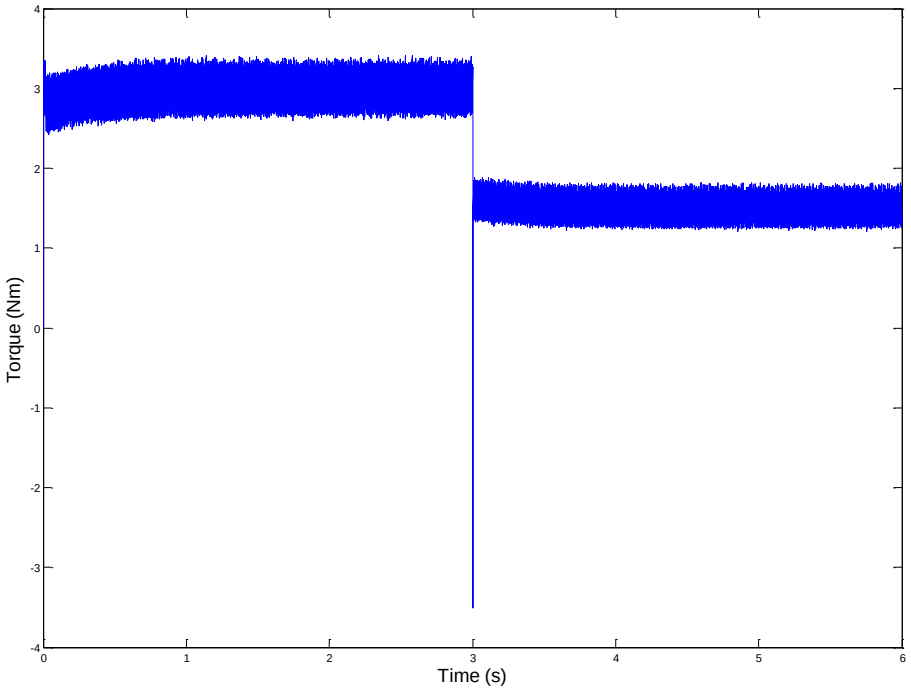


Figure 2.7: Electrical torque.

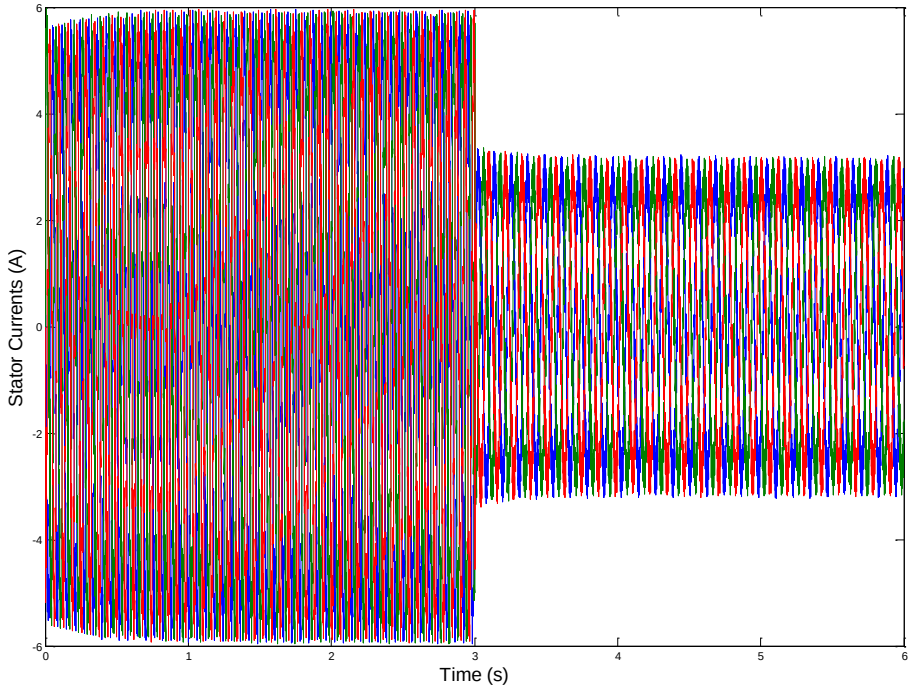


Figure 2.8: Motor stator current in abc domain.

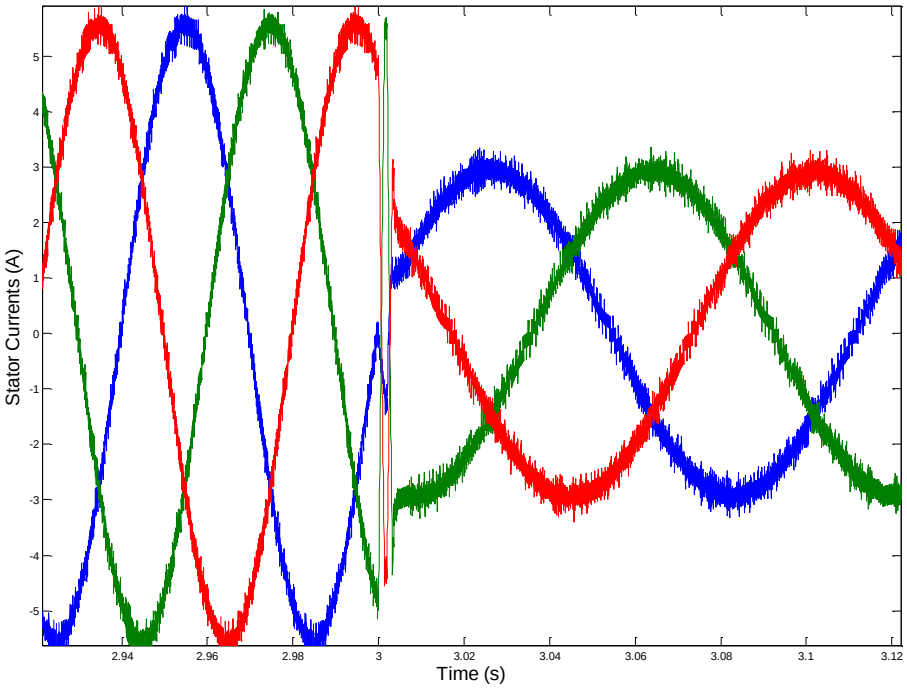


Figure 2.9: Motor stator currents due to a speed step change.

3 Practical implementation of a PMSM drive system

An experimental system is designed to implement FOC of IPM that is explained in this chapter. System architecture is presented firstly. Afterwards, the hardware components are presented. Practical measurements results are added also.

3.1 General hardware overview

Figure 3.1 shows a simple schematic diagram of the system. The equipments used in the lab setup of this thesis are listed below:

- Permanent magnet synchronous machine
- Inverter
- Voltage, current, rotor angle and speed measurement equipments
- dSpace DS1103 control system
- 24V relay
- An optocard for over current protection
- Various electrical items such as wires, connectors, grounding and so on

All these equipment are installed/organized in the following way:

- A measurement box that includes:
  - DC voltage source that provides the equipments with $\pm 15V$
  - Three voltage transducers UMAT2 with three channels for voltage measurements each one
  - Seven current sensors LEM LA 50-S for current measurements
  - A resolver-to-digital converter that measures rotor angle and speed
  - Connector terminals to electrically link different components
- The inverter box which includes:
  - A $\pm 15V_{DC}$ voltage source that supplies the inverter control system
  - A $24V_{DC}$ voltage source that feeds the grid contactor
  - A four leg switch-mode inverter that uses Mosfet switches (one leg is spare)
  - A relay (C3-A 30) for the PMSM secondary winding connection to the grid
  - A designed electronic board to drive the relay
- The PMSM with double stator windings and the resolver already installed on the shaft. Resolver coils are available from the motor through a 12-pin connector installed in the motor housing.
- Control system is based on the dSpace, including the following parts:
  - Two CP1103 dSpace board with analog and digital I/O
  - A CLP1103 dSpace board with luminous LEDs that show the state of the different signals

- The optocard, that in case of over current in inverter, shuts down the PWM signal to the transistors of the inverter to avoid damaging the converter
- A DIO interface card that receives the measurement signals and send an error signal to the optocard in case of over currents

To check all the connections inside each subsystem and between them, see *Appendix C. Lab setup diagrams*.

As mentioned before, the control system will be expanded to serve as an integrated charger described in [9]. So the secondary winding voltages and currents are measured by the transducers. Moreover, there is a relay for connecting the three-phase grid voltages to the secondary set of windings.

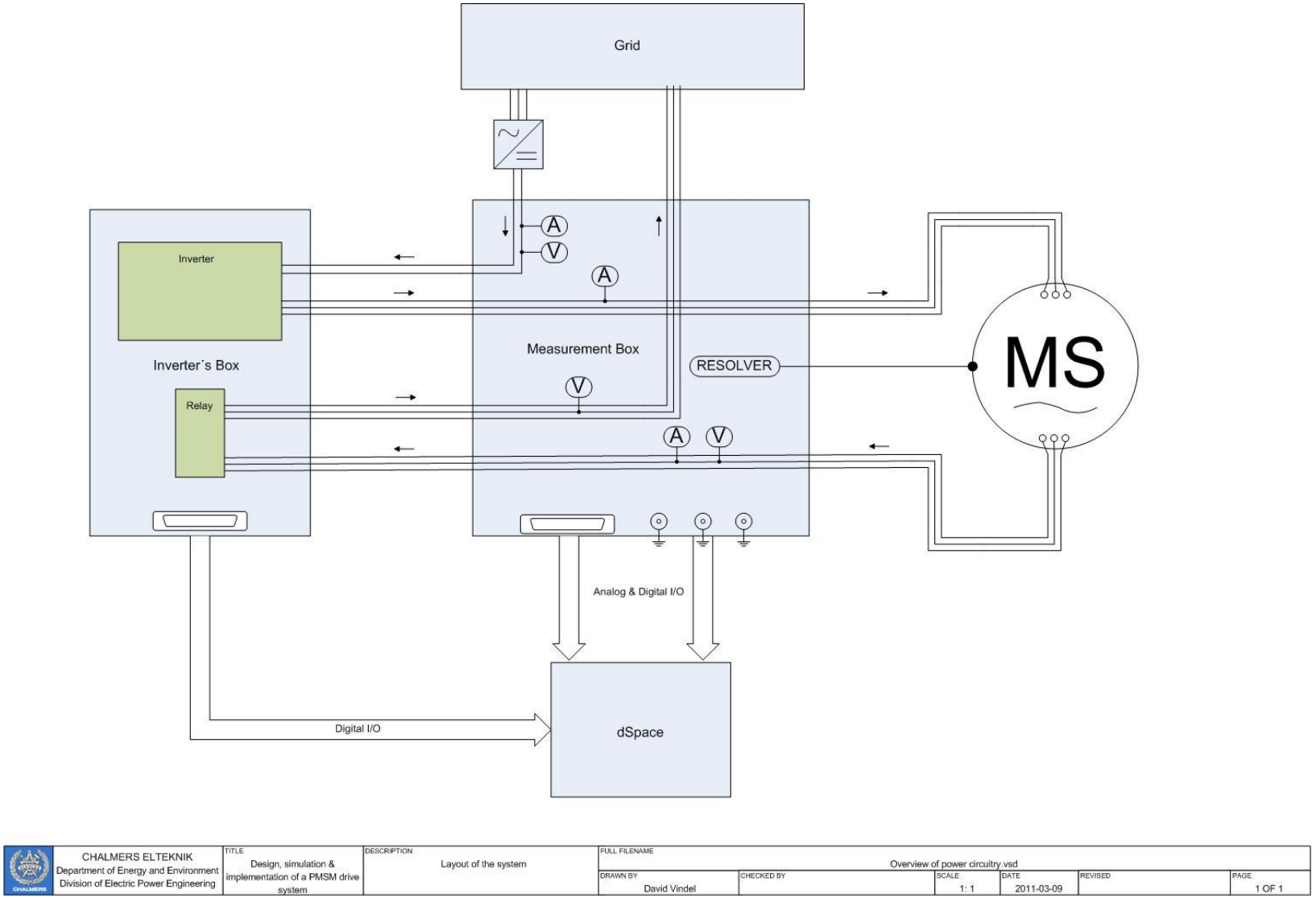


Figure 3.1: Simple schematic diagram of the drive system.

3.2 PMSM

The machine used in the practical setup is a surface mounted permanent magnet synchronous motor. The motor parameters used in the practical set up are listed in Table 3.1. The magnetic flux created by the permanent magnets has a fixed value. For PMSM, the inductances in direct and quadrature axes are the same values.

Table 3.1: PMSM parameters

Parameter	Value	Description
$\mathbf{P_n}$ **[W]**	2 000	Rated power
$\mathbf{U_n}$ **[V]**	420	Rated voltage
$\mathbf{I_{max}}$ **[A]**	1.5	Max. Current per winding
$\boldsymbol{\omega_n}$ **[rpm]**	1 000	Rated speed
$\boldsymbol{\omega_{max}}$ **[rpm]**	5 000	Max. Speed
$\mathbf{T_n}$ **[Nm]**	3	Rated torque
$\mathbf{T_{max}}$ **[Nm]**	5	Max. Torque
$\mathbf{R_s}$ **[Ω]**	7.1	Stator phase resistance
Ld [H]	$30 \cdot 10^{-3}$	Direc-axis inductance
Lq [H]	$30 \cdot 10^{-3}$	Quadrature-axis inductance
$\boldsymbol{\varphi_{pm}}$ **[T]**	0.2	Permanent magnet flux
p	3	Pole pairs
J [kgm^2]	$5.8 \cdot 10^{-4}$	Inertia
B [Nms]	0.002	Viscous coefficient

The most innovative feature of this PMSM is its double stator winding. That means, each phase winding has been divided in two equivalent parts. One part of the three phase windings (A, B and C) are called primary windings and the other (A', B' and C') are called secondary windings [9]. This division is one of the key points of the 'Isolated Integrated Charger' that is explained in [9]. Anyhow, this thesis only related with the speed control of the motor and these secondary windings are not used.

The primary side stator windings have wye connection.

3.3 Inverter

A 4-leg inverter is used in the lab setup where one leg is left without use. Table 3.2 summarizes the inverter specifications. Detailed information can be found in [10].

Table 3.2: Inverter characteristics.

Parameter	Value	Description
V_{DC} [V]	0-600	Input DC voltage
I_n [A_{rms}]	10	Rated rms current per phase
I_{max} [A]	15	Max. Current
P_{max} [W]	7 000	Max. Output power
f_{max} [Hz]	20 000	Max. Switching frequency

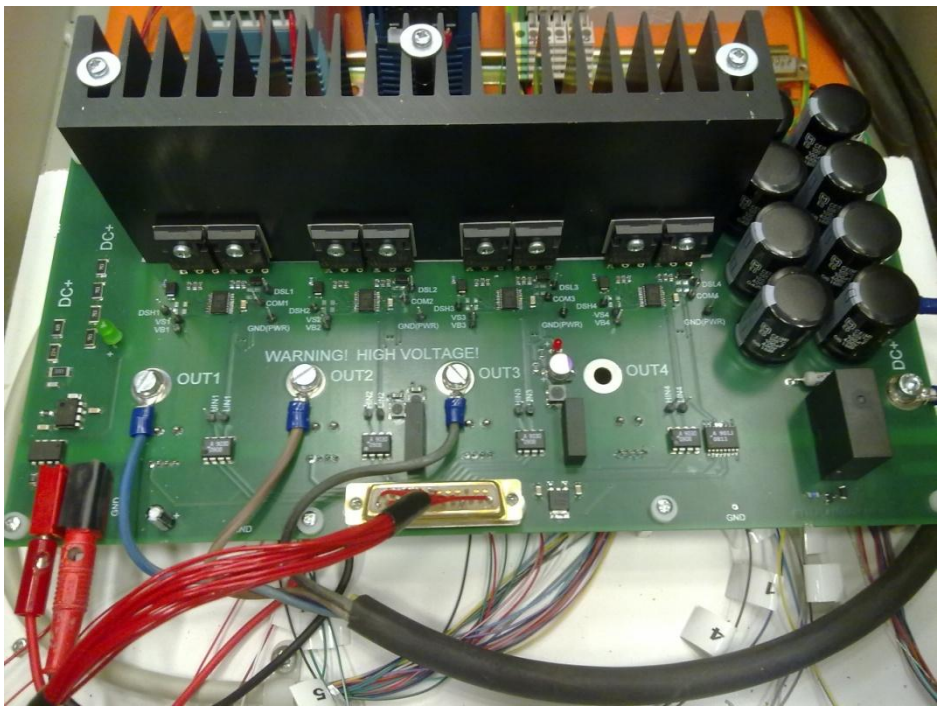


Figure 3.2: Inverter.

The control of the inverter's switching is carried out by PWM pulses generated by dSpace three-phase PWM block, with 12 kHz period. The duty cycle of each period is set by the controller and a conversion block. Both are explained below, in the dSpace software section. The connection between the inverter's control circuit and dSpace is done by a 25-pin D type connector that transmits six PWM signals, as well as two

more command signals (relay and fault clear) needed for the inverter's start up process.

To start up the inverter, the following steps should be taken:

- Connect all necessary cables (+15V, DC supply, control system and load)
- Turn on the control system
- Turn on the low voltage supply
- Turn on the high voltage supply
- Start the control system by:
  1. Turn on the relay when the DC voltage has reached the desired level (~1s)
  2. Set FLT_CLR high
  3. Start switching
  4. Set FLT_CLR low

Once these steps are done, the inverter is ready for normal use [10].

3.4 Measurement interfaces

The controller of the motor's speed requires certain measurements of different variables as voltages, currents, angle or speed. All this data is obtained by means of the measurement equipment listed at the beginning of this chapter. In the Figure 3.3 it is shown where all those measurements are taken.

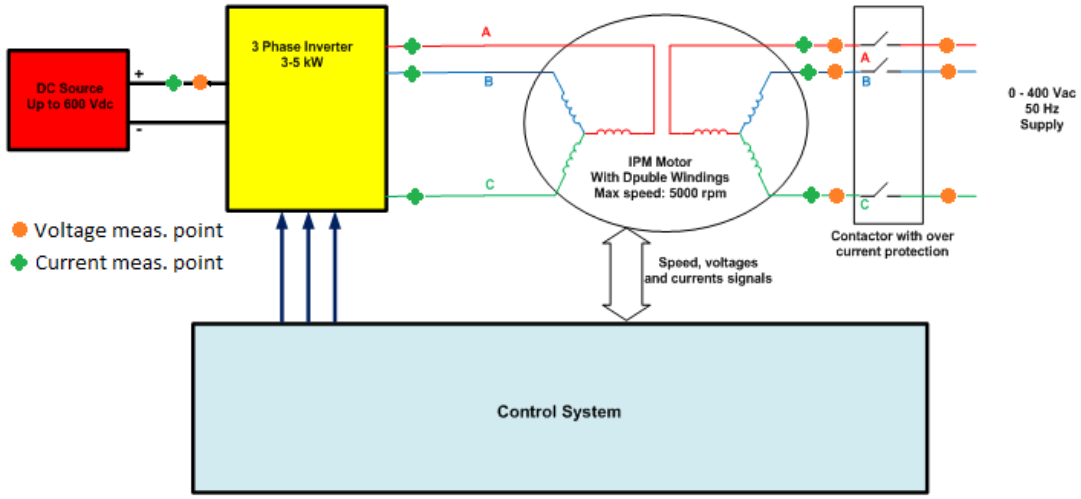


Figure 3.3: Schematic of the voltages & currents measurement points.

As it has been seen in chapter 2 (Figure 2.5), for the speed control of the PMSM is only needed to know the *abc* currents supplied to the motor and the speed and position of the rotor. In this sketch there are other current and voltage measurements that are not needed for the purpose of this thesis, but are useful in future works with this setup (integrated charger for a plug-in hybrid vehicle). That is the reason why these extras have been already installed.

Now, a deeper and detailed overview of the measurement hardware used will be presented.

3.4.1 Voltage measurements

For the voltage measurements, three voltage transducers UMAT2 have been used. Each transducer has three different channels, as can be seen in Figure 3.4, with a common neutral point for three phase voltage measures. As far as it is only needed 7 channels, two of the transducers are used for two different three phase voltage measurements and the third transducer has only one channel in use, for measuring the DC voltage input of the inverter.

The transducer cards work as follows: first, the input voltage goes through a resistor ladder that reduces the voltage level. After, the reduced signal goes to the AD210 electronic device, an isolated amplifier.

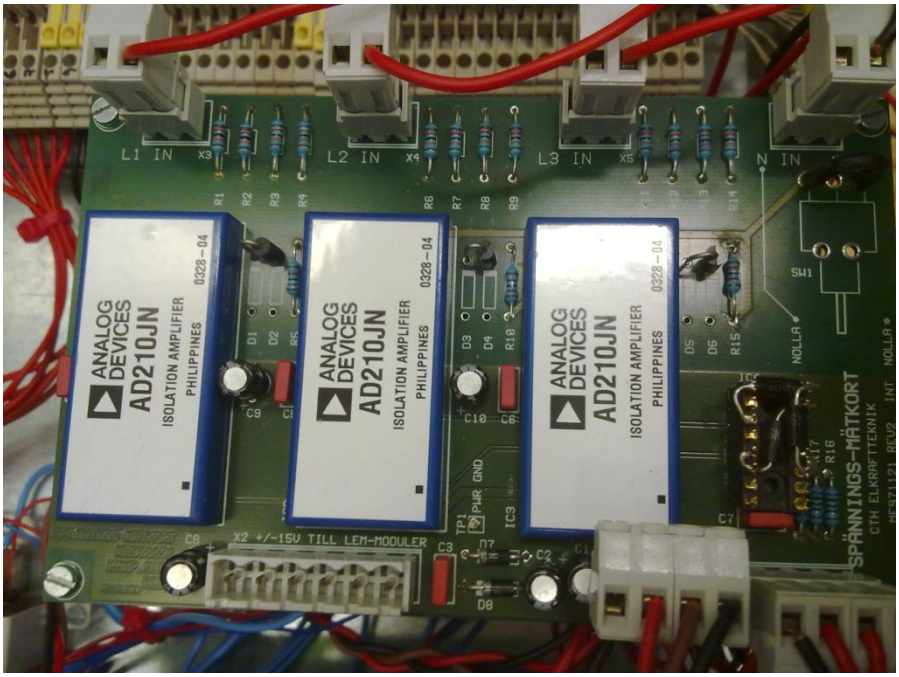


Figure 3.4: Voltage transducer UMAT2.

Resistors ladder design

The resistor ladder had to be designed and soldered before the testing and mounting of the transducer. Figure 3.5 shows the used resistors ladder network. For this purpose and considering that the voltage range to be measured is $\pm 400V$ and the output signals of the transducers should be in the range $\pm 10V$, the following procedure has been performed:

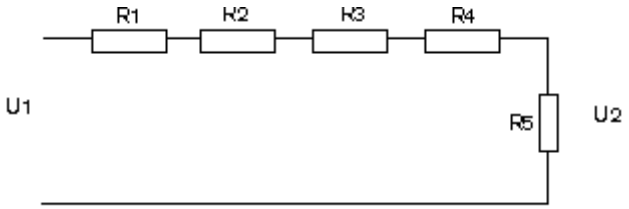


Figure 3.5: Sketch of the resistor ladder of the UMAT2 transducer.

where the initial conditions are:

$$U_1 = \pm 400V$$
$$U_2 = \pm 10V$$
$$R_1 = R_2 = R_3 = R_4 \quad (3.1).$$

And the relation between both voltages corresponds to a voltage divider:

$$\frac{U_2}{U_1} = \frac{10}{400} = 0.0025 = \frac{R5}{\sum R_i} \quad (3.2).$$

According to (3.2), the resistors values chosen are:

$$R_1 = R_2 = R_3 = R_4 = 120k\Omega$$
$$R_5 = 12k\Omega$$

This gives the proportion between input and output voltage:

$$U_2 = \frac{R5}{\sum R_i} U_1 = \frac{12}{480+12} U_1 = 0{,}02439 U_1 \quad (3.3).$$

Testing of the voltage transducers

Each channel of each voltage transducer has been tested before the final mounting. For that purpose, 15 voltage measurements within the range 10-420 V_{DC} have been performed, connecting the transducer to a high voltage source. The goal of these tests is to check the linear relation between the input and output voltages and also, that the slope of this relation adjust to the theoretical slope obtained in equation (3.3).

In Figure 3.6 are presented the results of the tests for each voltage transducer. Note that the way the transducer cards are named correspond to their position in the measurement box.

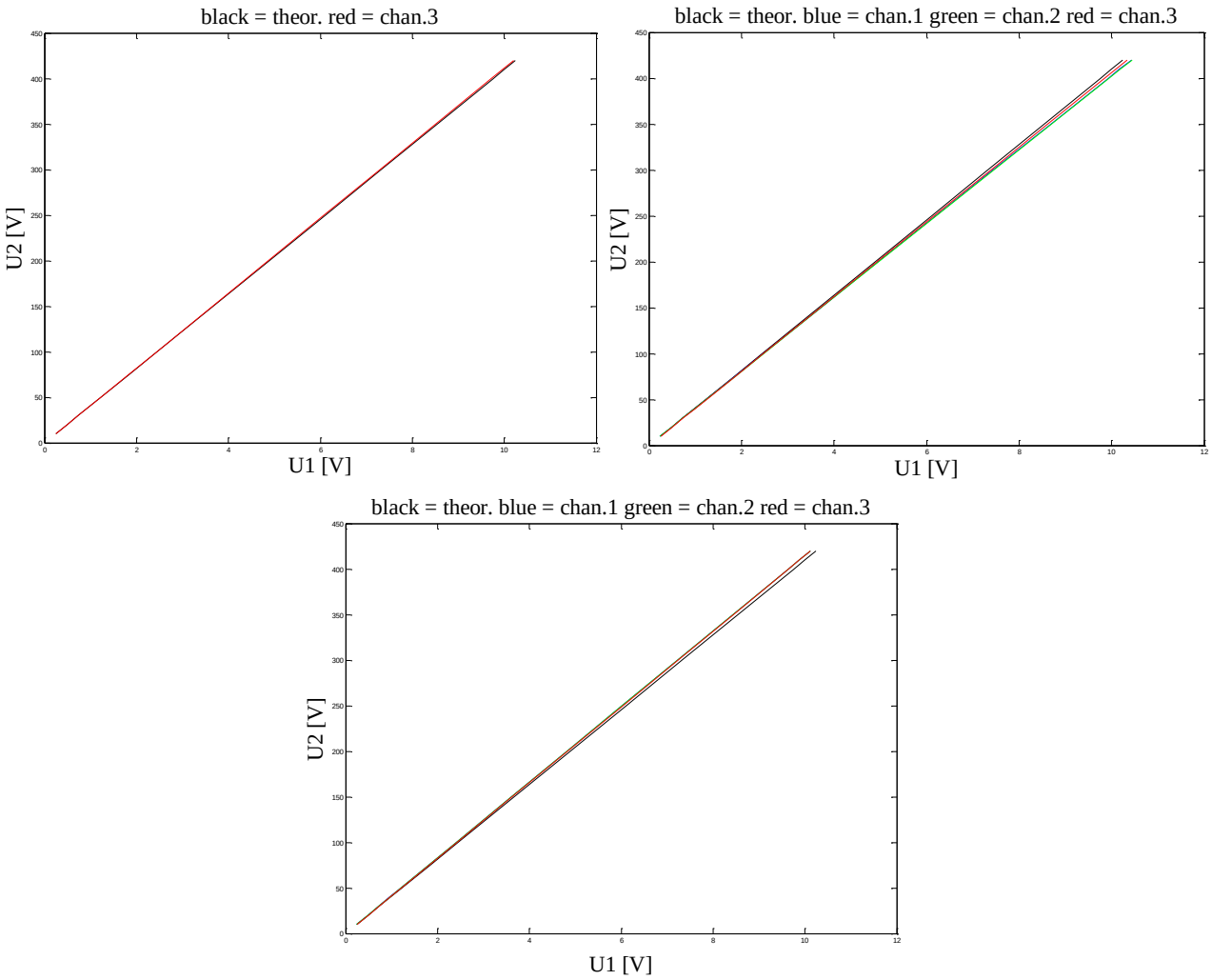


Figure 3.6: Voltage transducers test.

The voltage transducers have a good performance in terms of linearity and error. Now, the real slope of each channel is computed, in order to use that value in the future programming for the real time application that will control the lab tests. The errors computed correspond to a nominal voltage measure (400 V).

For the upper transducer the slopes of each channel are:

Channel 1, slope = 0,02411.	Error = 1,189%.
Channel 2, slope = 0,02411.	Error = 1,291%.
Channel 3, slope = 0,02408.	Error = 1,189%.

For the mid transducer the slopes of each channel are:

Channel 1, slope = 0,02485.	Error = 1,681%.
Channel 2, slope = 0,02488.	Error = 1,886%.
Channel 3, slope = 0,02459.	Error = 0,877%.

For the lower transducer the slope is:

Channel 3, slope = 0,02426. Error = 0,499%.

3.4.2 Current measurements

For measuring the currents, seven LEM LA 50-S/SP1 modules are used. This device, with galvanic isolation between the primary and the secondary circuit, outputs a secondary current (I_2) proportional to the current that is measured (I_1). This I_2 flows through a resistor (R_{meas}) producing a voltage drop (U_{meas}). This voltage is the signal that dSpace receives. In Figure 3.7 can be seen a sketch of the working principle of the LEM module. In Figure 3.8 a real picture of the modules is shown.

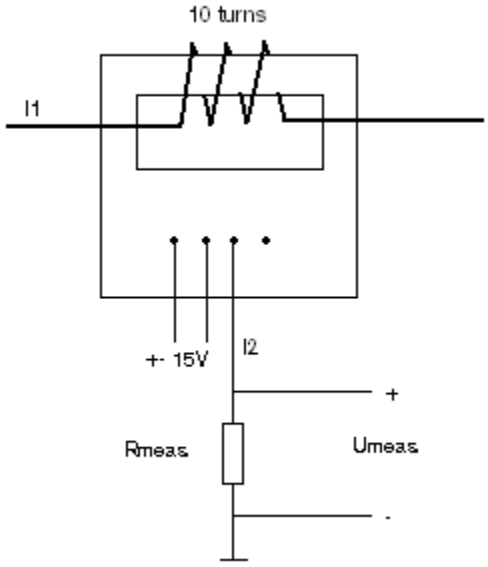


Figure 3.7: Current measurement using LEM module.

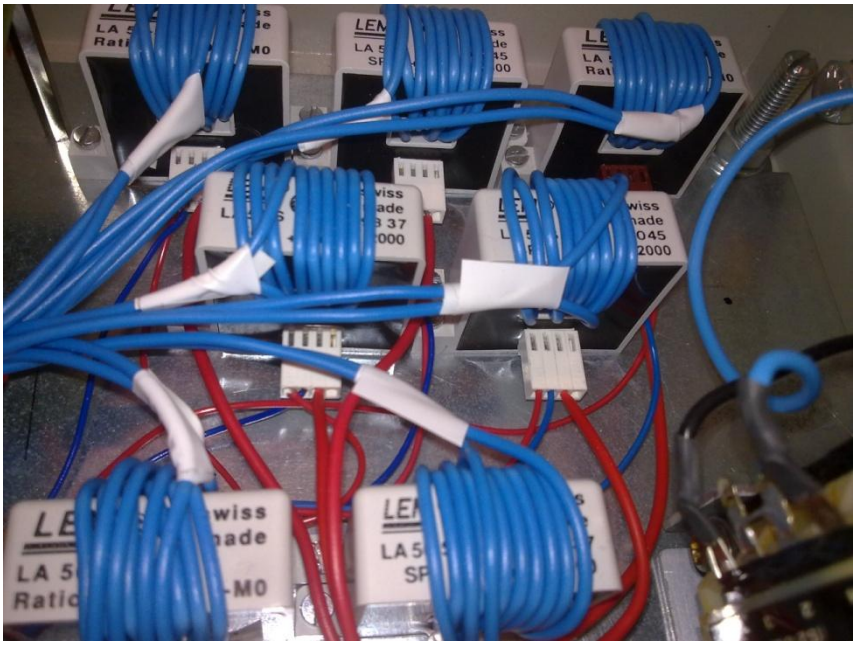


Figure 3.8: Current probes. LEM LA 50-S/SP1.

Parameters design

The voltage signal U_{meas} should be between $\pm 10V$. It is needed to choose an appropriate number of turns of the primary circuit as well as a value for R_{meas} (between 0-300Ω, according to the data sheet), so the relation between the output voltage and the input current is determined. To begin with, the relation between the input and output currents, according to the data sheet of the LEM module is:

$$I_1 = \frac{2000}{N} I_2 \tag{3.4}$$

Where N is the number of turns. For nominal currents below 50 A, a better accuracy is obtained by having several primary turns. So N = 10 turns is selected. Now, the relation between the secondary current and the output voltage has to be used to compute R_{meas}:

$$U_{meas} = I_2 R_{meas} \tag{3.5}$$

Combining equations (3.4) and (3.5) it is obtained:

$$I_1 = \frac{2000}{N} \frac{U_{meas}}{R_{meas}} = 200 \frac{U_{meas}}{R_{meas}} \tag{3.6}$$

If we choose a R_{meas} = 200 Ω, the linear relation between I_1 and U_{meas} is unitary.

Testing of the current modules

Each current module has been tested with 26 different current values between 0-6 A. The results of these tests showed that a good linear relation exists between the input current and the output voltage and that the experimental slope of this relation is almost the expected value (less than 1% error in the worst case). Anyway, the experimental slopes, shown in Table 3.3, are the value used in the lab tests.

Table 3.3: Experimental slopes of the LEM modules.

LEM module	1	2	3	4	5	6	7
Experimental slope [V/A]	1,0040	0,9966	0,9773	1,0060	0,9833	1,0026	0,9906

3.4.3 Position and speed measurements

Both, rotor position and speed are measured with a resolver-to-digital converter. This converter, pictured in Figure 3.9: Resolver-to-digital PBC., generates and sends a

sinusoidal reference waveform to a coil mounted in the rotor, and measure induced voltages in the two coils mounted on the stator. These two measured signals are processed by the resolver-to-digital converter, which is AD2S83 in this case, and the angle is extracted in a digital word. The number of digital bits for the angle measurement is programmable by the device.

In the board of the converter there is an option for choosing the resolution. In our case the appropriate resolution is 12 bit, which is the highest one that permits measuring up to 5000 rpm. Some other trimming had to be done to tune the reference wave generation or remove the offset in the output. Finally, some external components have to be mounted in the printed circuit board. The selection is shown in Table 3.4.

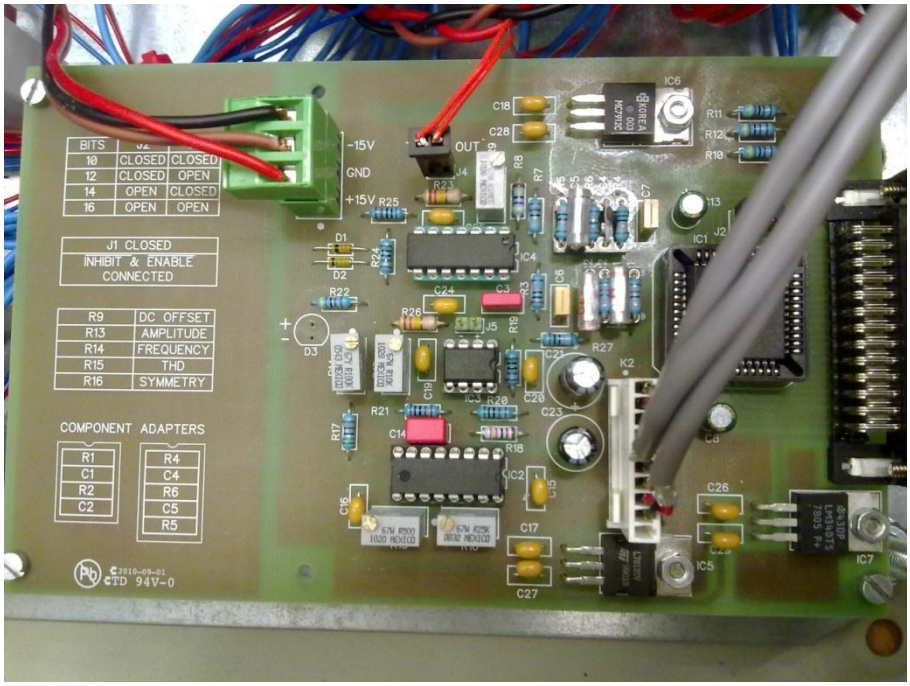


Figure 3.9: Resolver-to-digital PBC.

Table 3.4: External component selection for the resolver-to-digital PBC.

		Components selection		Value	
Components		**Typ. Values**	**Comments**	**For 12-bit**	**Units**
HF Filter	R_1	15 - 56 kΩ	May be omitted. Then, R_2=R_3	2,400E+04	Ω
	R_2	15 - 56 kΩ	Same value than R_1	2,400E+04	Ω
	C_1	$1/(2\pi R_1 f_{ref})$	Same value than C_2	6,631E-10	F
	C_2	$1/(2\pi R_1 f_{ref})$	May be omitted. Then, C_1=C_3	6,631E-10	F
Gain scaling	R_4*	$E_{dc}/(300e\text{-}9)$	If R_1 & C_2 are used	1,333E+05	Ω
		$E_{dc}/(100e\text{-}9)$	If R_1 & C_2 aren't used	4,000E+05	Ω
AC coup of ref. input	R_3	100 kΩ		1,000E+05	Ω
	C_3	$> 1/(R_3 f_{ref})$	R_3 in ohms	1,000E-09	F
Max	R_6**	$T = VCO_{rate}/(2^N)$	N=resolution, VCO_{rate}=trackin	83,333	rps

track rate			rate(rps)		
		R_6=6,81e10/(Tn)	n=bits per revolution, min R_6=62kΩ	1,995E+05	Ω
Close-loop BW select	C_4	$21/(R_6 f_{bw}^2)$	Choose f_{bw} according to resolution	1,684E-11	F
	C_5	$5C_4$		8,421E-11	F
	R_5	$4/(2\pi f_{bw} C_5)$		3,024E+06	Ω

Where:

$$f_{ref} = 10\,000Hz$$

$$VCO_{rate} = 5\,000rpm = 83.33rps$$

$$f_{bw} = 2\,500Hz$$

* $E_{dc} = 0.04$ for 12 bit resolution

** $n = 4095$ bits per revolution

Note: according to the data sheet, f_{bw} should be 4 times lower than f_{ref} for a 12 bit resolution.

With these component's values, the output from the speed meter is presented in Table 3.5.

Table 3.5: Output voltage for different rotor speeds.

Speed		Current	V_{out}
rpm	Hz	µA	**V**
100	1,667	0,803	**0,160**
250	4,167	2,008	**0,400**
500	8,333	4,016	**0,800**
750	12,500	6,024	**1,200**
1000	16,667	8,031	**1,600**
1500	25,000	12,047	**2,400**
2000	33,333	16,063	**3,200**
2500	41,667	20,078	**4,000**
3000	50,000	24,094	**4,800**
3500	58,333	28,110	**5,600**
4000	66,667	32,125	**6,400**
4500	75,000	36,141	**7,200**
5000	83,333	40,157	**8,000**

Testing and tuning of the resolver-to-digital transducer

The measuring of the rotor angle was tested and tuned (there was need to synchronize the 0 rad output with a magnet axis) running the machine as a generator and measuring the angle and voltages induced.

As it can be seen in Figure 3.10, the phase A voltage (red wave) peak is aligned with the 0 rad. angle. That means that we can suppose the voltage to follow a sinusoidal waveform. The Clark and Park transformations are used to transform three-phase voltages to the stationary and rotating reference frames *αβ* and *dq*. For the machine rotating at no-load, the voltage has just q component and d component is zero. The resolved angle output is compensated by an offset angle, after the conversion from mechanical to electrical angle.

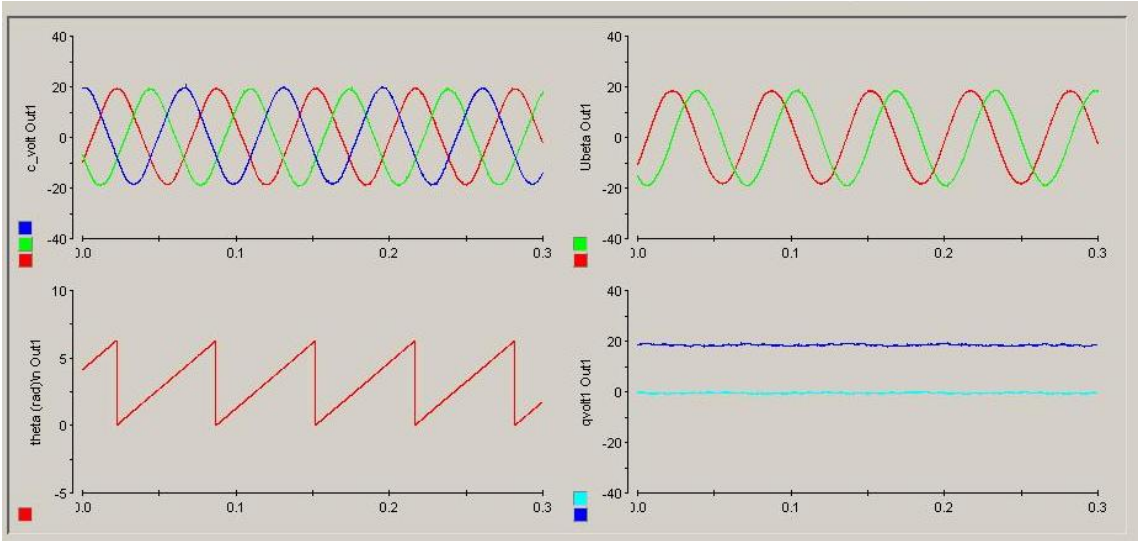


Figure 3.10: Rotor angle (left bottom), abc voltage (left top), αβ voltage (right top) and dq voltage (right bottom).

3.5 Connection to the grid by a relay

In future works, this lab setup will be used for charging purposes. In order to connect the secondary windings of the motor to the grid, secondary and grid voltage should be synchronized (amplitude and phase). Some control has to be done to achieve this goal, and once both voltages are synchronized, the relay closes the connection. This three-phase relay is activated by a TTL signal sent by dSpace, but this signal is 5 V and the relay control system needs 24 V to close the contacts.

In order to solve this voltage difference, an electronic circuit has been designed. This circuit receives the TTL signal and a 24 V signal. The TTL signal activates the transistor allowing the 24 V signal reach the relay control circuit. A scheme of the circuit can be seen in Figure 3.11 and Figure 3.12 shows the implementation.

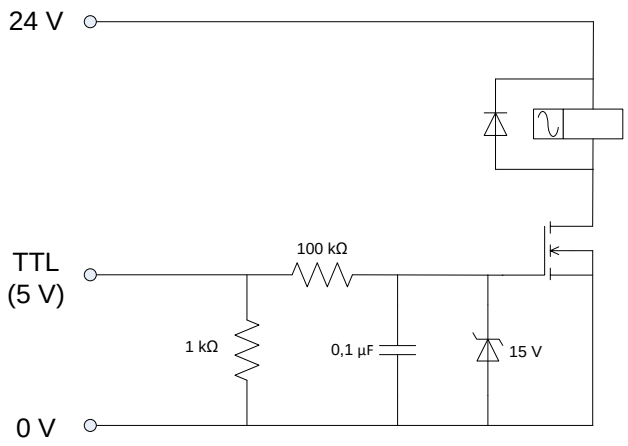


Figure 3.11: Scheme of the relay activation circuit.

Figure 3.12: Three-phase relay (left) and relay activation circuit (right).

3.6 dSpace system

The dSpace system is a tool used to build real-time control systems. It is used to connect different kind of signals (analogue or digital) that measurement devices obtain to a computer, as well as send signals from the computer to the devices in order to control them.

The dSpace system is the interface between the physical world (motor, inverter, measure sensors...) and the computer, from where the lab tests is controlled and the results are plotted. The dSpace system model used in this setup is CP1103 system, with different analogue I/O and digital I/O.

The controller has to be programmed and then, by means of the analogue and digital I/O, some command signals are sent to the system and the measured values are received.

Software part

The dSpace programming has been carried out using Simulink. Most of the model is equal to the one used in chapter 2 for the simulations. Only few parts have been changed, added or removed. These modifications are shown in *Appendix E. dSPace software implementation*.

Special attention should be placed in the *Simulation > Configuration Parameters*. The next modifications should be done before running a real time application:

- The stop time is set to "inf".
- The solver type should be "Fixed-step".
- The solver is "ode1 (Euler)".
- The block reduction option in the optimization menu should be unmarked.

Without these modifications, the program would return an error message when trying to compile.

The modifications carried out to the original Simulink program (the one used for the simulations in chapter 2) are as following:

- Some ADC block are added for receiving the voltage, current and speed measurements. Apart from the linear conversion mentioned in the measurement equipment description, a gain of 190 has to be added because dSpace reduces in 10 times the input value (a $\pm 10V$ input correspond to $\pm 1V$ in Simulink).
- The inverter's model is removed. Instead there is the real inverter. Some blocks are added to initialize the inverter.
- The motor model is removed. Instead there is the real PMSM.
- The PWM block is changed for the PWM three-phase generation that includes the RTI library in Simulink. Now the voltage command get to a conversion block, where it is obtained the duty cycle of each phase of thee PWM, and these signal are the input to the PWM block.
- A new block dedicated to the resolver has to be added. The resolver is driven by the inhibit signal. This is a square signal that indicates when the data in the resolver transducer has to be updated and when has to be sent to dSpace. When inhibit is low data is sent and when is high, data is being updated. This inhibit signal (12 kHz square) is also used to trigger the interrupt that drives the controller block.
- The controller, as well as the Clark and Park transformations remains the same.

The system has been organized in two main blocks: measurements and controller. The measurement block is triggered with the PWM interrupt block. The purpose of that is to synchronize all the measurements with the peak of the carrier wave (triangular wave) of the PWM. All the measurements are captured at the same time (with a sampling time of 12 kHz). Then, the controller block is triggered with an interrupt generated within the measurement block, so when the data capture is finished all the operations required for the control will begin.

All the changes performed to the original Simulink blocks of chapter 2 can be seen in *Appendix E. dSpace software implementation*.

The other software tool used is ControlDesk. With ControlDesk is possible to create instrument panels whit control, display and plotting possibilities. By connecting the Simulink variables to plotters, slide bars, displays, leds...etc the user can modify constants or command values, or check the current, speed or torque waveforms. Figure 3.13 shows the instrumentation panel used for this experiment.

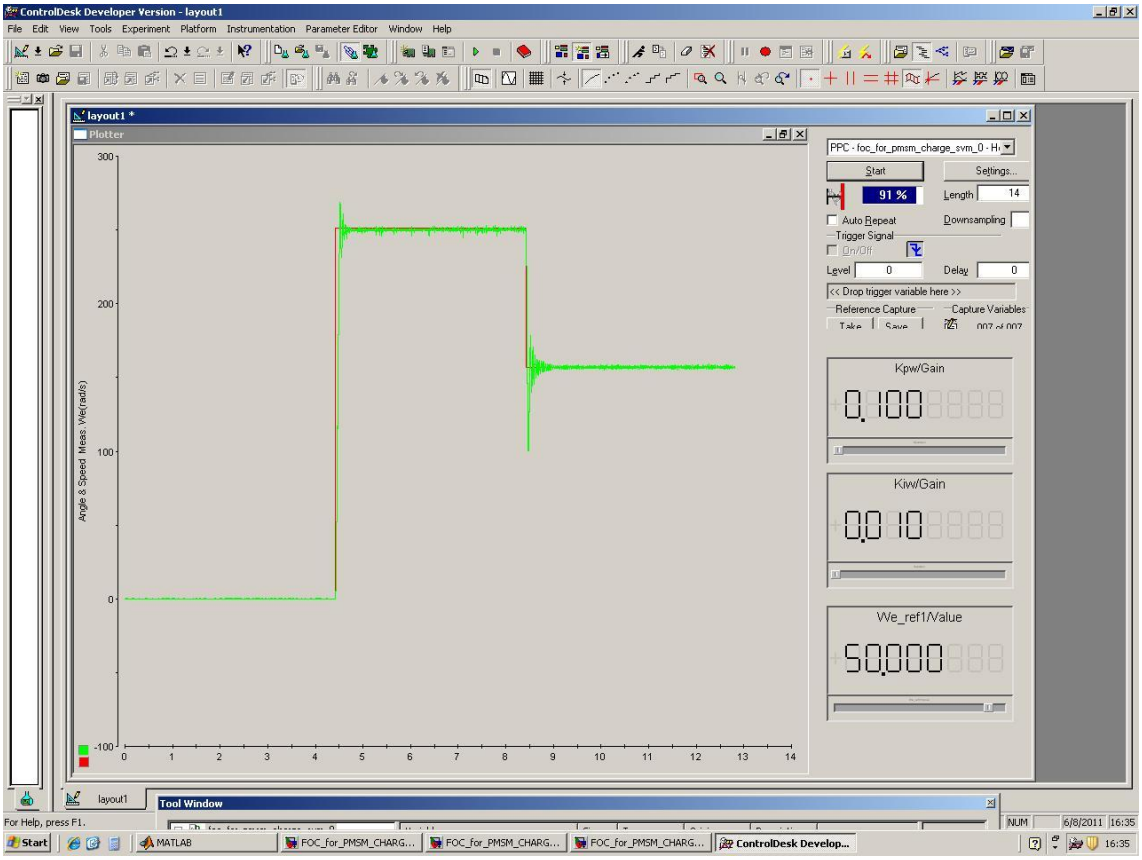


Figure 3.13: Layout of the dSpace instrumentation panel.

Hardware part

The dSpace boards CP1103 and CPL1103, shown in Figure 3.14, are connected to the host PC. Then, these boards provide some inputs and outputs to be connected to the external devices. In this project 6 analogue inputs (ADC) are being used, as well as the master and slave digital I/O. The connections are the following (and can be seen also in *Appendix C. Lab setup diagrams*):

- One analogue input for the speed
- Two analogue inputs for the DC current and voltage (input of the inverter)
- Three analogue inputs for the three phase currents which feed the PMSM
- The master digital I/O for controlling the resolver-to-digital board, and read the 12-angle bits
- The slave digital I/O for the PWM pulses, the inverter's initialization commands and the grid contactor operation

The hardware system is already prepared to use another 9 analogue inputs that measure the three phase secondary currents and voltages as well as the grid voltage, when the charging tests are performed.

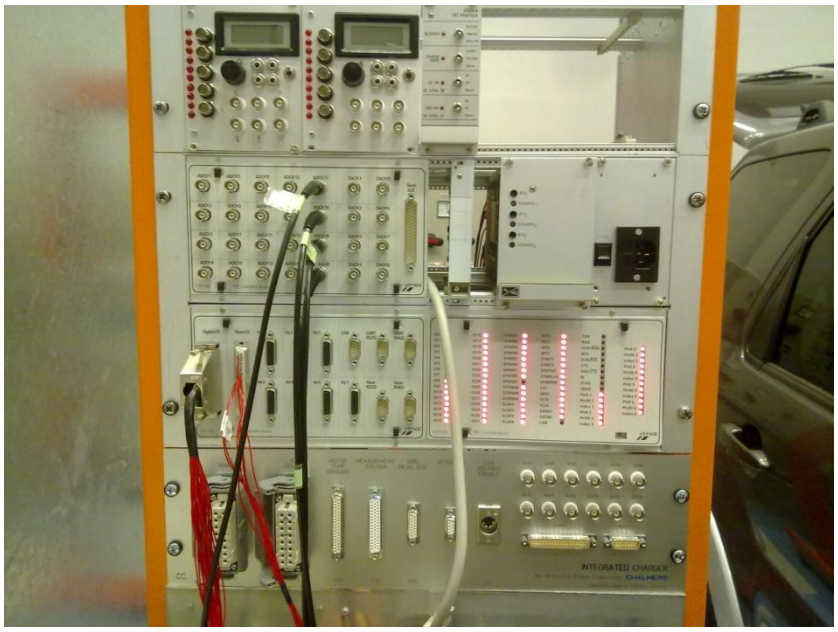


Figure 3.14: dSpace connections boards CP1103 and CPL1103.

3.7 Experimental results

Now, the results of the experimental test are presented.

Figure 3.15 and Figure 3.16 shows the speed response of the system due to a step change in the speed command. The zoomed stator currents for each speed step are shown in Figure 3.17 and Figure 3.18, respectively.

As it is shown in these figures, the system has a good dynamic response.

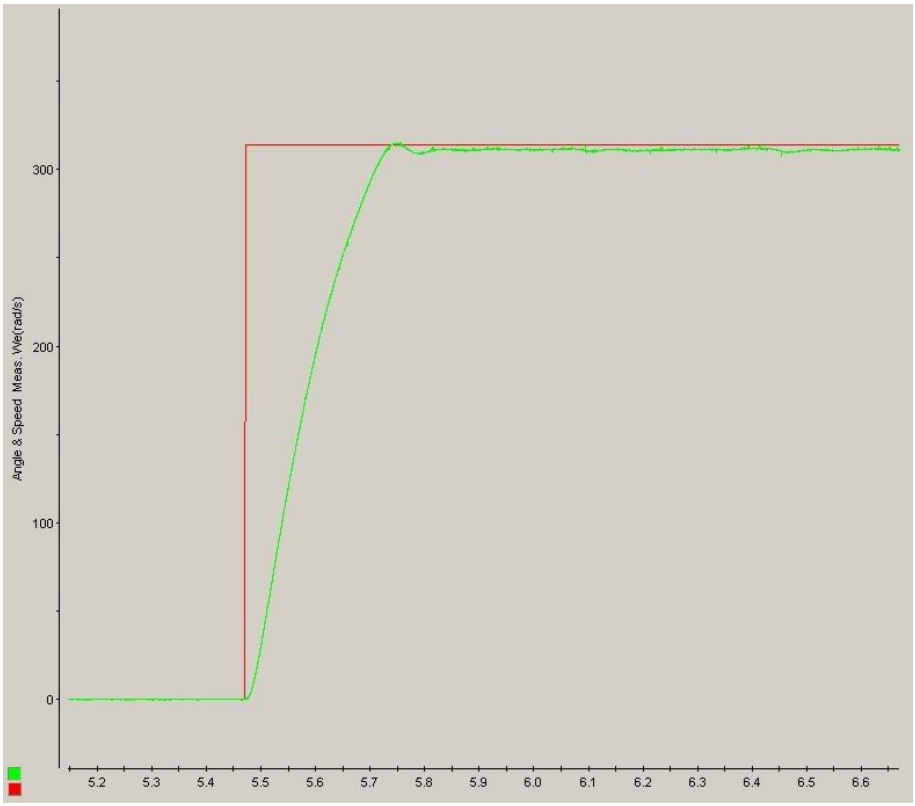


Figure 3.15: Electrical speed. 1st step.

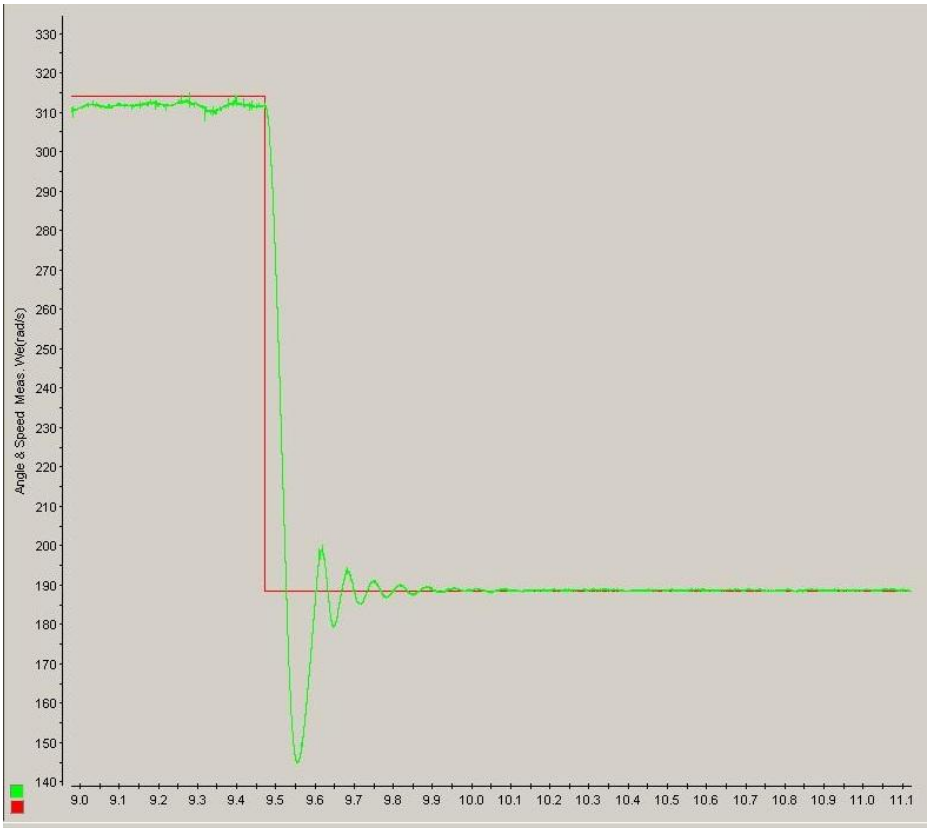


Figure 3.16: Electrical speed. 2nd step.

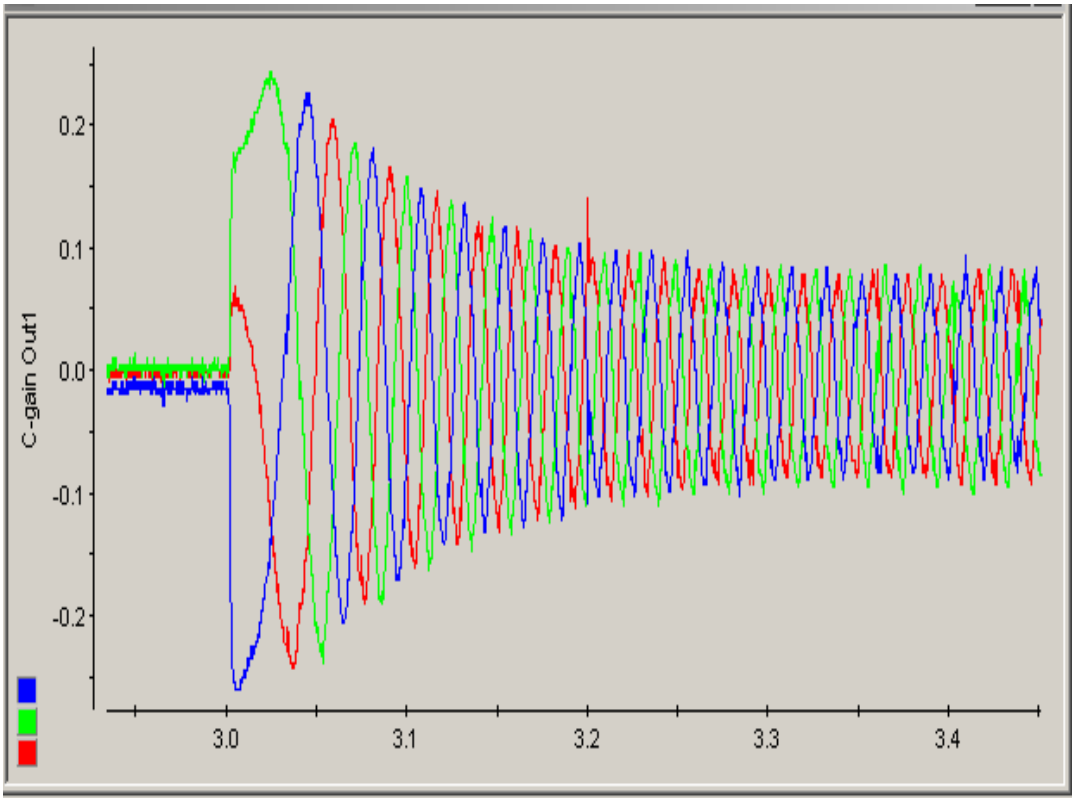


Figure 3.17: Stator currents in abc domain due to the first speed step.

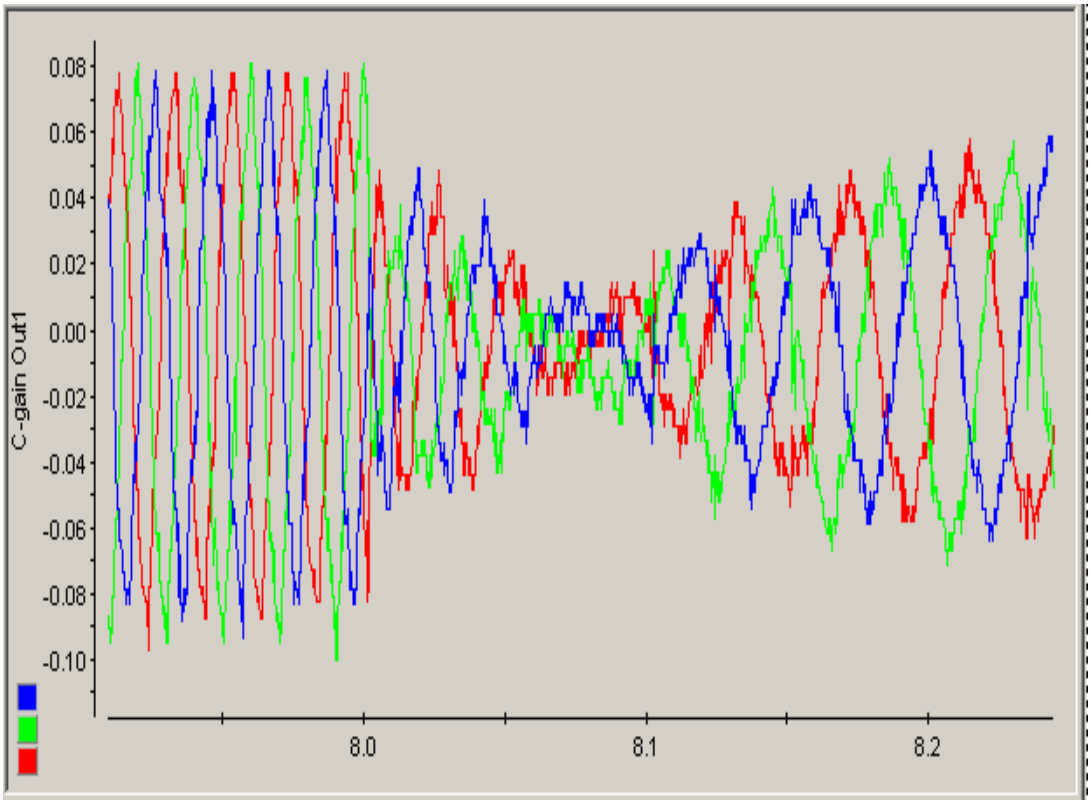


Figure 3.18: Stator currents in abc domain due to the second speed step.

4 Conclusions and future work

4.1 Conclusions

Field-oriented control of a permanent magnet synchronous motor is designed, simulated and implemented in this thesis.

Firstly, the whole drive system is simulated by the use of Matlab/Simulink. With the motor equations, a model for the machine has been developed in Simulink, as well as models for the PWM signal generator, inverter, controller and Clark and Park transformations. The results of the simulation show the good response of the model when tracking a command speed.

Afterwards a lab setup was implemented using a 2 kW PMSM and dSpace as the computer-system interface. After the calibration of every measuring device and the proper corrections of the controller model, some lab tests were carried up to check the validity of the simulation results. The results show that the system has a good dynamic response.

4.2 Future work

The current hardware will be extended to implement an isolated integrated charger as explained in [9].

The classical PWM method is used to generate the requested motor voltages. To improve the system performance in terms of torque ripple, power quality and better DC voltage utilization, space vector modulation can be employed.

The speed is estimated by the measurement of the position. The speed estimation can be improved by the use of Kalman filters.

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Appendices

Appendix A. Reference frame conversion

First of all, it should be defined a three phase magnitude (can be either voltage or current) as follows:

$$\begin{aligned} x_a &= X_m \cos(\omega t) \\ x_b &= X_m \cos\left(\omega t - \tfrac{2\pi}{3}\right) \\ x_c &= X_m \cos\left(\omega t + \tfrac{2\pi}{3}\right) \end{aligned} \quad \text{(A.1)}$$

Now, this three phase system can be written with only two components, real and imaginary. This format is called space vector:

$$x(t) = x_\alpha + j x_\beta = \tfrac{2}{3} K \left(x_a(t) + x_b(t) e^{-j\frac{2\pi}{3}} + x_c(t) e^{j\frac{2\pi}{3}} \right) \quad \text{(A.2)}$$

The *K* factor is a scaling constant, and depending on the value that takes, the transformation will have certain characteristics. The transformation is given by the following matrix:

$$T_{abc \to \alpha\beta} = K \begin{bmatrix} 2/3 & -1/3 & -1/3 \\ 0 & 1/\sqrt{3} & -1/\sqrt{3} \end{bmatrix} \quad \text{(A.3)}$$

And the inverse transformation is given by the matrix:

$$T_{\alpha\beta \to abc} = \tfrac{1}{K} \begin{bmatrix} 1 & 0 \\ -1/2 & \sqrt{3}/2 \\ -1/2 & -\sqrt{3}/2 \end{bmatrix} \quad \text{(A.4)}$$

The typical values for the *K* constant are:

Table A.1: K constant choices

Amplitude invariant	$\boldsymbol{K = 1}$
RMS-value invariant	$K = {}^{1}/_{\sqrt{2}}$
Power invariant	$K = {}^{\sqrt{3}}/_{\sqrt{2}}$

To convert from the three phase or the stationary two-axis reference frames to the rotating two-axis reference frame (dq axis) is applied to the previous space vector $x(t) = x_\alpha + jx_\beta$ the next transformation:

$$x_{dq} = x(t)e^{-j\theta} \tag{A.5}$$

Where $\theta = \omega t$, the electrical angle. This transformation "makes" the previous stationary axis to spin with ω frequency and so, the previous varying values of flux, voltages or currents are converted into constant values. The transformation matrices are the following:

$$T_{abc\to dq} = \begin{bmatrix} cos(\theta_r) & cos\left(\theta_r - \frac{2\pi}{3}\right) & cos\left(\theta_r + \frac{2\pi}{3}\right) \\ -sin(\theta_r) & -sin\left(\theta_r - \frac{2\pi}{3}\right) & -sin\left(\theta_r + \frac{2\pi}{3}\right) \end{bmatrix} \tag{A.6}$$

$$T_{\alpha\beta\to dq} = \begin{bmatrix} cos\theta_r & sin\theta_r \\ -sin\theta_r & cos\theta_r \end{bmatrix} \tag{A.7}$$

And the inverse transformation matrices are:

$$T_{dq\to abc} = \begin{bmatrix} cos(\theta_r) & -sin(\theta_r) \\ cos\left(\theta_r - \frac{2\pi}{3}\right) & -sin\left(\theta_r - \frac{2\pi}{3}\right) \\ cos\left(\theta_r + \frac{2\pi}{3}\right) & -sin\left(\theta_r + \frac{2\pi}{3}\right) \end{bmatrix} \tag{A.8}$$

$$T_{dq\to\alpha\beta} = \begin{bmatrix} cos\theta_r & -sin\theta_r \\ sin\theta_r & cos\theta_r \end{bmatrix} \tag{A.9}$$

Sources [2, 8]

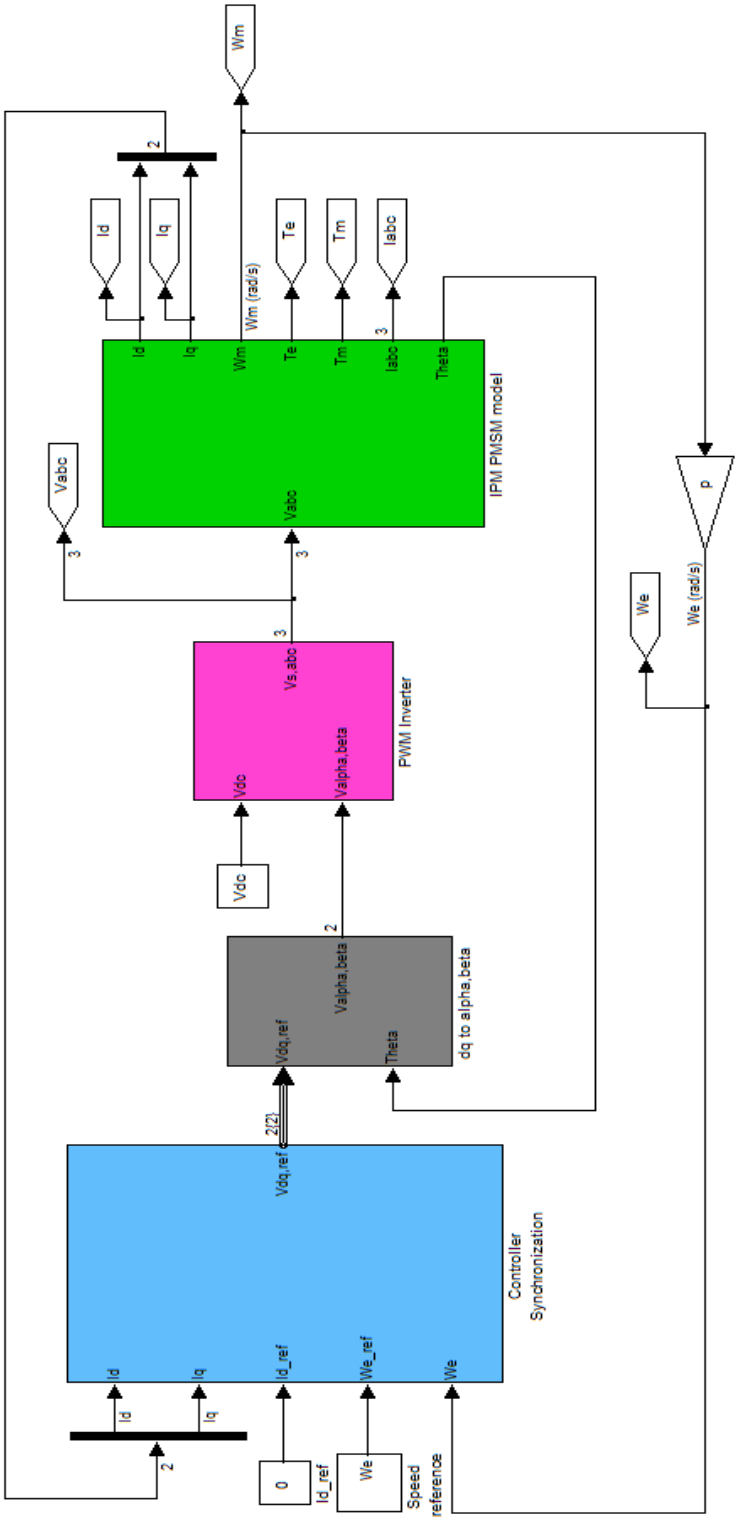
Appendix B. Matlab code and Simulink block diagrams

Matlab code of the file *Parameters.m*

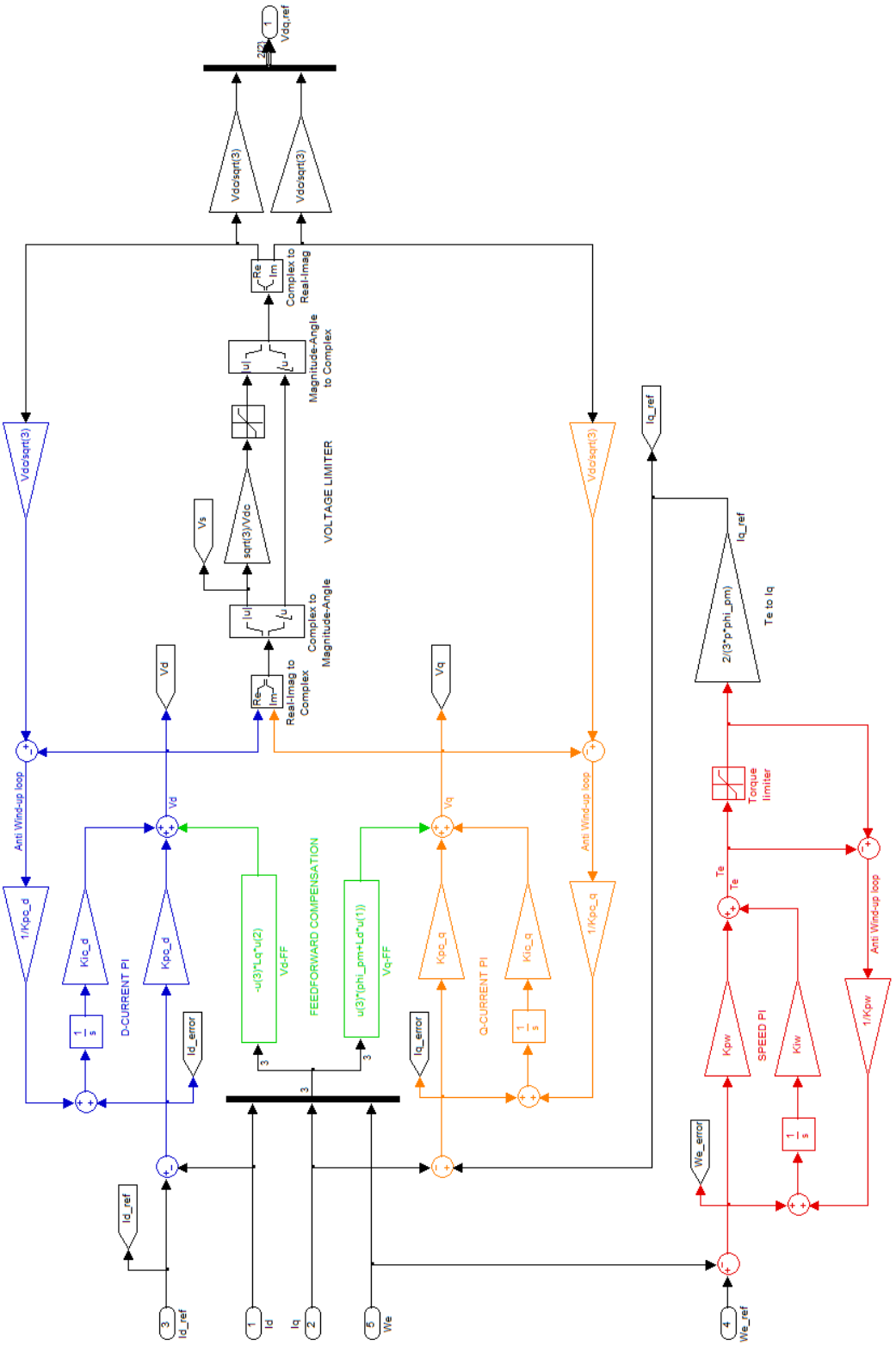
```
%//////////////////////////////////////////////////////////////////
%                      2 kW motor parameters
%
%            Master thesis student David Vindel Muñoz.
%             Electric Power Engineering Department
%                 Chalmers Tekniska Högskola
%
%                           March 2011
%//////////////////////////////////////////////////////////////////

clear all

% PMSM parameters
Rs = 7.1;                       %Stator resistance
Ld = 30e-3;                     %d-axis inductance
Lq = 30e-3;                     %q-axis inductance
phi_pm = 0.12;                  %Permanent magnet flux
p = 3;                          %Pole pairs
J = 5.8e-4;                     %Inertia
B = 0.002;                      %Viscous coefficient
Wbase = 1000*pi/30;             %Base speed
Wmax = 5000*pi/30;              %Max. speed
Prated = 2000;                  %Rated power
Trated = 3;                     %Rated torque

% Controller parameters
Vdc = 400;

% Current PI parameters
Fs = 10e3;                      %Inverter's Swithcing frequency 10[kHz]
alpha_i = 2*pi*Fs/10;           %Parameter used for Kp & Ki
Kpc_d = alpha_i*Ld;             %Prop.constant of d-axis current reg.
Kic_d = alpha_i*Rs;             %Int. constant of d-axis current reg.
Kpc_q = alpha_i*Lq;             %Prop. constant of q-axis current reg.
Kic_q = alpha_i*Rs;             %Int. constant of q-axis current reg.

% Speed PI parameters
alpha_w = alpha_i/10;           %Parameter used for Kp & Ki
Kpw = alpha_w*J;                %Prop. constant of speed reg.
Kiw = alpha_w*B;                %Int. constant of speed reg.
```

Simulink diagram blocks:

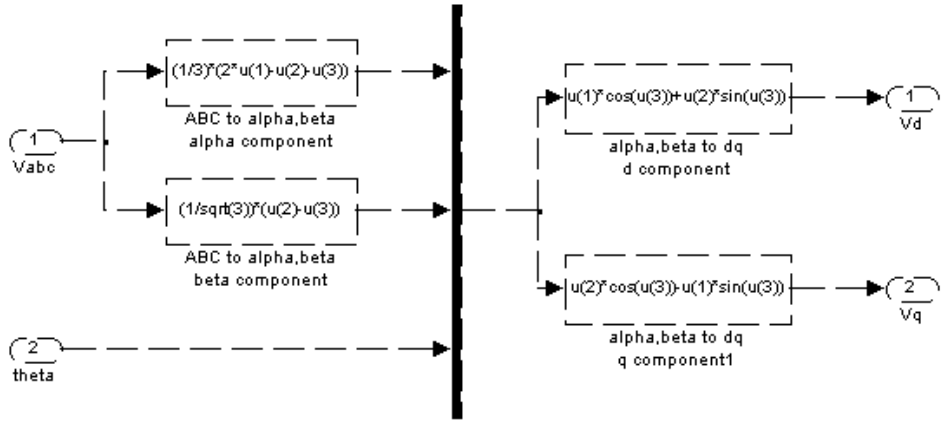
1. Main system



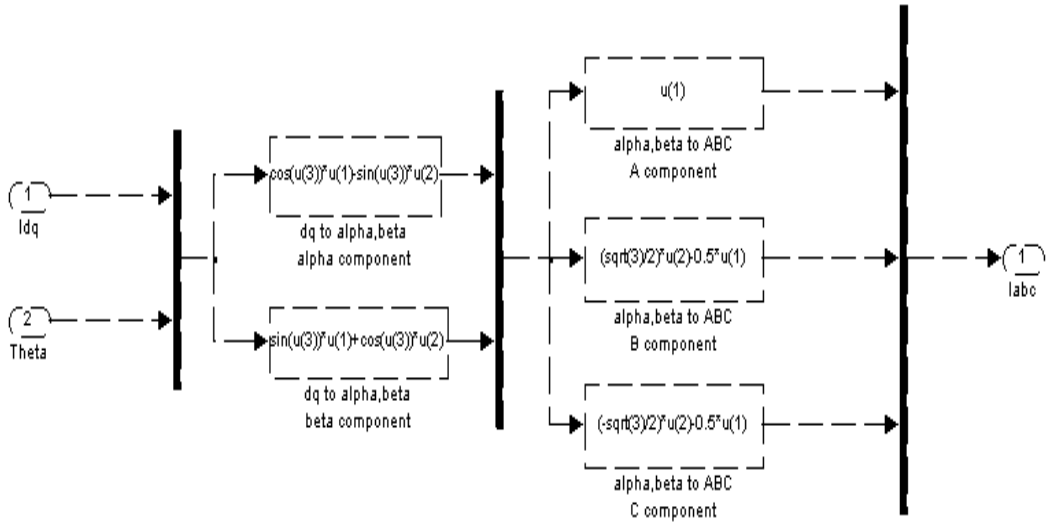
2. Speed controller



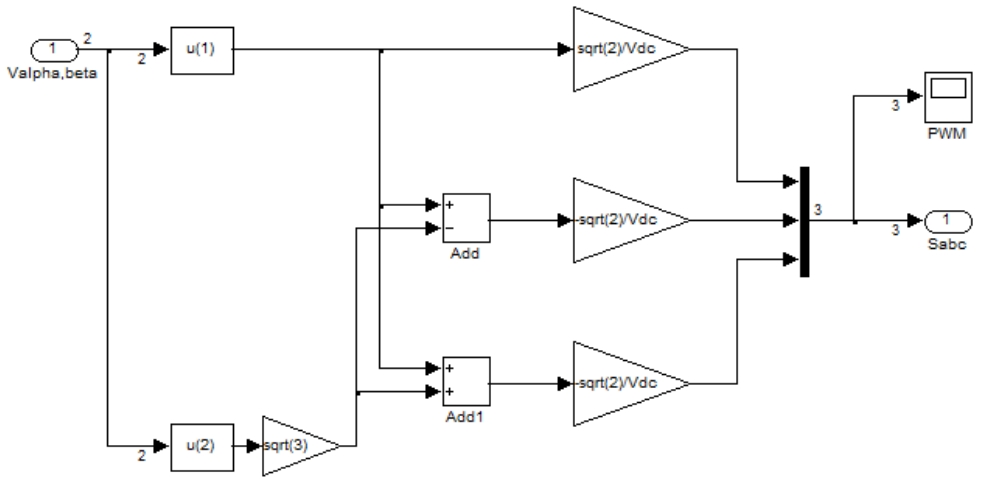
3. Clark & Park reference frame conversion (direct)



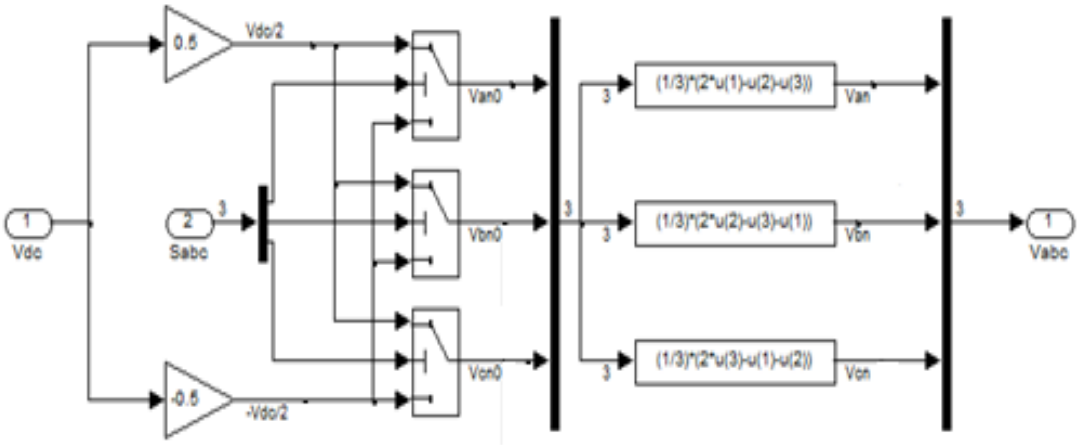
4. Clark & Park reference frame conversion (inverse)



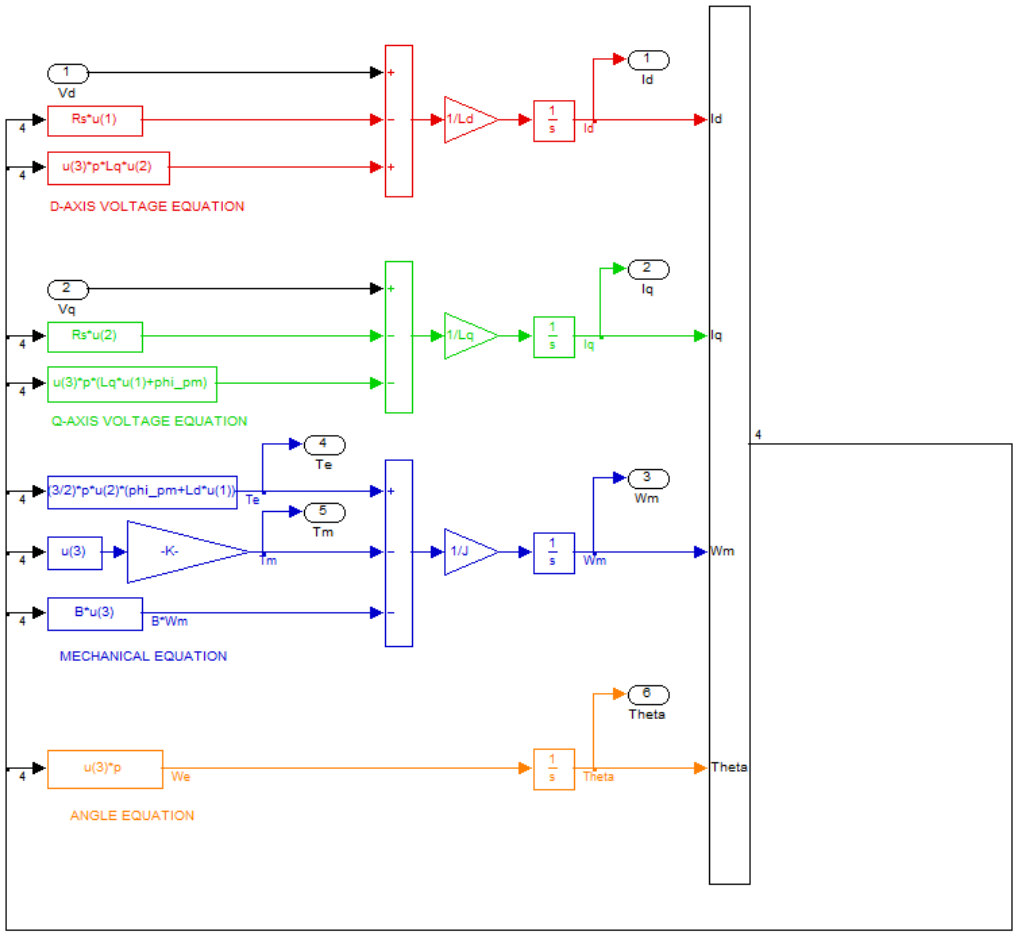
5. PWM generation



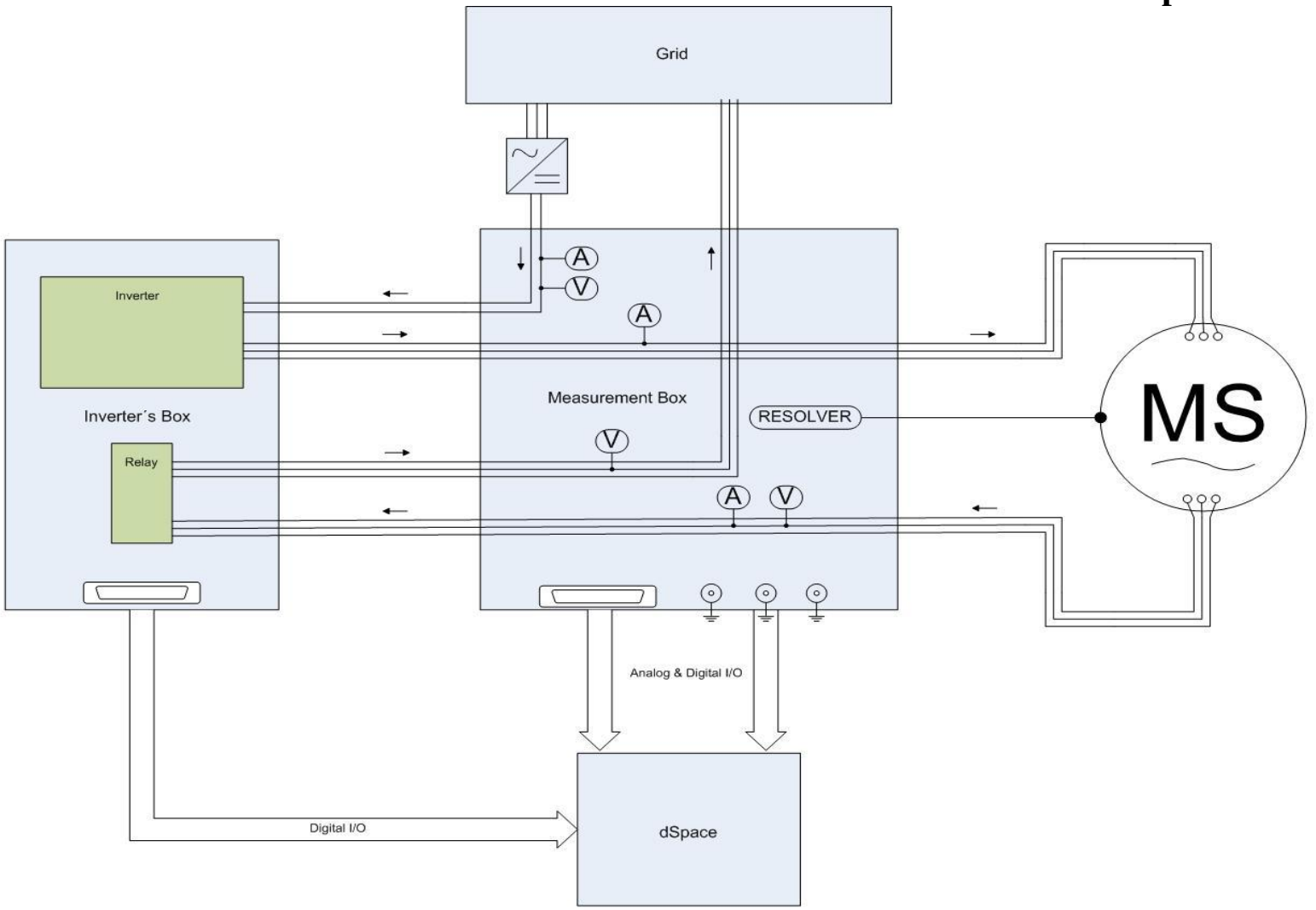
6. Inverter



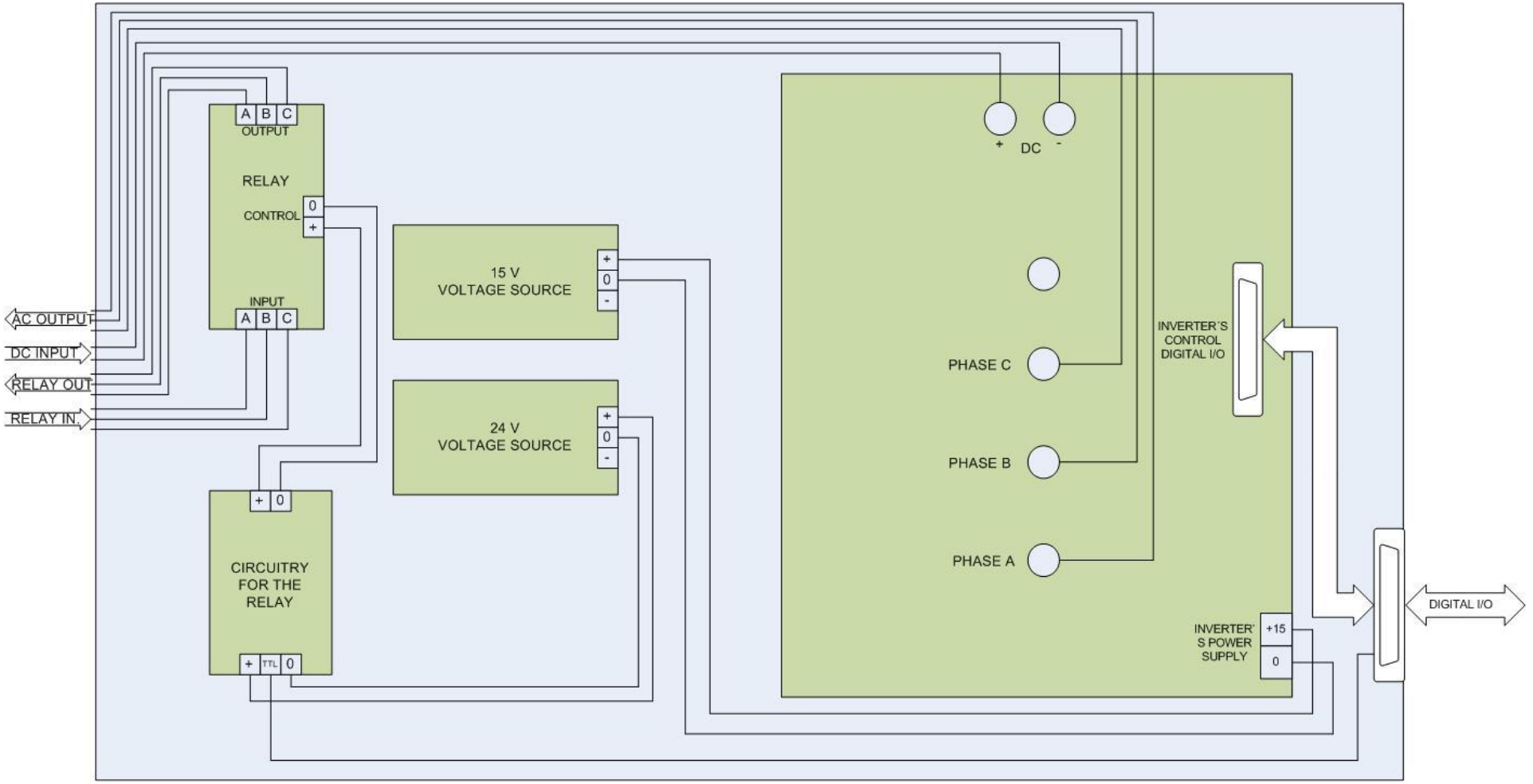
7. Permanent magnet synchronous machine model



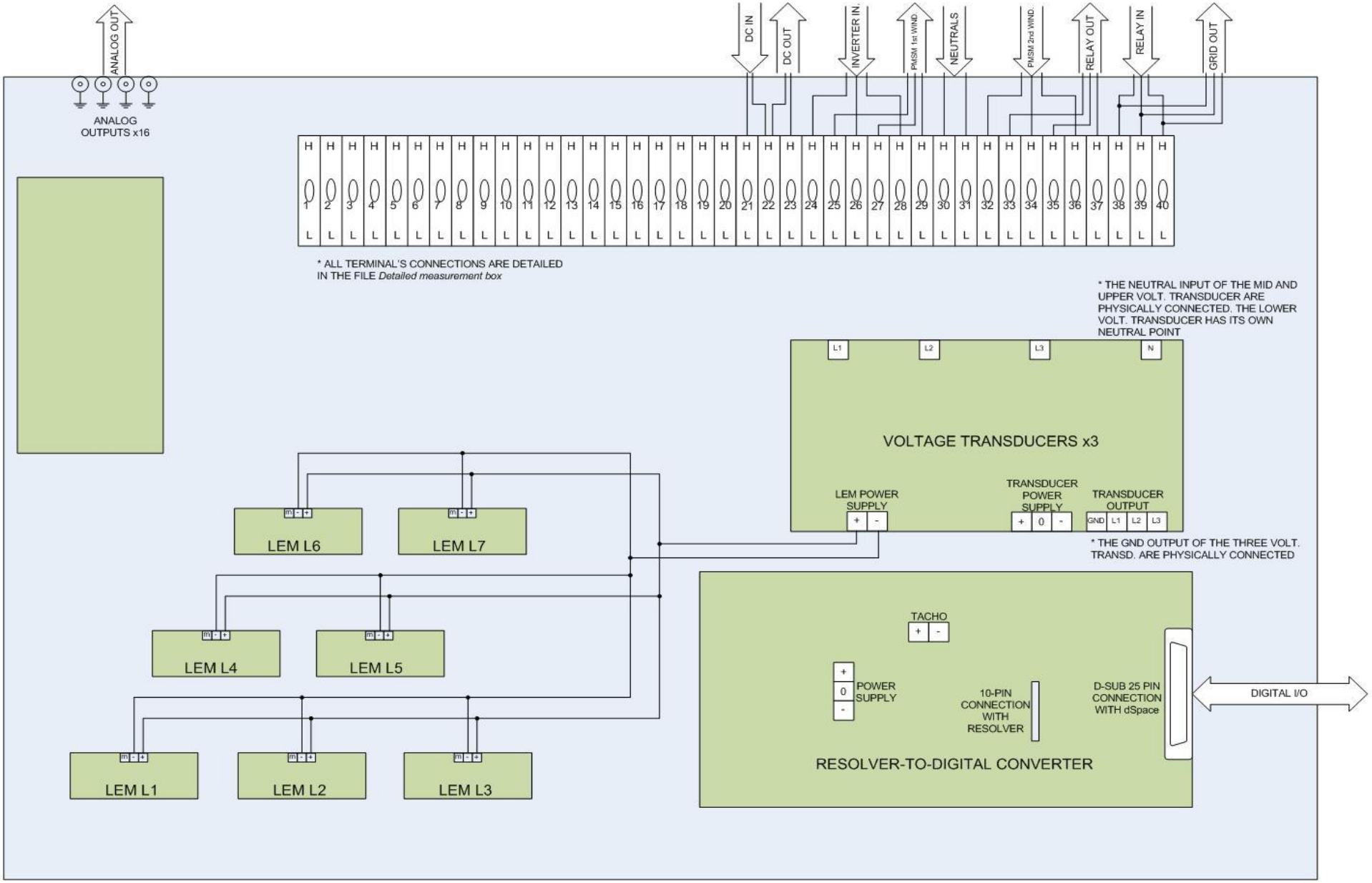
Appendix C. Lab setup diagrams



CHALMERS ELTEKNIK Department of Energy and Environment Division of Electric Power Engineering	TITLE Design, simulation & implementation of a PMSM drive system	DESCRIPTION Layout of the system	FULL FILENAME Overview of power circuitry.vsd					
			DRAWN BY David Vindel	CHECKED BY	SCALE 1: 1	DATE 2011-03-09	REVISED	PAGE 1 OF 1



CHALMERS ELTEKNIK Department of Energy and Environment Division of Electric Power Engineering	TITLE Design, simulation & implementation of a PMSM drive system	DESCRIPTION Inverter's box connections	FULL FILENAME Detailed inverter box.vsd					
			DRAWN BY David Vindel	CHECKED BY	SCALE 1: 1	DATE 2011-03-09	REVISED	PAGE 1 OF 1



CHALMERS ELTEKNIK Department of Energy and Environment Division of Electric Power Engineering	TITLE Design, simulation & implementation of a PMSM drive system	DESCRIPTION Measurement box connections	FULL FILENAME Detailed measurement box.vsd					
			DRAWN BY David Vindel	CHECKED BY	SCALE 1: 1	DATE 2011-03-09	REVISED	PAGE 1 OF 1

TERMINAL PIN	CONNECTED TO
1H	ANALOG OUTPUT 1 (+)
1L	LEM L1 OUPUT
2H	ANALOG OUTPUT 2 (+)
2L	LEM L2 OUPUT
3H	ANALOG OUTPUT 3 (+)
3L	LEM L3 OUPUT
4H	ANALOG OUTPUT 4 (+)
4L	LEM L4 OUPUT
5H	ANALOG OUTPUT 5 (+)
5L	LEM L5 OUPUT
6H	ANALOG OUTPUT 6 (+)
6L	LEM L6 OUPUT
7H	ANALOG OUTPUT 7 (+)
7L	LEM L7 OUPUT
8H	-15 V
8L	TRANSD. & RESOLV. POWER SUPPLY
9H	0 V
9L	TRANSD. & RESOLV. POWER SUPPLY
10H	+15 V
10L	TRANSD. & RESOLV. POWER SUPPLY
11H	ANALOG OUTPUT 16 (+)
11L	TACHO (+)
12H	ANALOG OUTPUT 16 (-)
12L	TACHO (-)
13H	ANALOG OUTPUT 9-15 (-)
13L	VOLT. TRANSD. OUTPUT (N)
14H	ANALOG OUTPUT 9 (+)

TERMINAL PIN	CONNECTED TO
14L	VOLT. TRANSD. OUT. LOWER (L3)
15H	ANALOG OUTPUT 10 (+)
15L	VOLT. TRANSD. OUT. MID (L1)
16H	ANALOG OUTPUT 11 (+)
16L	VOLT. TRANSD. OUT. MID (L2)
17H	ANALOG OUTPUT 12 (+)
17L	VOLT. TRANSD. OUT. MID (L3)
18H	ANALOG OUTPUT 13 (+)
18L	VOLT. TRANSD. OUT. UPPER (L1)
19H	ANALOG OUTPUT 14 (+)
19L	VOLT. TRANSD. OUT. UPPER (L2)
20H	ANALOG OUTPUT 15 (+)
20L	VOLT. TRANSD. OUT. UPPER (L3)
21H	Vdc (+) (VOLTAGE SOURCE)
21L	VOLT. TRANSD. LOW INPUT (L1) & LEM L1
22H	Vdc (-) (VOLT. SOURCE & INVERTER)
22L	VOLT. TRANSD. LOW INPUT (N)
23H	Vdc (+) (INVERTER)
23L	LEM L1
24H	INVERTER PHASE A
24L	LEM L2
25H	PMSM 1st WINDING PHASE A
25L	LEM L2
26H	INVERTER PHASE B
26L	LEM L3
27H	PMSM 1st WINDING PHASE B
27L	LEM L3

TERMINAL PIN	CONNECTED TO
28H	INVERTER PHASE C
28L	LEM L4
29H	PMSM 1st WINDING PHASE C
29L	LEM L4
30H	PMSM 1st WINDING NEUTRAL
30L	-----
31H	PMSM 2nd WINDING NEUTRAL
31L	VOLT. TRANSD. INPUT MID & UPP. (N)
32H	PMSM 2nd WINDING PHASE A
32L	VOLT. TRANSD. INPUT MID (L1) & LEM L5
33H	RELAY INPUT PHASE A
33L	LEM L5
34H	PMSM 2nd WINDING PHASE B
34L	VOLT. TRANSD. INPUT MID (L2) & LEM L6
35H	RELAY INPUT PHASE B
35L	LEM L6
36H	PMSM 2nd WINDING PHASE C
36L	VOLT. TRANSD. INPUT MID (L3) & LEM L7
37H	RELAY INPUT PHASE C
37L	LEM L7
38H	RELAY OUTPUT PHASE A
38L	VOLT. TRANSD. INPUT UPP. (L1)
39H	RELAY OUTPUT PHASE B
39L	VOLT. TRANSD. INPUT UPP. (L2)
40H	RELAY OUTPUT PHASE C
40L	VOLT. TRANSD. INPUT UPP. (L3)

CHALMERS ELTEKNIK Department of Energy and Environment Division of Electric Power Engineering	TITLE Design, simulation & implementation of a PMSM drive system	DESCRIPTION Wiring of the measurement box	FULL FILENAME Wiring of the measurement box.vsd					
			DRAWN BY David Vindel	CHECKED BY	SCALE 1: 1	DATE 2011-03-09	REVISED	PAGE 1 OF 1

Appendix D. Data sheet of experimental equipments

The experimental equipment used in this thesis is introduced in chapter 3. Each device is constructed with different components as mentioned in D.1. In this appendix, the data sheet, or part of it of each component is attached.

Table D.1: devices and components.

Device	Component	Description
Voltage PBC	UMAT2	Voltage transducer for voltage measurements
	AD210	3-port isolation amplifier
Current Probes	LA50S/SP1	LEM modules for current measurements
Resolver PBC	AD2S83	Resolver to digital transducer
	XR2206	Monolithic function generator
	L272M	Dual operational amplifier
	LM234	Low quad operational amplifier
	PBC scheme	Overall scheme of the PBC
Three-Phase Relay	C3 A30	3-phase relay
	IRF830	Mosfet for the driving circuit

Below, the data sheet of each component is presented. In some cases, the data sheet of one component is too extensive, so only the first pages are included. In case of need of the whole document, it can be found in the web page www.datasheetcatalog.com, as well as in other similar pages.

Current Transducer LA 50-S/SP1

I_{PN} = 50 A

For the electronic measurement of currents : DC, AC, pulsed..., with a galvanic isolation between the primary circuit (high power) and the secondary circuit (electronic circuit).

Electrical data

I_{PN}	Primary nominal r.m.s. current		50		A
I_P	Primary current, measuring range		0 .. ± 100		A
R_M	Measuring resistance		R_{Mmin}	R_{Mmax}	
	with ± 15 V	@ ± 50 A_{max}	0	330	Ω
		@ ± 100 A_{max}	0	100	Ω
I_{SN}	Secondary nominal r.m.s. current		25		mA
K_N	Conversion ratio		1 : 2000		
V_C	Supply voltage (± 5 %)		± 15		V
I_C	Current consumption		10 + I_S		mA
V_d	R.m.s. voltage for AC isolation test, 50 Hz, 1 min		3		kV

Accuracy - Dynamic performance data

X_G	Overall accuracy @ I_{PN}, T_A = 25°C		± 0.5		%
ε_L	Linearity		< 0.1		%
			Typ	Max	
I_O	Offset current @ I_P = 0, T_A = 25°C			± 0.1	mA
I_{OT}	Thermal drift of I_O	- 10°C .. + 70°C	± 0.2	± 0.4	mA
t_r	Response time [1] @ 90 % of I_{PN}		< 1		µs
di/dt	di/dt accurately followed		> 50		A/µs
f	Frequency bandwidth (- 1 dB)		DC .. 150		kHz

General data

T_A	Ambient operating temperature		- 10 .. + 70	°C
T_S	Ambient storage temperature		- 25 .. + 85	°C
R_S	Secondary coil resistance @ T_A = 70°C		130	Ω
m	Mass		45	g
	Standards [2]		EN 50178	

Features

- Closed loop (compensated) current transducer using the Hall effect
- Insulated plastic case recognized according to UL 94-V0.

Special features

- I_P = 0 .. ± 100 A
- K_N = 1 : 2000

Advantages

- Excellent accuracy
- Very good linearity
- Low temperature drift
- Optimized response time
- Wide frequency bandwidth
- No insertion losses
- High immunity to external interference
- Current overload capability.

Applications

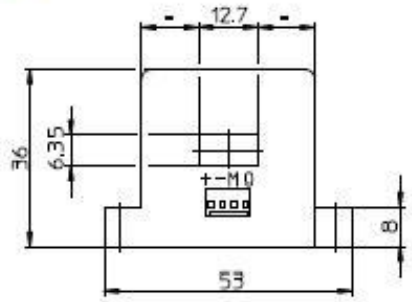
- AC variable speed drives and servo motor drives
- Static converters for DC motor drives
- Battery supplied applications
- Uninterruptible Power Supplies (UPS)
- Switched Mode Power Supplies (SMPS)
- Power supplies for welding applications.

Notes : [1] With a di/dt of 50 A/µs
[2] A list of corresponding tests is available.

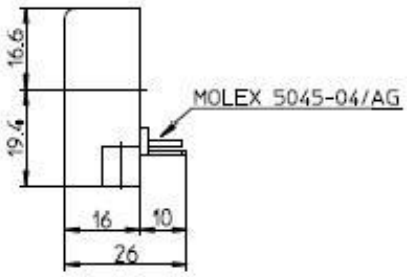
991014/5

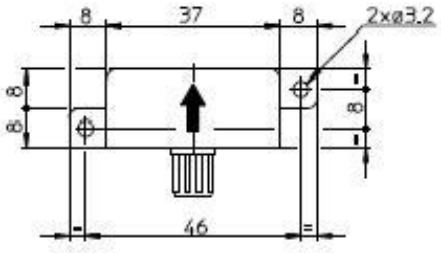
Dimensions LA 50-S/SP1 (in mm. 1 mm = 0.0394 inch)

Front view



Left view



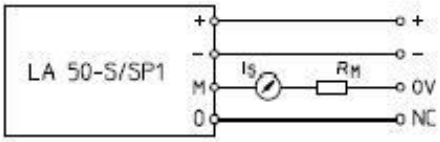


Top view

Secondary terminals

Terminal + : supply voltage + 15 V
Terminal - : supply voltage - 15 V
Terminal M : measure
Terminal 0 : NC

Connection



Mechanical characteristics

• General tolerance	± 0.2 mm
• Fastening	2 holes ∅ 3.2 mm
• Primary through-hole	12.7 x 6.35 mm
• Connection of secondary	Molex 5045-04/AG

Remarks

- I_s is positive when I_p flows in the direction of the arrow.
- Temperature of the primary conductor should not exceed 100°C.
- Dynamic performances (di/dt and response time) are best with a single bar completely filling the primary hole.
- In order to achieve the best magnetic coupling, the primary windings have to be wound over the top edge of the device.
- To measure nominal currents of less than 50 A, the optimum accuracy is obtained by having several primary turns (nominal current x number of turns < 50 At).

LEM reserves the right to carry out modifications on its transducers, in order to improve them, without previous notice.

ANALOG DEVICES

Precision, Wide Bandwidth 3-Port Isolation Amplifier

AD210*

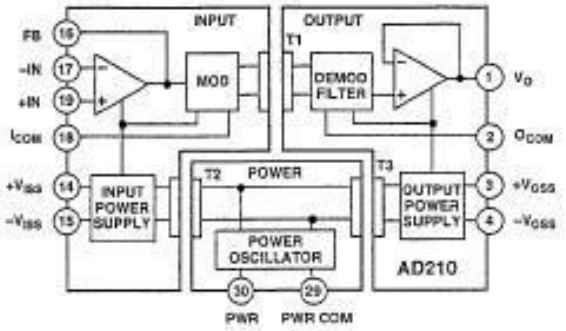
FEATURES

High CMV Isolation: 2500 V rms Continuous
±3500 V Peak Continuous
Small Size: 1.00" × 2.10" × 0.350"
Three-Port Isolation: Input, Output, and Power
Low Nonlinearity: ±0.012% max
Wide Bandwidth: 20 kHz Full-Power (–3 dB)
Low Gain Drift: ±25 ppm/°C max
High CMR: 120 dB (G = 100 V/V)
Isolated Power: ±15 V @ ±5 mA
Uncommitted Input Amplifier

APPLICATIONS

Multichannel Data Acquisition
High Voltage Instrumentation Amplifier
Current Shunt Measurements
Process Signal Isolation

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD210 is the latest member of a new generation of low cost, high performance isolation amplifiers. This three-port, wide bandwidth isolation amplifier is manufactured with surface-mounted components in an automated assembly process. The AD210 combines design expertise with state-of-the-art manufacturing technology to produce an extremely compact and economical isolator whose performance and abundant user features far exceed those offered in more expensive devices.

The AD210 provides a complete isolation function with both signal and power isolation supplied via transformer coupling internal to the module. The AD210's functionally complete design, powered by a single +15 V supply, eliminates the need for an external DC/DC converter, unlike optically coupled isolation devices. The true three-port design structure permits the AD210 to be applied as an input or output isolator, in single or multichannel applications. The AD210 will maintain its high performance under sustained common-mode stress.

Providing high accuracy and complete galvanic isolation, the AD210 interrupts ground loops and leakage paths, and rejects common-mode voltage and noise that may other vise degrade measurement accuracy. In addition, the AD210 provides protection from fault conditions that may cause damage to other sections of a measurement system.

PRODUCT HIGHLIGHTS

The AD210 is a full-featured isolator providing numerous user benefits including:

High Common-Mode Performance: The AD210 provides 2500 V rms (Continuous) and ± 3500 V peak (Continuous) common-mode voltage isolation between any two ports. Low input capacitance of 5 pF results in a 120 dB CMR at a gain of 100, and a low leakage current (2 µA rms max @ 240 V rms, 60 Hz).

High Accuracy: With maximum nonlinearity of ±0.012% (B Grade), gain drift of ± 25 ppm/°C max and input offset drift of (±10 ±30/G) µV/°C, the AD210 assures signal integrity while providing high level isolation.

Wide Bandwidth: The AD210's full-power bandwidth of 20 kHz makes it useful for wideband signals. It is also effective in applications like control loops, where limited bandwidth could result in instability.

Small Size: The AD210 provides a complete isolation function in a small DIP package just 1.00" × 2.10" × 0.350". The low profile DIP package allows application in 0.5" card racks and assemblies. The pinout is optimized to facilitate board layout while maintaining isolation spacing between ports.

Three-Port Design: The AD210's three-port design structure allows each port (Input, Output, and Power) to remain independent. This three-port design permits the AD210 to be used as an input or output isolator. It also provides additional system protection should a fault occur in the power source.

Isolated Power: ±15 V @ 5 mA is available at the input and output sections of the isolator. This feature permits the AD210 to excite floating signal conditioners, front-end amplifiers and remote transducers at the input as well as other circuitry at the output.

Flexible Input: An uncommitted operational amplifier is provided at the input. This amplifier provides buffering and gain as required and facilitates many alternative input functions as required by the user.

*Covered by U.S. Patent No. 4,703,283.

REV. A

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 Fax: 617/326-8703

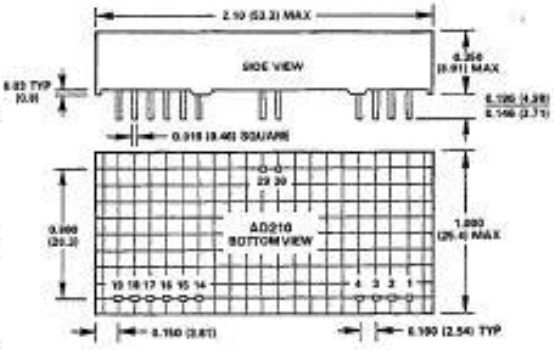
AD210–SPECIFICATIONS (typical @ +25°C, and V_c = +15 V unless otherwise noted)

Model	AD210AN	AD210BN	AD210JN
GAIN			
Range	1 V/V – 100 V/V	*	*
Error	±2% max	±1% max	*
vs. Temperature(0°C to +70°C)	+25 ppm/°C max	*	*
(–25°C to +85°C)	±50 ppm/°C max	*	*
vs. Supply Voltage	±0.002%/V	*	*
Nonlinearity[1]	±0.025% max	±0.012% max	*
INPUT VOLTAGE RATINGS			
Linear Differential Range	±10 V	*	*
Maximum Safe Differential Input	±15 V	*	*
Max. CMV Input-to-Output	*		
ac, 60 Hz, Continuous	2500 V rms	*	1500 V rms
dc, Continuous	±3500 V peak	*	±2000 V peak
Common-Mode Rejection	*		
60 Hz, G = 100 V/V	*		
R_S ≤ 500 Ω Impedance Imbalance	120 dB	*	*
Leakage Current Input-to-Output	*		
@ 240 V rms, 60 Hz	2 μA rms max	*	*
INPUT IMPEDANCE			
Differential	10^{12} Ω	*	*
Common Mode	5 GΩ‖5 pF	*	*
INPUT BIAS CURRENT			
Initial, @ +25°C	30 pA typ (400 pA max)	*	*
vs. Temperature (0°C to +70°C)	10 nA max	*	*
(–25°C to +85°C)	50 nA max	*	*
INPUT DIFFERENCE CURRENT			
Initial, @ +25°C	5 pA typ (200 pA max)	*	*
vs. Temperature(0°C to + 70°C)	2 nA max	*	*
(–25°C to +85°C)	10 nA max	*	*
INPUT NOISE			
Voltage (1 kHz)	18 nV/√Hz	*	*
(10 Hz to 10 kHz)	4 μV rms	*	*
Current (1 kHz)	0.01 pA/√Hz	*	*
FREQUENCY RESPONSE			
Bandwidth (–3 dB)	*		
G = 1 V/V	20 kHz	*	*
G = 100 V/V	15 kHz	*	*
Settling Time (±10 mV, 20 V Step)	*		
G = 1 V/V	150 μs	*	*
G = 100 V/V	500 μs	*	*
Slew Rate (G = 1 V/V)	1 V/μs	*	*
OFFSET VOLTAGE (RTI)[2]			
Initial, @ +25°C	±15 ±45/G) mV max	(±5 ±15/G) mV max	*
vs. Temperature (0°C to +70°C)	(±10 ±30/G) μV/°C	*	*
(–25°C to +85°C)	(±10 ±50/G) μV/°C	*	*
RATED OUTPUT[3]			
Voltage, 2 kΩ Load	±10 V min	*	*
Impedance	1 Ω max	*	*
Ripple (Bandwidth = 100 kHz)	10 mV p-p max	*	*
ISOLATED POWER OUTPUTS[4]			
Voltage, No Load	±15 V	*	*
Accuracy	±10%	*	*
Current	±5 mA	*	*
Regulation, No Load to Full Load	See Text	*	*
Ripple	See Text	*	*
POWER SUPPLY			
Voltage, Rated Performance	+15 V dc ± 5%	*	*
Voltage, Operating	+15 V dc ± 10%	*	*
Current, Quiescent	50 mA	*	*
Current, Full Load – Full Signal	80 mA	*	*
TEMPERATURE RANGE			
Rated Performance	–25°C to +85°C	*	*
Operating	–40°C to +85°C	*	*
Storage	–40°C to +85°C	*	*
PACKAGE DIMENSIONS			
Inches	1.00 × 2.10 × 0.350	*	*
Millimeters	25.4 × 53.3 × 8.9	*	*

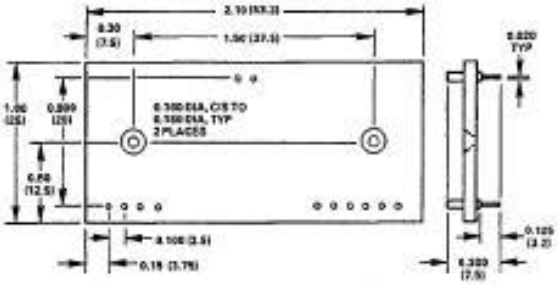
NOTES
*Specifications same as AD210AN.
[1]Nonlinearity is specified as a % deviation from a best straight line..
[2]RTI – Referred to Input.
[3]A reduced signal swing is recommended when both ±V_{ISS} and ±V_{OSS} supplies are fully loaded, due to supply voltage reduction.
[4]See text for detailed information.
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



AC1059 MATING SOCKET



AD210 PIN DESIGNATIONS

Pin	Designation	Function
1	V_O	Output
2	O_{COM}	Output Common
3	+V_{OSS}	+Isolated Power @ Output
4	–V_{OSS}	–Isolated Power @ Output
14	+V_{ISS}	+Isolated Power @ Input
15	–V_{ISS}	–Isolated Power @ Input
16	FB	Input Feedback
17	–IN	–Input
18	I_{COM}	Input Common
19	+IN	+Input
29	Pwr Com	Power Common
30	Pwr	Power Input

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD210 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

1) The input circuit of the voltage transducer card, (UMAT3), is designed in accordance to Fig 5. By omitting components and place a few straps, a circuit like Fig 2 can be achieved.

INSIDE THE AD210

The AD210 basic block diagram is illustrated in Figure 1. A +15 V supply is connected to the power port, and ±15 V isolated power is supplied to both the input and output ports via a 50 kHz carrier frequency. The uncommitted input amplifier can be used to supply gain or buffering of input signals to the AD210. The fullwave modulator translates the signal to the carrier frequency for application to transformer T1. The synchronous demodulator in the output port reconstructs the input signal. A 20 kHz, three-pole filter is employed to minimize output noise and ripple. Finally, an output buffer provides a low impedance output capable of driving a 2 kΩ load.

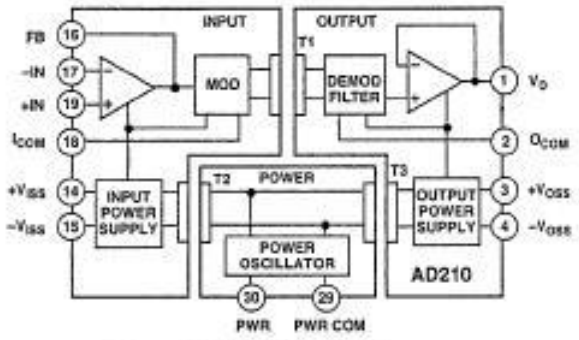


Figure 1. AD210 Block Diagram

USING THE AD210

The AD210 is very simple to apply in a wide range of applications. Powered by a single +15 V power supply, the AD210 will provide outstanding performance when used as an input or output isolator, in single and multichannel configurations.

Input Configurations: The basic unity gain configuration for signals up to ±10 V is shown in Figure 2. Additional input amplifier variations are shown in the following figures. For smaller signal levels Figure 3 shows how to obtain gain while maintaining a very high input impedance.

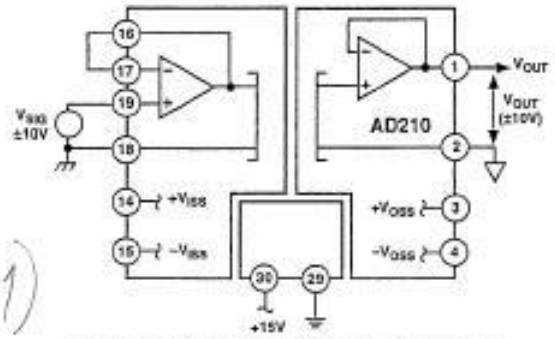


Figure 2. Basic Unity Gain Configuration

The high input impedance of the circuits in Figures 2 and 3 can be maintained in an inverting application. Since the AD210 is a three-port isolator, either the input leads or the output leads may be interchanged to create the signal inversion.

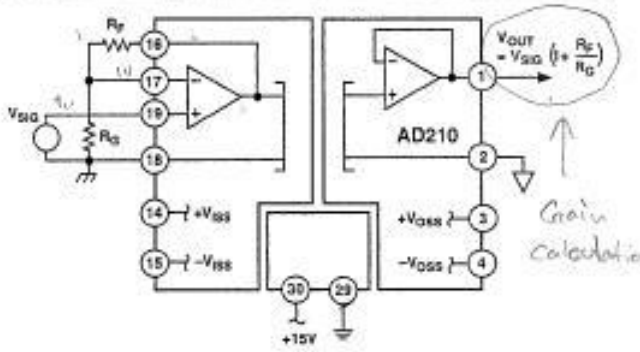


Figure 3. Input Configuration for G > 1

Figure 4 shows how to accommodate current inputs or sum currents or voltages. This circuit configuration can also be used for signals greater than ±10 V. For example, a ±100 V input span can be handled with R_F = 20 kΩ and R_{S1} = 200 kΩ.

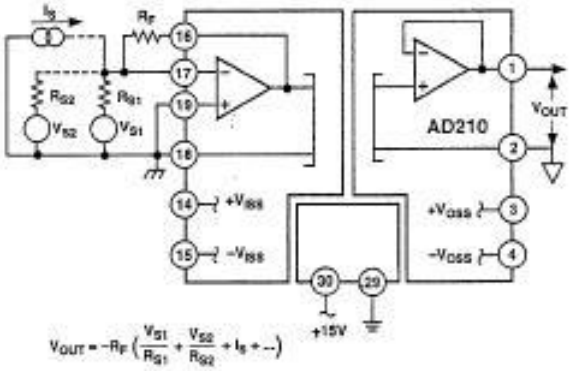


Figure 4. Summing or Current Input Configuration

Adjustments

When gain and offset adjustments are required, the actual circuit adjustment components will depend on the choice of input configuration and whether the adjustments are to be made at the isolator's input or output. Adjustments on the output side might be used when potentiometers on the input side would represent a hazard due to the presence of high common-mode voltage during adjustment. Offset adjustments are best done at the input side, as it is better to null the offset ahead of the gain.

Figure 5 shows the input adjustment circuit for use when the input amplifier is configured in the noninverting mode. This offset adjustment circuit injects a small voltage in series with the

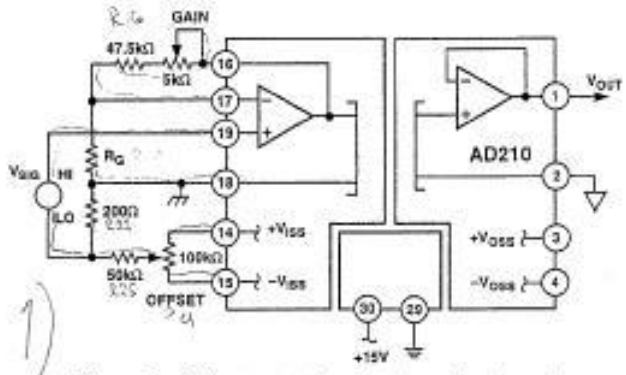


Figure 5. Adjustments for Noninverting Input

low side of the signal source. This will not work if the source has another current path to input common or if current flows in the signal source LO lead. To minimize CMR degradation, keep the resistor in series with the input LO below a few hundred ohms.

Figure 5 also shows the preferred gain adjustment circuit. The circuit shows R_F of 50 kΩ, and will work for gains of ten or greater. The adjustment becomes less effective at lower gains (its effect is halved at G = 2) so that the pot will have to be a larger fraction of the total R_F at low gain. At G = 1 (follower) the gain cannot be adjusted downward without compromising input impedance; it is better to adjust gain at the signal source or after the output.

Figure 6 shows the input adjustment circuit for use when the input amplifier is configured in the inverting mode. The offset adjustment nulls the voltage at the summing node. This is preferable to current injection because it is less affected by subsequent gain adjustment. Gain adjustment is made in the feedback and will work for gains from 1 V/V to 100 V/V.

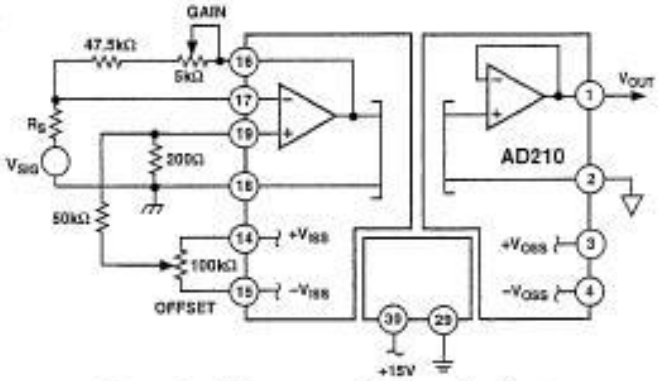


Figure 6. Adjustments for Inverting Input

Figure 7 shows how offset adjustments can be made at the output, by offsetting the floating output port. In this circuit, ±15 V would be supplied by a separate source. The AD210's output amplifier is fixed at unity, therefore, output gain must be made in a subsequent stage.

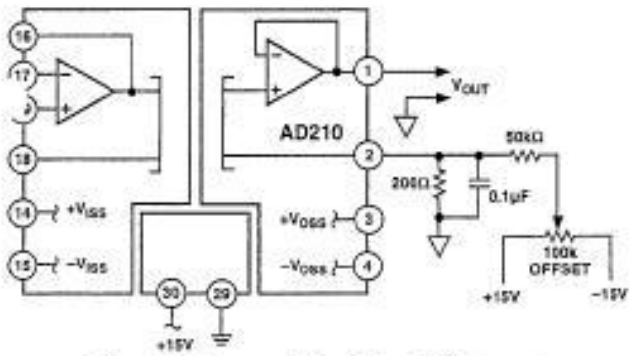


Figure 7. Output-Side Offset Adjustment

PCB Layout for Multichannel Applications: The unique pinout positioning minimizes board space constraints for multichannel applications. Figure 8 shows the recommended printed circuit board layout for a noninverting input configuration with gain.

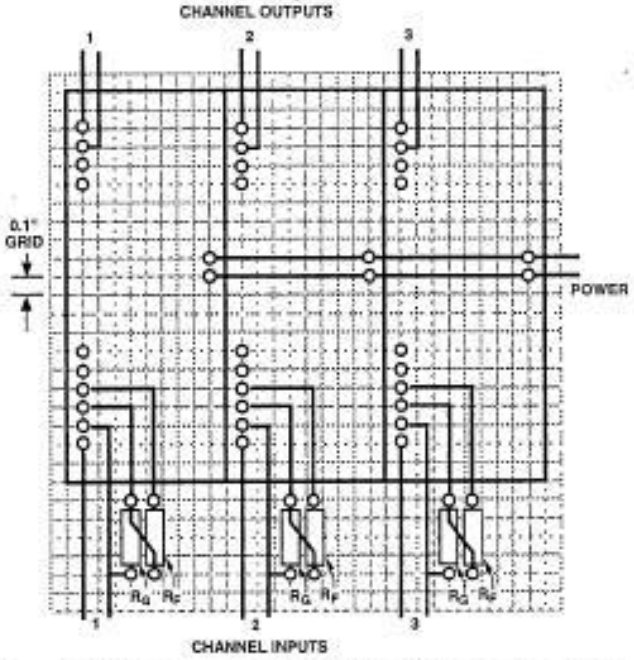


Figure 8. PCB Layout for Multichannel Applications with Gain

Synchronization: The AD210 is insensitive to the clock of an adjacent unit, eliminating the need to synchronize the clocks. However, in rare instances channel to channel pick-up may occur if input signal wires are bundled together. If this happens, shielded input cables are recommended.

PERFORMANCE CHARACTERISTICS

Common-Mode Rejection: Figure 9 shows the common-mode rejection of the AD210 versus frequency, gain and input source resistance. For maximum common-mode rejection of unwanted signals, keep the input source resistance low and carefully lay out the input, avoiding excessive stray capacitance at the input terminals.

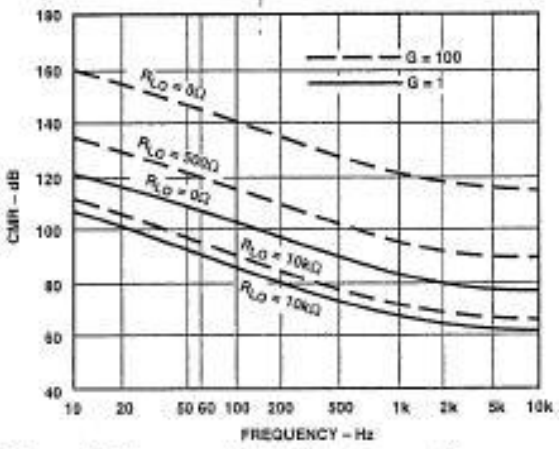


Figure 9. Common-Mode Rejection vs. Frequency

Chemistry, Energy and Environment, Master's Thesis

55

3 polos, contactos inversores

RELECO

C3-A30

Aplicación general

Tres contactos inversores

10A 250V AC1 0,5A 110V DC1
10A 30V DC1 0,5A 220V DC1

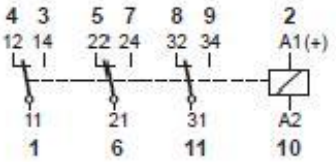


Tabla 1 Vida eléctrica, ops. x 10^6

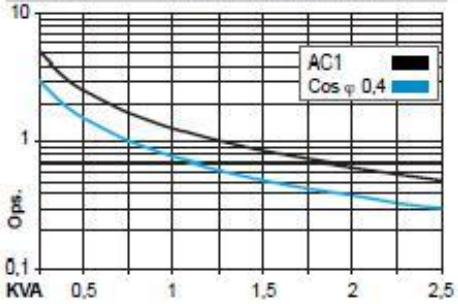
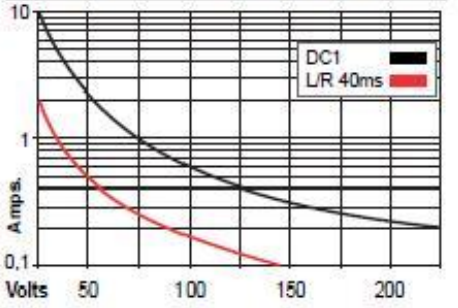
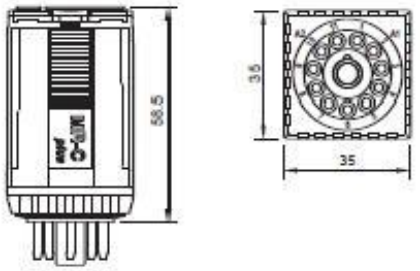


Tabla 2 Carga máxima en CC



Dimensiones mm.



Tipos estándar

CA: 50 Hz, (60 Hz): 24, 48, 115, (120), 230, (240)

	C3-A30	**Vca**
X = LED (estándar)	**C3-A30X**	**Vca**
Supresor RC	**C3-A30R**	**Vca**

CC 24, 48, 110, 220

	C3-A30	**Vcc**
X = LED, sin polaridad (estándar)	**C3-A30X**	**Vcc**
Diodo de paso libre	**C3-A30DX**	**Vcc**
Diodos de paso y polaridad	**C3-A30FX**	**Vcc**
CA/CC rectificador (24,48 y 60V)	**C3-A30BX**	**Vcc**

Relés compatibles con bases **S3-B, S3-S, S3-MP,S3-MS, S3-L y S3-PO**

Contactos

Materiales: Estándar, código 0	AgNi
Opción, código 8	AgNi + 10µ Au
Opción, código 9	AgNi + 0,2µ Au
Intensidad máxima	10 A
Sobrecarga instantánea (20 ms.)	30 A
Tensión máxima	250 V
Carga máxima en CA (Tabla 1)	2,5 KVA
Carga máxima en CC	ver Tabla 2
Corriente mínima recomendada	10 mA / 10 V

Bobinas (Ohms ± 10% @ 20°C)

Voltaje de operación	≤ 0,8 x **Un**
Voltaje de apertura	≥ 0,1 x **Un**
Potencia nominal	2,2 VA (CA) / 1,3 W (CC)

Vca	Ω	mA	Vcc	Ω	mA
24	67	92	24	443	54
48	296	46	48	1K8	27
115	1K7	19	110	9K2	12
230	7K1	9,5	220	36K1	6

Aislamiento

Rigidez dieléctrica, (Vrms/1min.)	
Contacto abierto	1.000 V
Entre contactos adyacentes	2,5 KV
Entre contactos y bobina	2,5 KV
Resistencia de aislamiento a 500V	≥ 3GΩ
Aislamiento según IEC 61810-5	2,5 KV/ 3

Especificaciones

Tiempo de operación	16 ms.
Tiempo de apertura + rebote	8 ms.
Temperatura ambiente	-40°C (sin hielo) ... +70°C
Vida mecánica, ops.	10 mill. en CA y 20 mill. en CC
Vida eléctrica a carga nominal	≥100.000 ops.
Frecuencia de operación a carga nominal	1.200 / hora
Grado de protección	IP40 / RT1
Peso aproximado	95 grs.

IEC 61810 EN 60947

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Time Rise Time	V_{DD} = 250 V I_D = 2.9 A R_G = 4.7 Ω V_{GS} = 10 V (see test circuit, figure 3)		11.5 8		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD} = 400 V I_D = 3 A V_{GS} = 10 V		22 7.2 8	30	nC nC nC

SWITCHING OFF

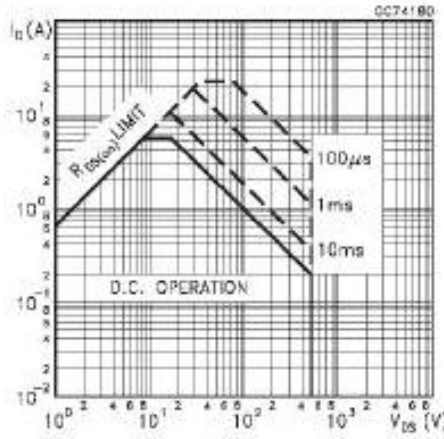
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$ t_f t_c	Off-voltage Rise Time Fall Time Cross-over Time	V_{DD} = 400 V I_D = 4.5 A R_G = 4.7 Ω V_{GS} = 10 V (see test circuit, figure 5)		7 5 15		ns ns ns

SOURCE DRAIN DIODE

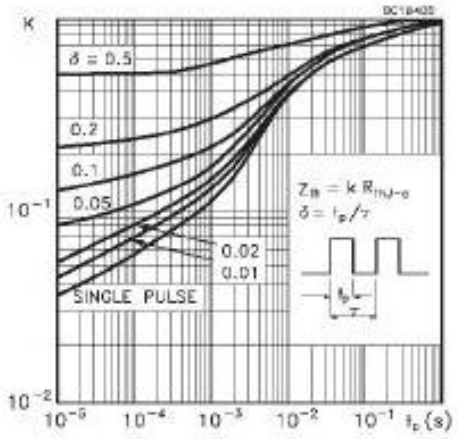
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}(•)	Source-drain Current Source-drain Current (pulsed)				4.5 18	A A
V_{SD} (*)	Forward On Voltage	I_{SD} = 4.5 A V_{GS} = 0			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 4.5 A di/dt = 100 A/µs V_{DD} = 100 V T_j = 150 °C (see test circuit, figure 5)		435 3.3 15		ns µC A

(*) Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %
(•) Pulse width limited by safe operating area

Safe Operating Area



Thermal Impedance



ANALOG DEVICES

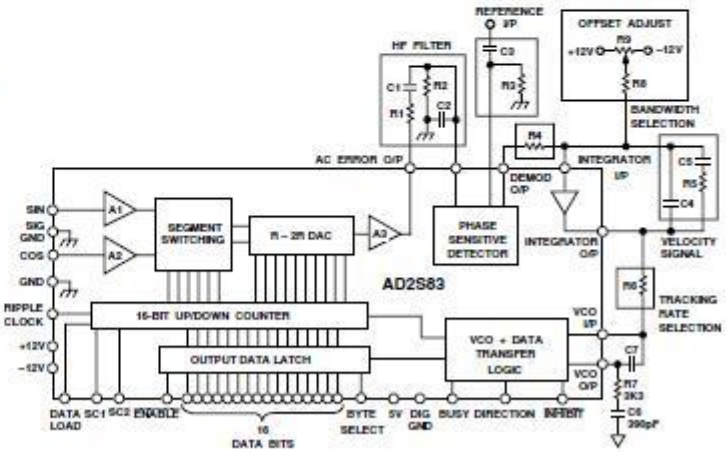
Variable Resolution, Resolver-to-Digital Converter

AD2S83

FEATURES
Tracking R/D Converter
High Accuracy Velocity Output
High Max Tracking Rate 1040 RPS (10 Bits)
44-Lead PLCC Package
10-, 12-, 14-, or 16-Bit Resolution Set by User
Ratiometric Conversion
Stabilized Velocity Reference
Dynamic Performance Set by User
Industrial Temperature Range

APPLICATIONS
DC and AC Servo Motor Control
Process Control
Numerical Control of Machine Tools
Robotics
Axis Control

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD2S83 is a monolithic 10-, 12-, 14-, or 16-bit tracking resolver-to-digital converter.

The converter allows users to *select their own resolution and dynamic performance with external components.* The converter allows users to select the resolution to be 10, 12, 14, or 16 bits and to track resolver signals rotating at up to 1040 revs per second (62,400 rpm) when set to 10-bit resolution.

The AD2S83 converts resolver format input signals into a parallel natural binary digital word using a ratiometric tracking conversion method. This ensures high noise immunity and tolerance of long leads allowing the converter to be located remote from the resolver.

The position output from the converter is presented via 3-state output pins which can be configured for operations with 8- or 16-bit bus. BYTE SELECT, $\overline{\text{ENABLE}}$ and $\overline{\text{INHIBIT}}$ pins ensure easy data transfer to 8- and 16-bit data bus, and outputs are provided to allow for cycle or pitch counting in external counters.

A precise analog signal proportional to velocity is also available and will replace a tachogenerator.

The AD2S83 operates over reference frequencies in the range 0 Hz to 20,000 Hz.

PRODUCT HIGHLIGHTS

High Accuracy Velocity Output. A precision analog velocity signal with a typical linearity of ±0.1% and reversion error less than ±0.3% is generated by the AD2S83. The provision of this signal removes the need for mechanical tachogenerators used in servo systems to provide loop stabilization and speed control.

Resolution Set by User. Two control pins are used to select the resolution of the AD2S83 to be 10, 12, 14 or 16 bits allowing optimum resolution for each application.

Ratiometric Tracking Conversion. This technique provides continuous output position data without conversion delay. It also provides noise immunity and tolerance of harmonic distortion on the reference and input signals.

Dynamic Performance Set by the User. By selecting external resistor and capacitor values the user can determine bandwidth, maximum tracking rate and velocity scaling of the converter to match the system requirements. The component values are easy to select using the free component selection software design aid.

MODELS AVAILABLE

Information on the models available is given in the Ordering Guide.

REV. E

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AD2S83–SPECIFICATIONS ($\pm V_S = \pm 12$ V dc ± 5%; $V_L = 5$ V dc ± 10%; $T_A = -40°C$ to $+85°C$)

Parameter	Conditions	Min	Typ	Max	Unit
SIGNAL INPUTS (SIN, COS)					
Frequency[1]		0		20,000	Hz
Voltage Level		1.8	2.0	2.2	V rms
Input Bias Current			60	150	nA
Input Impedance		1.0			MΩ
REFERENCE INPUT (REF)					
Frequency		0		20,000	Hz
Voltage Level		1.0		8.0	V pk
Input Bias Current			60	150	nA
Input Impedance		1.0			MΩ
PERFORMANCE					
Repeatability				1	LSB
Allowable Phase Shift	(Signals to Reference)	–10		+10	Degree
Max Tracking Rate	10 Bits	1040			rps
	12 Bits	260			rps
	14 Bits	65			rps
	16 Bits	16.25			rps
Bandwidth	User Selectable				
ACCURACY					
Angular Accuracy	A, I			**±8 +1 LSB**	arc min
Monotonicity	Guaranteed Monotonic				
Missing Codes (16-Bit Resolution)	A, I			**4**	Codes
VELOCITY SIGNAL					
LINEARITY[2, 3, 4]					
AD2S83AP					
0 kHz–500 kHz	–40°C to +85°C		±0.15	**±0.25**	% FSR
0.5 MHz–1 MHz	–40°C to +85°C		±0.25	**±1.0**	% FSR
AD2S83IP					
0 kHz–500 kHz	–40°C to +85°C		±0.25	**±0.5**	% FSR
0.5 MHz–1 MHz	–40°C to +85°C		±0.25	**±1.0**	% FSR
Reversion Error					
AD2S83AP	–40°C to +85°C		±0.5	**±1.0**	% O/P
AD2S83IP	–40°C to +85°C		±1.0	**±1.5**	% O/P
DC Zero Offset[5]			±3		mV
Gain Scaling Accuracy			±1.5	**±3**	% FSR
Output Voltage	1 mA Load	±8			V
Dynamic Ripple	Mean Value			1.0	% rms O/P
INPUT/OUTPUT PROTECTION					
Analog Inputs	Overvoltage Protection		±8		V
Analog Outputs	Short Circuit O/P Protection	±5.6	±8	±10.4	mA
DIGITAL POSITION					
Resolution	10, 12, 14, and 16				Bits
Output Format	Bidirectional Natural Binary				
Load				3	LSTTL
$\overline{\text{INHIBIT}}$[6]					
Sense	Logic LO to $\overline{\text{INHIBIT}}$				
Time to Stable Data		240	390	490	ns
$\overline{\text{ENABLE}}$[6]	Logic LO Enables Position Output				
$\overline{\text{ENABLE}}$[6]/Disable Time	Logic HI Outputs in High Impedance State	35		110	ns
BYTE SELECT[6]					
Sense					
Logic HI	MS Byte DB1–DB8				
Logic LO	LS Byte DB1–DB8				
Time to Data Available		60		140	ns
SHORT CYCLE INPUTS	Internally Pulled High via 100 kΩ to $+V_S$				
SC1 SC2					
0 0	10-Bit Resolution				
0 1	12-Bit Resolution				
1 0	14-Bit Resolution				
1 1	16-Bit Resolution				

Parameter	Conditions	Min	Typ	Max	Unit
$\overline{\text{COMPLEMENT}}$	Internally Pulled High via 100 kΩ to $+V_S$. Logic LO to Activate; No Connect for Normal Operation				
$\overline{\text{DATA LOAD}}$					
Sense	Internally Pulled High via 100 kΩ to $+V_S$. Logic LO Allows Data to be Loaded into the Counters from the Data Lines		150	300	ns
BUSY[6, 7]					
Sense	Logic HI When Position O/P Changing				
Width		150		350	ns
Load	Use Additional Pull-Up (See Figure 2)			1	LSTTL
DIRECTION[6]					
Sense	Logic HI Counting Up Logic LO Counting Down				
Max Load				3	LSTTL
RIPPLE CLOCK[6]					
Sense	Logic HI All 1s to All 0s All 0s to All 1s				
Width	Dependent on Input Velocity	300			ns
Reset	Before Next Busy				
Load				3	LSTTL
DIGITAL INPUTS					
Input High Voltage, V_{IH}	$\overline{\text{INHIBIT}}$, $\overline{\text{ENABLE}}$ DB1–DB16, Byte Select $\pm V_S = \pm 11.4$ V, $V_L = 5.0$ V	2.0			V
Input Low Voltage, V_{IL}	$\overline{\text{INHIBIT}}$, $\overline{\text{ENABLE}}$ DB1–DB16, Byte Select $\pm V_S = \pm 12.6$ V, $V_L = 5.0$ V			0.8	V
DIGITAL INPUTS					
Input High Current, I_{IH}	$\overline{\text{INHIBIT}}$, $\overline{\text{ENABLE}}$ DB1–DB16 $\pm V_S = \pm 12.6$ V, $V_L = 5.5$ V			±100	µA
Input Low Current, I_{IL}	$\overline{\text{INHIBIT}}$, $\overline{\text{ENABLE}}$ DB1–DB16, Byte Select $\pm V_S = \pm 12.6$ V, $V_L = 5.5$ V			±100	µA
DIGITAL INPUTS					
Low Voltage, V_{IL}	$\overline{\text{ENABLE}}$ = HI SC1, SC2, $\overline{\text{DATA LOAD}}$ $\pm V_S = \pm 12.0$ V, $V_L = 5.0$ V			1.0	V
Low Current, I_{IL}	$\overline{\text{ENABLE}}$ = HI SC1, SC2, $\overline{\text{DATA LOAD}}$ $\pm V_S = \pm 12.0$ V, $V_L = 5.0$ V			–400	µA
DIGITAL OUTPUTS					
High Voltage, V_{OH}	DB1–DB16 RIPPLE CLK, DIR $\pm V_S = \pm 12.0$ V, $V_L = 4.5$ V $I_{OH} = 100$ µA	2.4			V
Low Voltage, V_{OL}	DB1–DB16 RIPPLE CLK, DIR $\pm V_S = \pm 12.0$ V, $V_L = 5.5$ V $I_{OL} = 1.2$ mA			0.4	V

NOTES
[1]Angular accuracy is not guaranteed <50 Hz reference frequency.
[2]Linearity derates from 500 kHz–1000 kHz @ 0.0017%/kHz.
[3]Refer to Definition of Linearity, "The AD2S83 as a Silicon Tachogenerator."
[4]Worst case reversion error at temperature extremes.
[5]Velocity output offset dependent on value for R6.
[6]Refer to timing diagram.
[7]Busy pulse guaranteed up to a VCO rate of 900 kHz.

All min and max specifications are guaranteed. Specifications in **boldface** are tested on all production units at final electrical test. Specifications subject to change without notice.

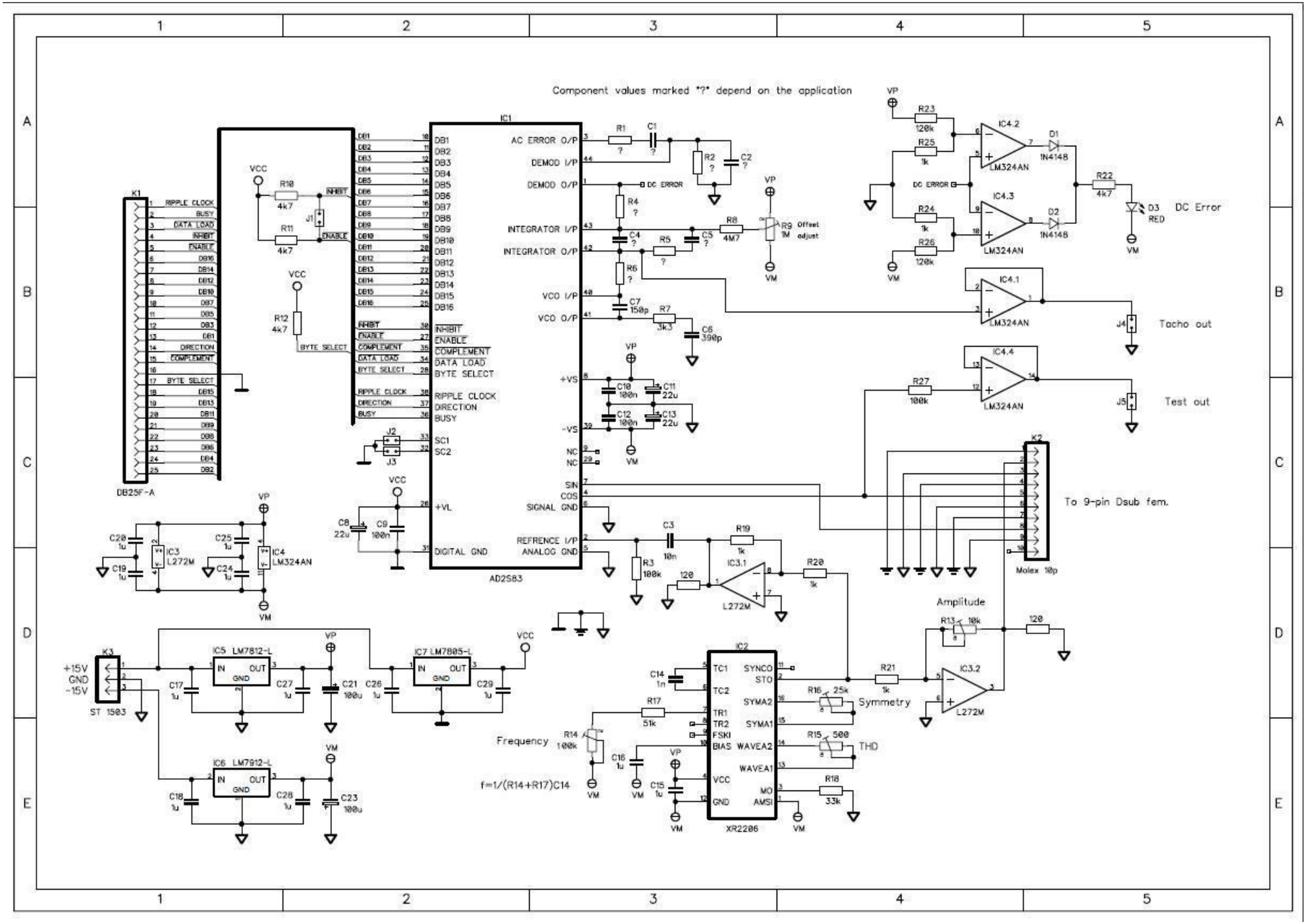
AD2S83–SPECIFICATIONS ($\pm V_S = \pm 12$ V dc ± 5%; $V_L = 5$ V dc ± 10%; $T_A = -40°C$ to $+85°C$)

Parameter	Conditions	Min	Typ	Max	Unit
THREE-STATE LEAKAGE	DB1–DB16 Only				
Current I_L	$\pm V_S = \pm 12.0$ V, $V_L = 5.5$ V $V_{OL} = 0$ V			**±20**	µA
	$\pm V_S = \pm 12.0$ V, $V_L = 5.5$ V $V_{OH} = 5.0$ V			**±20**	µA
RATIO MULTIPLIER					
AC Error Output Scaling	10 Bit		177.6		mV/Bit
	12 Bit		44.4		mV/Bit
	14 Bit		11.1		mV/Bit
	16 Bit		2.775		mV/Bit
PHASE SENSITIVE DETECTOR					
Output Offset Voltage				**12**	mV
Gain					
In Phase	w.r.t. REF	–0.882	–0.9	–0.918	V rms/V dc
In Quadrature	w.r.t. REF			±0.02	V rms/V dc
Input Bias Current			60	**150**	nA
Input Impedance		1.0			MΩ
Input Voltage				±8	V
INTEGRATOR					
Open-Loop Gain	At 10 kHz	57	60	63	dB
Dead Zone Current (Hysteresis)		**90**	100	**110**	nA/LSB
Input Offset Voltage			1	5	mV
Input Bias Current			60	**150**	nA
Output Voltage Range		**±8**			V
VCO					
Maximum Rate		1.1			MHz
VCO Rate	+ve DIR	**8.25**	8.50	**8.75**	kHz/µA
	–ve DIR	**8.25**	8.50	**8.75**	kHz/µA
VCO Power Supply Sensitivity					
Rate	$+V_S$			+0.5	%/V
	$-V_S$			–0.5	%/V
Input Offset Voltage			3		mV
Input Bias Current			12	**50**	nA
Input Bias Current Tempco			+0.22		nA/°C
Linearity of Absolute Rate					
AD2S83AP					
0 kHz–500 kHz			±0.15	**±0.25**	% FSR
0.5 MHz–1 MHz			±0.25	**±1.0**	% FSR
AD2S83IP					
0 kHz–500 kHz			±0.25	**±0.5**	% FSR
0.5 MHz–1 MHz			±0.25	**±1.0**	% FSR
Reversion Error					
AD2S83AP			±0.5	**±1.0**	% Output
AD2S83IP			±1.0	**±1.5**	% Output
POWER SUPPLIES					
Voltage Levels					
$+V_S$		+11.4		+12.6	V
$-V_S$		–11.4		–12.6	V
$+V_L$		+4.5	+5	$+V_S$	V
Current					
$\pm I_S$	$\pm V_S$ @ ±12 V		±12	**±23**	mA
$\pm I_S$	$\pm V_S$ @ ±12.6 V		±19	**±30**	mA
$\pm I_L$	$+V_L$ @ ±5.0 V		±0.5	**±1.5**	mA

All min and max specifications are guaranteed. Specifications in **boldface** are tested on all production units at final electrical test.
Specifications subject to change without notice.

ORDERING GUIDE

Model	Temperature Range	Accuracy	Package Description	Package Option
AD2S83AP	–40°C to +85°C	8 arc min	Plastic Leaded Chip Carrier	P-44A
AD2S83IP	–40°C to +85°C	8 arc min	Plastic Leaded Chip Carrier	P-44A


Component values marked "?" depend on the application
IC1
AD2S83
DB25F-A
K1
K2
K3
IC2
XR2206
IC3
L272M
IC4
LM324AN
IC5 LM7812-L
IC6 LM7912-L
IC7 LM7805-L
IC3.1
IC3.2
IC4.1
IC4.2
IC4.3
IC4.4
AC ERROR O/P
DEMOD I/P
DEMOD O/P
INTEGRATOR I/P
INTEGRATOR O/P
VCO I/P
VCO O/P
SIGNAL GND
REFRENCE I/P
ANALOG GND
DIGITAL GND
DC ERROR
Offset adjust
Tacho out
Test out
To 9-pin Dsub fem.
Molex 10p
Amplitude
Symmetry
Frequency
THD
f=1/(R14+R17)C14
+15V
GND
-15V
ST 1503
1N4148
DC Error
RED

EXAR ...the analog plus company™

XR-2206

Monolithic
Function Generator

February 2008-8

FEATURES

- Low-Sine Wave Distortion, 0.5%, Typical
- Excellent Temperature Stability, 20ppm/°C, Typ.
- Wide Sweep Range, 2000:1, Typical
- Low-Supply Sensitivity, 0.01%V, Typ.
- Linear Amplitude Modulation
- TTL Compatible FSK Controls
- Wide Supply Range, 10V to 26V
- Adjustable Duty Cycle, 1% TO 99%

APPLICATIONS

- Waveform Generation
- Sweep Generation
- AM/FM Generation
- V/F Conversion
- FSK Generation
- Phase-Locked Loops (VCO)

GENERAL DESCRIPTION

The XR-2206 is a monolithic function generator integrated circuit capable of producing high quality sine, square, triangle, ramp, and pulse waveforms of high-stability and accuracy. The output waveforms can be both amplitude and frequency modulated by an external voltage. Frequency of operation can be selected externally over a range of 0.01Hz to more than 1MHz.

The circuit is ideally suited for communications, instrumentation, and function generator applications requiring sinusoidal tone, AM, FM, or FSK generation. It has a typical drift specification of 20ppm/°C. The oscillator frequency can be linearly swept over a 2000:1 frequency range with an external control voltage, while maintaining low distortion.

ORDERING INFORMATION

Part No.	Package	Operating Temperature Range
XR-2206P	16 Lead 300 Mil PDIP	–40°C to +85°C
XR-2206CP	16 Lead 300 Mil PDIP	0°C to +70°C
XR-2206D	16 Lead 300 Mil JEDEC SOIC	0°C to +70°C

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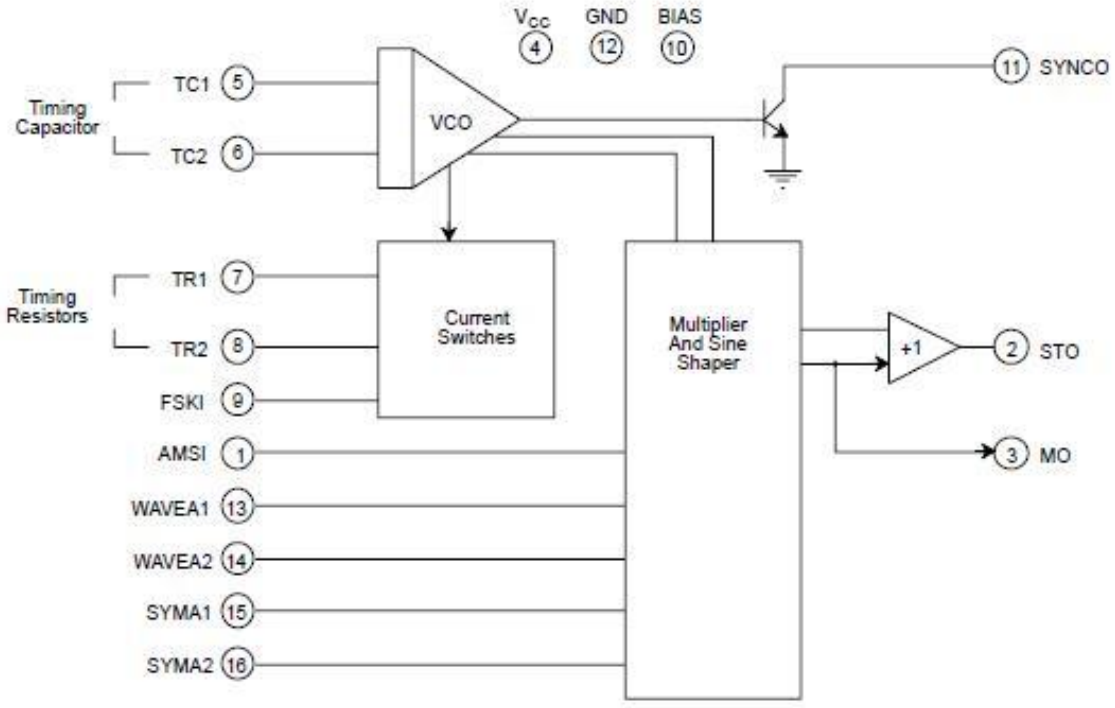
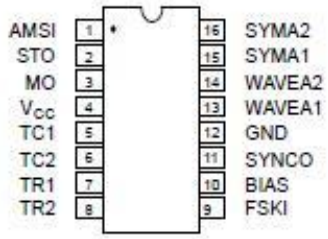
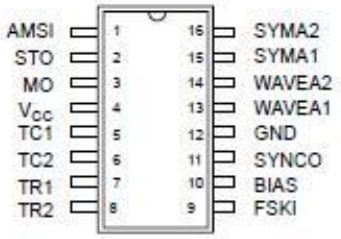


Figure 1. XR-2206 Block Diagram



16 Lead PDIP, CDIP (0.300")



16 Lead SOIC (Jedec, 0.300")

PIN DESCRIPTION

Pin #	Symbol	Type	Description
1	AMSI	I	**Amplitude Modulating Signal Input.**
2	STO	O	**Sine or Triangle Wave Output.**
3	MO	O	**Multiplier Output.**
4	V_{CC}		**Positive Power Supply.**
5	TC1	I	**Timing Capacitor Input.**
6	TC2	I	**Timing Capacitor Input.**
7	TR1	O	**Timing Resistor 1 Output.**
8	TR2	O	**Timing Resistor 2 Output.**
9	FSKI	I	**Frequency Shift Keying Input.**
10	BIAS	O	**Internal Voltage Reference.**
11	SYNCO	O	**Sync Output.** This output is a open collector and needs a pull up resistor to V_{CC}.
12	GND		**Ground pin.**
13	WAVEA1	I	**Wave Form Adjust Input 1.**
14	WAVEA2	I	**Wave Form Adjust Input 2.**
15	SYMA1	I	**Wave Symetry Adjust 1.**
16	SYMA2	I	**Wave Symetry Adjust 2.**

SGS-THOMSON MICROELECTRONICS

L272

DUAL POWER OPERATIONAL AMPLIFIERS

- OUTPUT CURRENT TO 1 A
- OPERATES AT LOW VOLTAGES
- SINGLE OR SPLIT SUPPLY
- LARGE COMMON-MODE AND DIFFERENTIAL MODE RANGE
- GROUND COMPATIBLE INPUTS
- LOW SATURATION VOLTAGE
- THERMAL SHUTDOWN

Powerdip
(8 + 8)

Minidip

SO16 (Narrow)

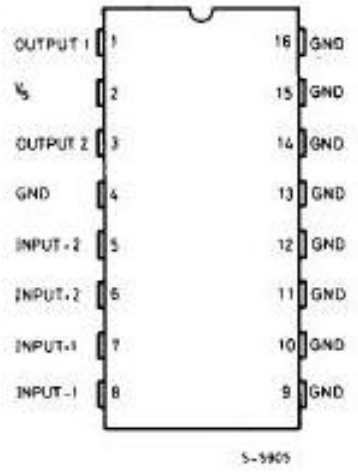
ORDERING NUMBERS : L272 (Powerdip)
L272M (Minidip)
L272D (SO16 Narrow)

DESCRIPTION

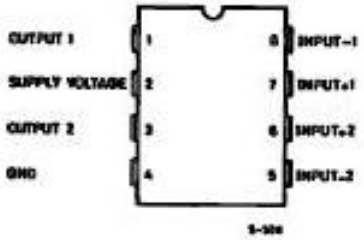
The L272 is a monolithic integrated circuits in Powerdip, Minidip and SO packages intended for use as power operational amplifiers in a wide range of applications including servo amplifiers and power supplies, compacts disc, VCR, etc.

The high gain and high output power capability provide superior performance whatever an operational amplifier/power booster combination is required.

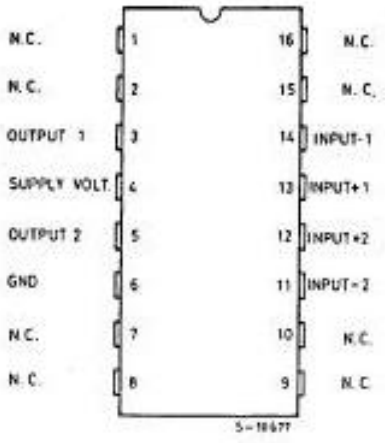
PIN CONNECTIONS (top view)



L272

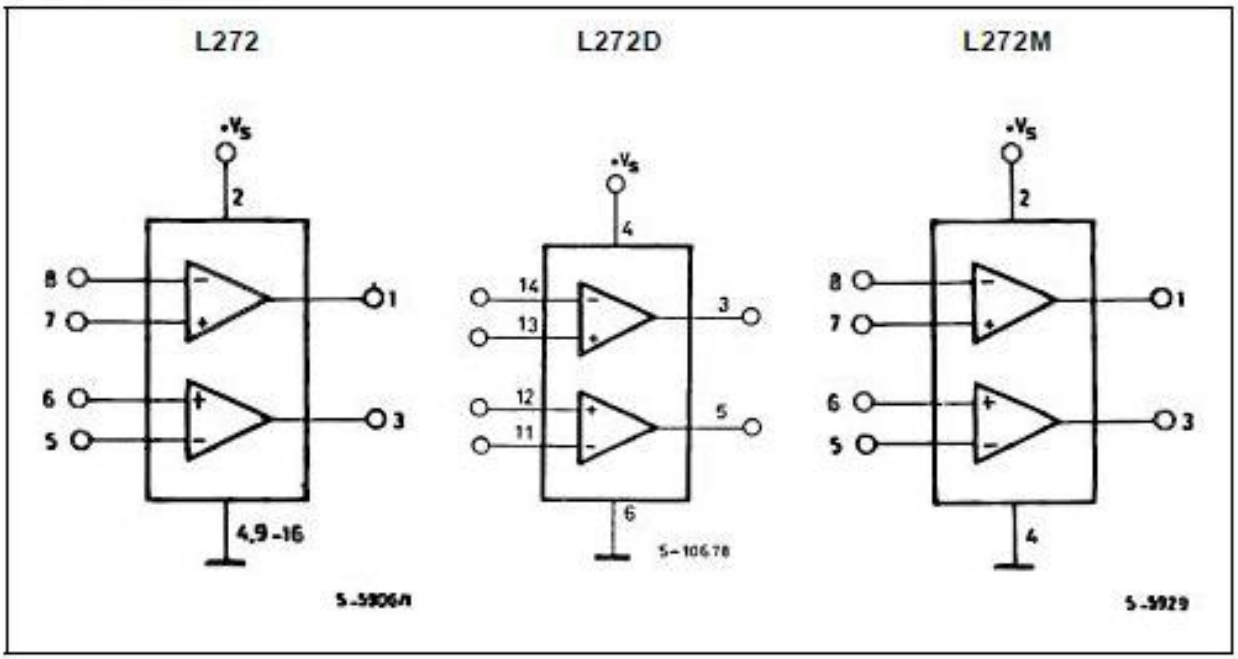


L272M

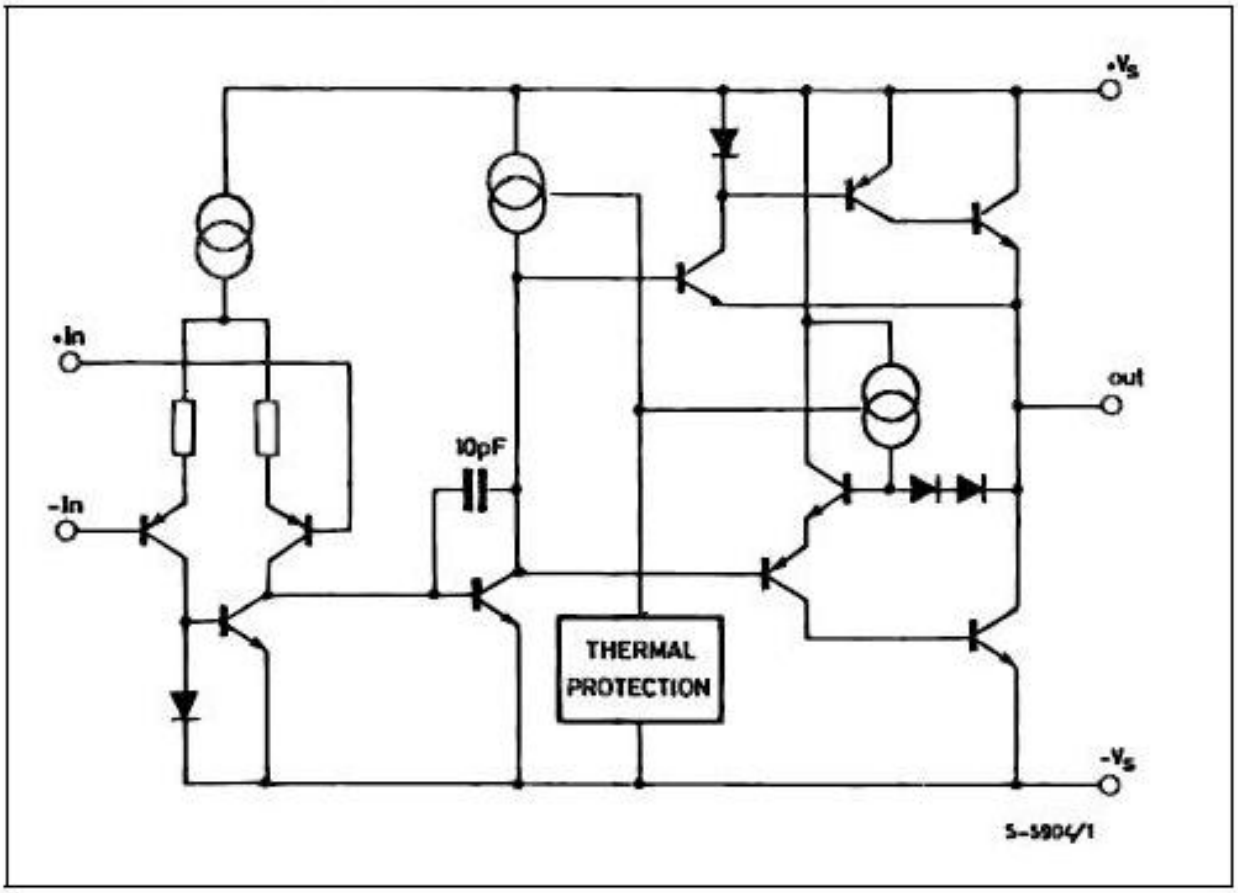


L272D

BLOCK DIAGRAMS



SCHEMATIC DIAGRAM (one only)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage	28	V
V_i	Input Voltage	V_s	
V_i	Differential Input Voltage	$\pm V_s$	
I_o	DC Output Current	1	A
I_p	Peak Output Current (non repetitive)	1.5	A
P_{tot}	Power Dissipation at: T_{amb} = 80°C (L272), T_{amb} = 50°C (L272M), T_{case} = 90 °C (L272D) T_{case} = 75 °C (L272)	1.2 5	W W
T_{op}	Operating Temperature Range (L272D)	– 40 to 85	°C
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

THERMAL DATA

Symbol	Parameter		Powerdip	SO16	Minidip	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-pins	Max.	15	–	* 70	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max.	70	–	100	°C/W
$R_{th\ j\text{-}alumina}$	Thermal Resistance Junction-alumina	Max.	–	** 50	–	°C/W

* Thermal resistance junction-pin 4
** Thermal resistance junctions-pins with the chip soldered on the middle of an alumina supporting substrate measuring 15x 20mm; 0.65mm thickness and infinite heatsink.

ELECTRICAL CHARACTERISTICS (V_S = 24V, T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply Voltage		4		28	V
I_s	Quiescent Drain Current	$V_O = \frac{V_S}{2}$ V_s = 24V V_s = 12V		8 7.5	12 11	mA mA
I_b	Input Bias Current			0.3	2.5	µA
V_{os}	Input Offset Voltage			15	60	mV
I_{os}	Input Offset Current			50	250	nA
SR	Slew Rate			1		V/µs
B	Gain-bandwidth Product			350		kHz
R_i	Input Resistance		500			kΩ
G_v	O. L. Voltage Gain	f = 100Hz f = 1kHz	60	70 50		dB dB
e_N	Input Noise Voltage	B = 20kHz		10		µV
I_N	Input Noise Current	B = 20kHz		200		pA
CRR	Common Mode Rejection	f = 1kHz	60	75		dB
SVR	Supply Voltage Rejection	f = 100Hz, R_G = 10kΩ, V_R = 0.5V V_s = 24V V_s = ± 12V V_s = ± 6V	 54	 70 62 56		dB
V_o	Output Voltage Swing	I_p = 0.1A I_p = 0.5A	 21	23 22.5		V V
C_s	Channel Separation	f = 1 kHz; R_L =10Ω, G_v = 30dB V_s = 24V V_s = ± 6V		 60 60		dB
d	Distortion	f = 1kHz, G_v = 3 dB, V_s = 24V, R_L = ∞		0.5		%
T_{sd}	Thermal Shutdown Junction Temperature			145		°C

National Semiconductor

August 2000

LM124/LM224/LM324/LM2902
Low Power Quad Operational Amplifiers

General Description

The LM124 series consists of four independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, DC gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM124 series can be directly operated off of the standard +5V power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional ±15V power supplies.

Unique Characteristics

- In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage
- The unity gain cross frequency is temperature compensated
- The input bias current is also temperature compensated

Advantages

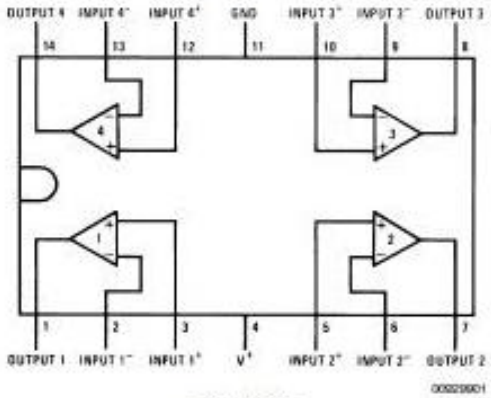
- Eliminates need for dual supplies
- Four internally compensated op amps in a single package
- Allows directly sensing near GND and V_{OUT} also goes to GND
- Compatible with all forms of logic
- Power drain suitable for battery operation

Features

- Internally frequency compensated for unity gain
- Large DC voltage gain 100 dB
- Wide bandwidth (unity gain) 1 MHz (temperature compensated)
- Wide power supply range:
  Single supply 3V to 32V
  or dual supplies ±1.5V to ±16V
- Very low supply current drain (700 µA)—essentially independent of supply voltage
- Low input biasing current 45 nA (temperature compensated)
- Low input offset voltage 2 mV and offset current: 5 nA
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing 0V to V^+ − 1.5V

Connection Diagrams

Dual-In-Line Package



Top View

Order Number LM124J, LM124AJ, LM124J/883 (Note 2), **LM124AJ/883** (Note 1), **LM224J, LM224AJ, LM324J, LM324M, LM324MX, LM324AM, LM324AMX, LM2902M, LM2902MX, LM324N, LM324AN, LM324MT, LM324MTX or LM2902N LM124AJRQML and LM124AJRQMLV**(Note 3)

See NS Package Number J14A, M14A or N14A

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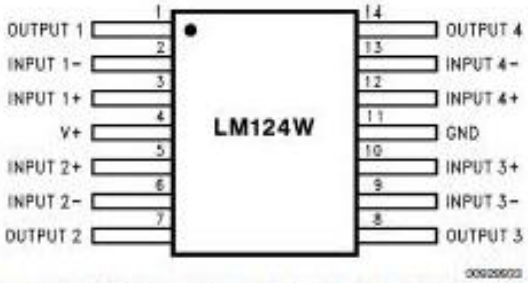
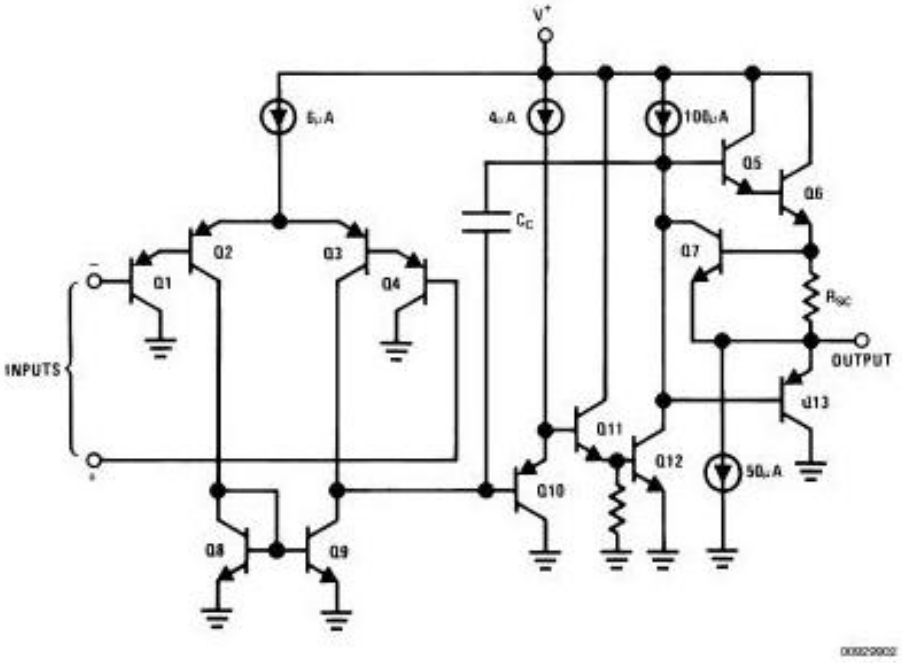
Connection Diagrams (Continued)



Order Number LM124AW/883, LM124AWG/883, LM124W/883 or LM124WG/883
LM124AWRQML and LM124AWRQMLV(Note 3)
See NS Package Number W14B
LM124AWGRQML and LM124AWGRQMLV(Note 3)
See NS Package Number WG14A

Note 1: LM124A available per JM38510/11006
Note 2: LM124 available per JM38510/11005
Note 3: See STD Mil DWG 5962R99504 for Radiation Tolerant Device

Schematic Diagram (Each Amplifier)



Absolute Maximum Ratings (Note 12)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

	LM124/LM224/LM324 LM124A/LM224A/LM324A	LM2902
Supply Voltage, V^+	32V	26V
Differential Input Voltage	32V	26V
Input Voltage	−0.3V to +32V	−0.3V to +26V
Input Current		
(V_{IN} < −0.3V) (Note 6)	50 mA	50 mA
Power Dissipation (Note 4)		
Molded DIP	1130 mW	1130 mW
Cavity DIP	1260 mW	1260 mW
Small Outline Package	800 mW	800 mW
Output Short-Circuit to GND		
(One Amplifier) (Note 5)		
$V^+ \leq 15V$ and $T_A = 25^\circ C$	Continuous	Continuous
Operating Temperature Range		−40°C to +85°C
LM324/LM324A	0°C to +70°C	
LM224/LM224A	−25°C to +85°C	
LM124/LM124A	−55°C to +125°C	
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C	260°C
Soldering Information		
Dual-In-Line Package		
Soldering (10 seconds)	260°C	260°C
Small Outline Package		
Vapor Phase (60 seconds)	215°C	215°C
Infrared (15 seconds)	220°C	220°C
See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.		
ESD Tolerance (Note 13)	250V	250V

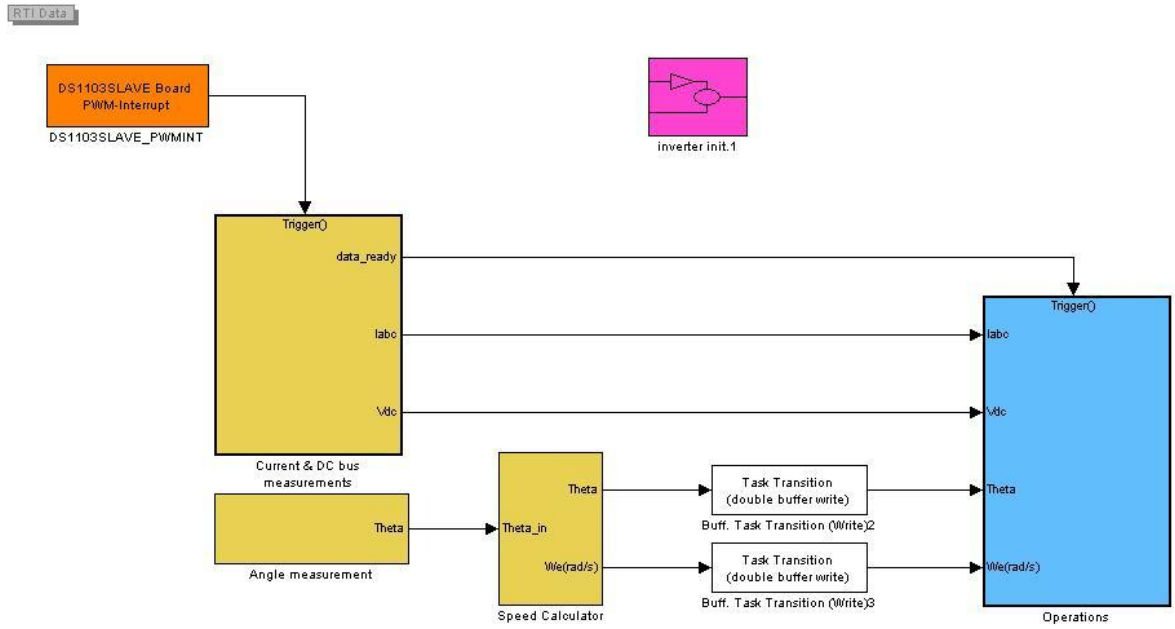
Electrical Characteristics

$V^+ = +5.0V$, (Note 7), unless otherwise stated

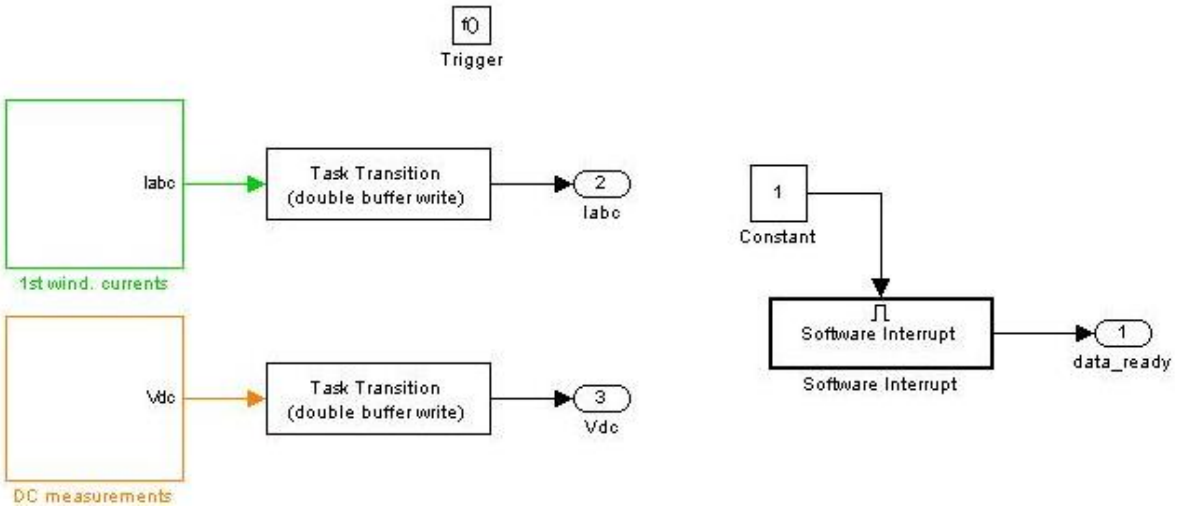
Parameter	Conditions	LM124A			LM224A			LM324A			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 8) $T_A = 25^\circ C$		1	2		1	3		2	3	mV
Input Bias Current (Note 9)	$I_{IN(+)}$ or $I_{IN(-)}$, $V_{CM} = 0V$, $T_A = 25^\circ C$		20	50		40	80		45	100	nA
Input Offset Current	$I_{IN(+)}$ or $I_{IN(-)}$, $V_{CM} = 0V$, $T_A = 25^\circ C$		2	10		2	15		5	30	nA
Input Common-Mode Voltage Range (Note 10)	$V^+ = 30V$, (LM2902, $V^+ = 26V$), $T_A = 25^\circ C$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	V
Supply Current	Over Full Temperature Range $R_L = \infty$ On All Op Amps										mA
	$V^+ = 30V$ (LM2902 $V^+ = 26V$)		1.5	3		1.5	3		1.5	3	
	$V^+ = 5V$		0.7	1.2		0.7	1.2		0.7	1.2	
Large Signal Voltage Gain	$V^+ = 15V$, $R_L \geq 2k\Omega$, ($V_O = 1V$ to $11V$), $T_A = 25^\circ C$	50	100		50	100		25	100		V/mV
Common-Mode	DC, $V_{CM} = 0V$ to $V^+ - 1.5V$,	70	85		70	85		65	85		dB

Appendix E. dSpace software implementation.

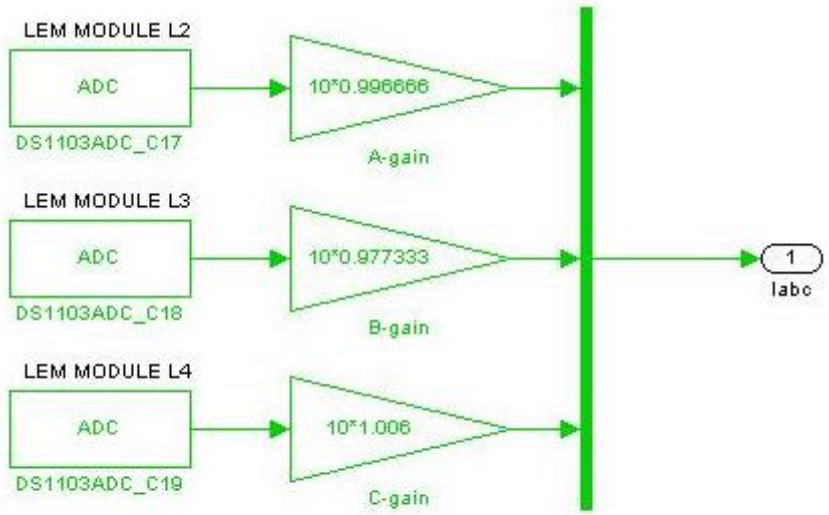
1. Main real-time system.

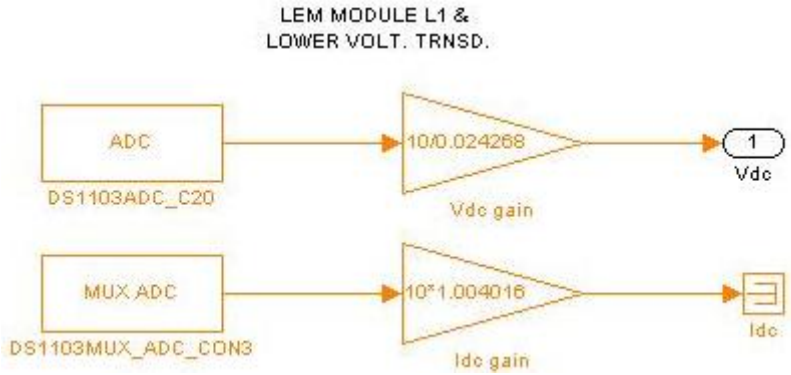


2. Current and DC bus measurements.

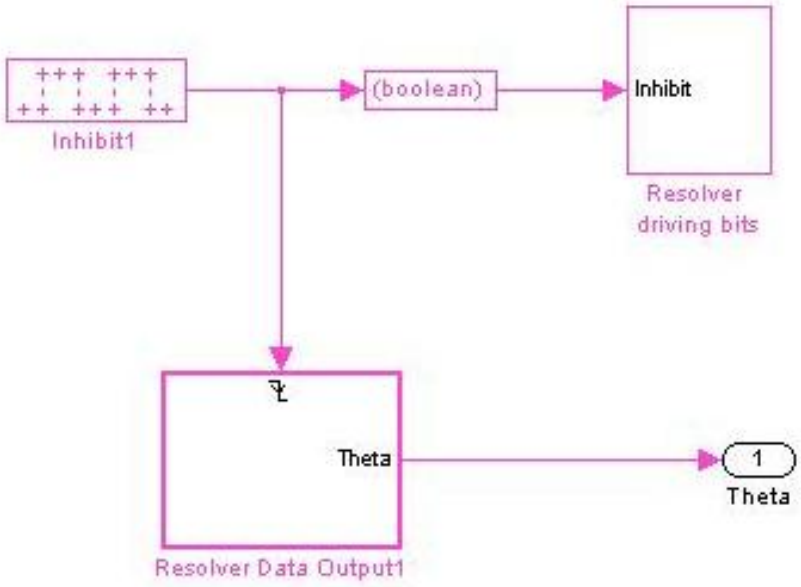


3. Analogue inputs reading.

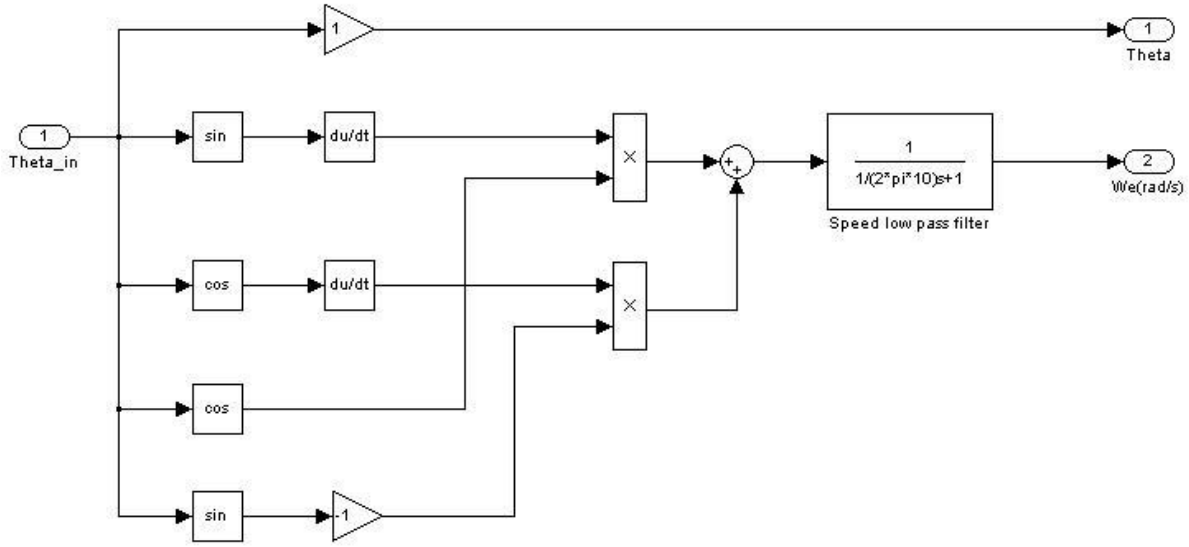




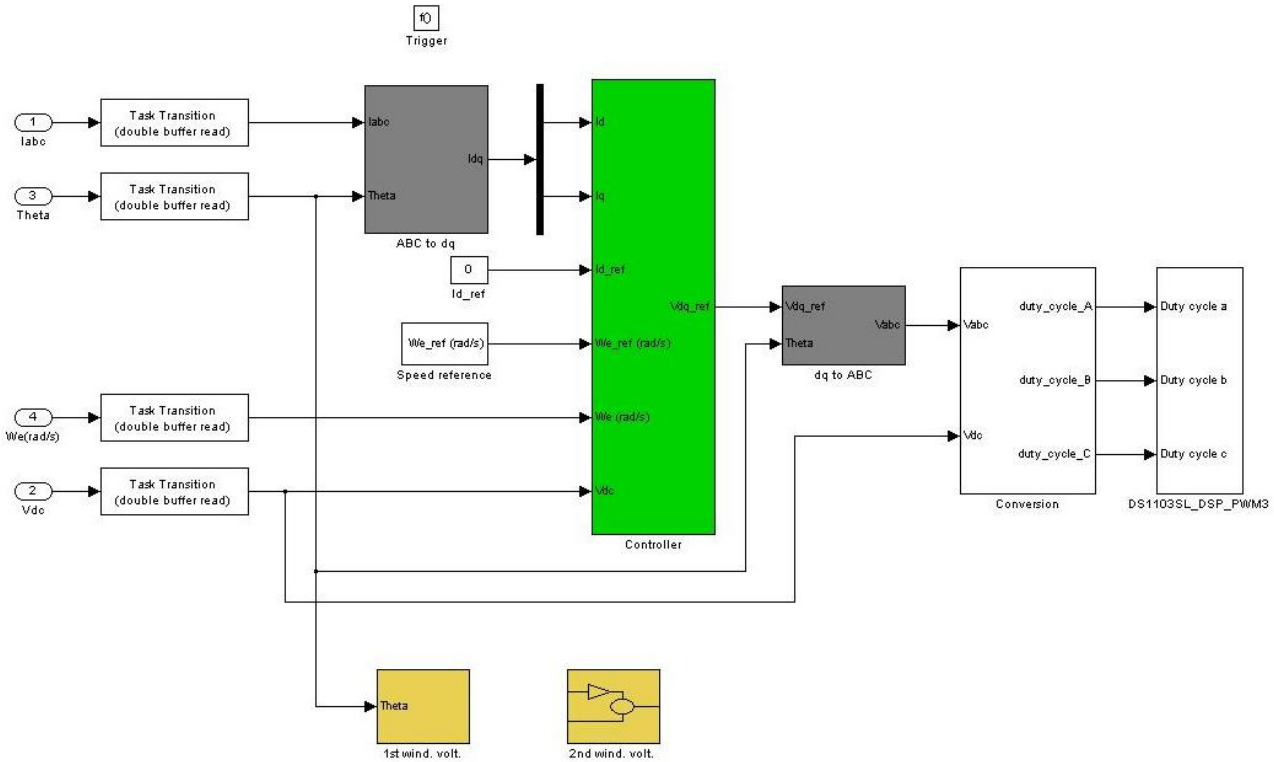
4. Angle measurement.



5. Speed calculation.



6. Operations.



7. Inverter's initialization blocks.