Ochoa, D., Barrado, A., Lázaro, A., Vázquez, R., Sanz, M. (25-28 June 2018). Modeling, control and analysis of input-series-output-parallel-output-series architecture with common-duty-ratio and input filter [proceedings]. IEEE 19th Workshop on Control and Modeling for Power Electronics (COMPEL), Padua, Italy. ISBN 978-1-5386-5541-2

.

DOI: https://doi.org/10.1109/COMPEL.2018.8460043

Modeling, Control and Analysis of Input-Series-Output-Parallel-Output-Series architecture with Common-Duty-Ratio and Input Filter

Diego Ochoa
Power Electronics System Group
Universidad Carlos lll de Madrid
Madrid, Spain
dochoa@ing.uc3m.es

Antonio Lazaro
Power Electronics System Group
Universidad Carlos lll de Madrid
Madrid, Spain
alazaro@ing.uc3m.es

Marina Sanz
Power Electronics System Group
Universidad Carlos lll de Madrid
Madrid, Spain
cmsanz@ing.uc3m.es

Andres Barrado
Power Electronics System Group
Universidad Carlos lll de Madrid
Madrid, Spain
andres.barrado@uc3m.es

Ramon Vazquez
Schaltbau Sepsa
Madrid, Spain
rvazquez@sepsa.es

***Abstract*-This paper introduces a new architecture for modular converters in railway applications and in general in high input voltage - high power applications. This topology consists of four Phase-shift Full Bridge converter which are connected in series at the input while in the output side every two of them are connected in parallel and then be connected in series. A stability analysis which is achieved through input voltage sharing is shown. A small-signal model of Input-Series-Output-Parallel-Output-Series architecture with common duty ratio control is presented. Considering the effect of the input filter over the modular converter, a linear controller is designed. Finally, simulation validates the theoretical predictions.**

Keywords-modular converter, input-series-output-parallel-output-series (TSOPOS), input filter, phase-shift full bridge converter (PS-FBC), PSIM, SmartCtrl.

I. INTRODUCTION

In recent years, modular converters have been an interesting solution for high power-voltage systems, since in topologies of traditional converters there are many limitations when selecting commercial switching devices [1-5]. Modular converters are popular in many applications such as microgrids, railways, wind turbines, etc.

As an application is the use of this architecture in the main converters of the traction systems or auxiliary services in railway applications since those converters operate at hundred-Kilowatt or Megawatt power levels and most common supply voltages go from 600V to 3 kV.

Due to these high-power levels it is necessary to have a converter with galvanic isolation and input filter as shown in fig. 1. In the proposed application there are many advantages to using modular converters because they are scalable systems [4].

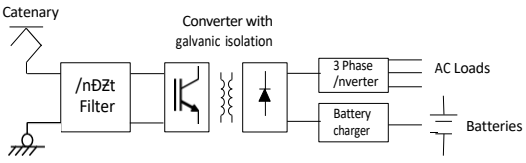

Figure 1: Typical structures of auxiliary converters in railway applications.

The input-series-output-parallel-output-series (ISOPOS) converter proposed consists of four Phase-shift Full Bridge converter (PS-FBC) which are connected in series at the input while in the output side every two of them are connected in parallel and then be connected in series. For each module the input voltage is reduced to V_{in}/k, where k is the number of modules and V_{in} is the input voltage of ISOPOS (in this case $k = 4$). For this reason, it is important to ensure the input voltage sharing (IVS) for the system to be stable and all the modules consume the same power.

Additional, the main purpose of the LC filter at the input of the DC-DC converter is to filter the voltage at connections and disconnections of the pantograph in cross-section changes and gaps. Further, it helps protections work against voltage spikes. Finally, it allows to fulfill the input impedance requirements specified by the railway companies [6].

On the other hand, linear controls in voltage mode and current mode are the most used in DC / DC converters [7], for this reason in this paper it is used the technique of injected-absorbed current method presented in [8] to obtain the following transfer function: control to output voltage (G_{vd}) and control to output voltage (G_{vd_if}) which considers the input filter effect.

Regarding the control of modular converters there are some techniques that allow to guarantee the input voltage sharing (IVS). One of them is described in [9] which it is applied an ISOP converter and consists of having the same number of control loops as modules, this technique uses a decoupling matrix to convert a multiple input multiple output system (MIMO) to single input single output (SISO) system with aim of reaching independent control loops, however in railway application is compulsory to use an LC filter at the input, it is not possible to apply a simple transformation [2]. Nevertheless, in [1] is proposed to have a single control loop that adjusts the duty cycle for all modules, this technique is known as common-duty-ratio control which is the preferred option in railway applications due to its simplicity and usability in field test and start up. Stability analysis of ISOPOS is carried out to verify that converter has natural balancing mechanisms.

II. STABILITY ANALISYS OF PROPOSED TOPOLOGY

This analysis is based on ISOPOS converter which operates in continuous current mode (MCC) and consist of four Phase-shift Full Bridge Converter (PS-FBC), the

architecture is shown in fig. 2. The basic operation principles and main waveforms of PS-FBC have been presented in [10]. One of the advantages of the PS-FBC is the soft switching operation due to phase shift modulation since ZVS can be achieved. In this paper, the ISOPOS converter has a single control loop that adjusts the duty cycle for all modules.

Assuming each module of the converter is identical, in steady-state operation, the input voltage and power in each module is distributed equally, therefore control technique must ensure input voltage sharing (IVS) when there is an individual input voltage or output current perturbation.

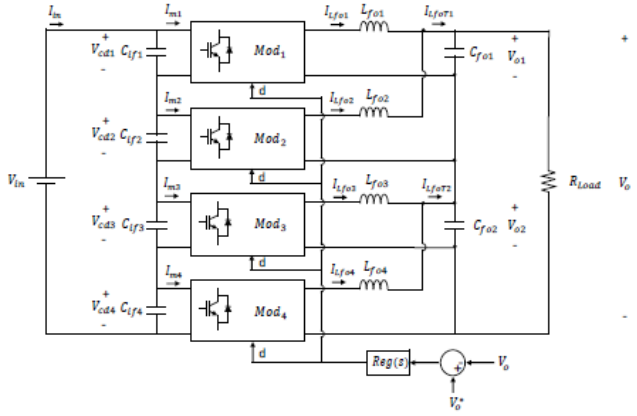

Figure 2: PS-FBC converters in input-series-output-parallel-output-series connection.

As converter is connected in series at the input the following conditions are established:

$$V_{in} = V_{cd1} + V_{cd2} + V_{cd3} + V_{cd4} \quad (1)$$

$$I_{in} = I_{m1} = I_{m2} = I_{m3} = I_{m4} \quad (2)$$

On the other hand, as the output port of each module is connected in parallel and then be connected in series, following conditions are established:

$$I_{LfoT1} = I_{Lfo1} + I_{Lfo2} \quad (3)$$

$$I_{LfoT2} = I_{Lfo3} + I_{Lfo4} \quad (4)$$

$$V_o = V_{o1} + V_{o2} \quad (5)$$

$$I_o = I_{LfoT1} = I_{LfoT2} \quad (6)$$

The following expressions describe the steady state operation of ISOPOS architecture:

$$V_{cd_x} = \frac{V_{in}}{k} \quad (7)$$

$$D_{eff_x} = D - D_{loss_x} \quad (8)$$

$$D_{loss_x} = \frac{R_d \cdot I_{Lfo_x}}{n \cdot V_{cd_x}} \quad (9)$$

$$R_d = 4 \cdot n^2 \cdot L_{lk} \cdot F_{sw} \quad (10)$$

$$D_{eff_x} = \frac{V_{o_x}}{n \cdot V_{cd_x}} \quad (11)$$

The term n represents the turns ratio of transformer, I_{Lfo} is the current of the output filter inductor, V_{cd} is the input voltage of individual module, D_{loss} represents the loss of the duty cycle due to leakage inductance of transformer, D is the duty cycle, D_{eff} represents the effective duty cycle, F_{sw} is switching frequency, L_{lk} is leakage inductance and subscript "x" indicates the module number.

Using expression (5) and (11), the output voltage can be defined as:

$$V_o = n \cdot D_{eff1} \cdot V_{cd1} + n \cdot D_{eff3} \cdot V_{cd3} \quad (12)$$

$$V_o = n \cdot D_{eff2} \cdot V_{cd2} + n \cdot D_{eff4} \cdot V_{cd4} \quad (13)$$

Adding expressions (12) and (13) is obtained:

$$2 \cdot V_o = n \cdot D_{eff1} \cdot V_{cd1} + n \cdot D_{eff2} \cdot V_{cd2} + n \cdot D_{eff3} \cdot V_{cd3} + n \cdot D_{eff4} \cdot V_{cd4} \quad (14)$$

Substituting (8) and (9) in (14).

$$2 \cdot V_o = n \cdot (V_{cd1} + V_{cd2} + V_{cd3} + V_{cd4}) \cdot D - 2 \cdot R_d \cdot I_o \quad (15)$$

Where:

$$I_o = \frac{V_o}{R_{Load}} \quad (16)$$

Finally, substituting expressions (16) in (15) and clearing V_o is obtained:

$$V_o = \frac{n \cdot (V_{cd1} + V_{cd2} + V_{cd3} + V_{cd4})}{2 \cdot \left(1 + \frac{R_d}{R_{Load}}\right)} \cdot D \quad (17)$$

From (17) it can be concluded that as the parameters n, R_d and R_{Load} are constant and the output voltage is regulated then duty cycle does not change in face of any perturbation at the individual input voltages. Since if one of the individual input voltages increases, remaining voltages decrease to satisfy the expression (1).

Since output voltage V_o is regulated and considering a load with constant power then indirectly the output currents I_{LfoT1} and I_{LfoT2} are regulated, this condition is imposed by series connection. Neglecting a mismatch of the components then $I_{Lfo1} = \frac{I_{LfoT1}}{2}$, this condition is imposed by parallel connection. Therefore from (9) it can be noticed that if the voltage V_{cd1} increases then D_{loss1} tends to decrease. Fig. 3 shows the simulation scheme in psim, which injects a perturbation in the individual input voltage V_{cd1}.

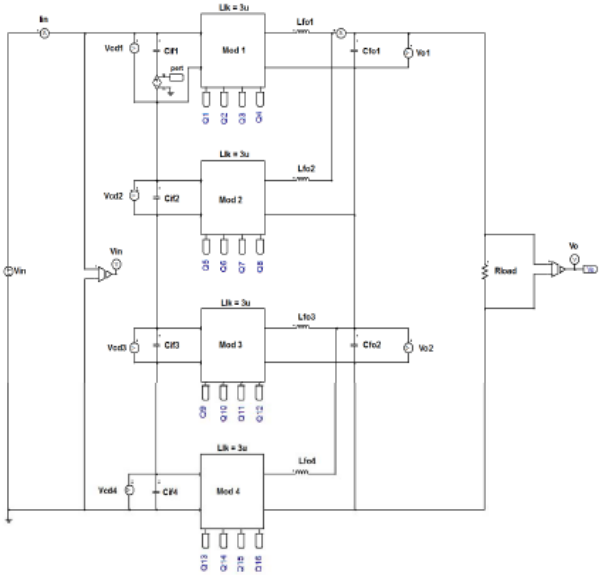

Figure 3: Psim schematic of ISOPOS converter.

The result of the simulation is in fig. 4, so it is demonstrated that duty cycle does not change and D_{loss1} decreases when there is a perturbation in V_{cd1}.

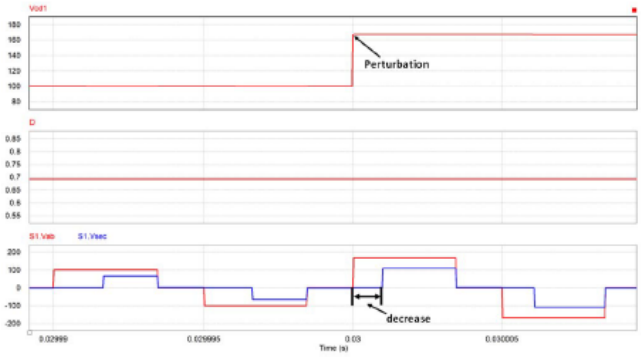

Figure 4: Simulation of the converter against a V_{cd1} perturbation.

On the other hand, at the input port, the current at the input capacitor C_{if1} in transient state is given by:

$$i_{Cif1} = i_{in} - n \cdot I_{Lfo1} \cdot D_{eff1} \tag{18}$$

Therefore, if D_{loss1} decreases then D_{eff1} increases according with expression (8).

$$D_{eff1} = D_{eff1} + \Delta d_{eff1} \tag{19}$$

The term Δd_{eff1} represents the perturbation of the effective duty cycle and D_{eff1} is the operating point. Substituting (19) in (18):

$$i_{Cif1} = I_{in} - n \cdot I_{Lfo1} \cdot D_{eff1} - n \cdot I_{Lfo1} \cdot \Delta d_{eff1} \tag{20}$$

It is demonstrated that ISOPOS converter has natural balancing mechanism since if V_{cd1} increases then i_{Cif1} decreases therefore when there is negative feedback, the system is stable, this effect can be observed in the fig. 5.

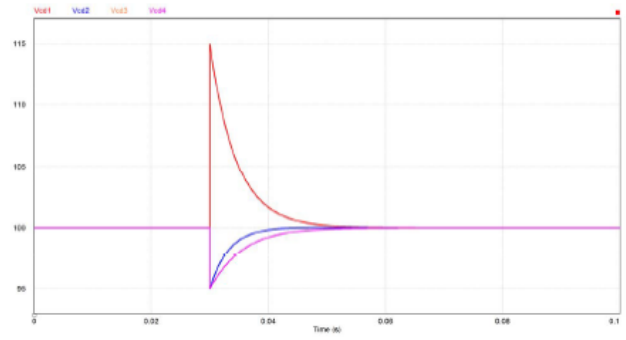

Figure 5: Simulation of ISOPOS converter when IVS is achieved.

III. Small Signal Model of ISOPOS Converter

This section proposes a brief review of the technique of injected-absorbed current method to obtain the small signal model of the ISOPOS architecture.

A. Clasical model of the injected-absorbed-current method

The technique of injected-absorbed-current method [8] allows obtaining a generalized small-signal model for most switching converters which facilitates the modeling and design process of control loops.

The following expressions constitute the circuit presented in fig. 6:

$$\hat{\imath}_m = A_i(s) \cdot \hat{d} - B_i(s) \cdot \hat{v}_o + C_i(s) \cdot \hat{v}_{in} \tag{21}$$

$$\hat{\imath}_{L_{foT}} = A_o(s) \cdot \hat{d} - B_o(s) \cdot \hat{v}_o + C_o(s) \cdot \hat{v}_{in} \tag{22}$$

$$\hat{d} = -G_{mod} \cdot Reg(s) \cdot \hat{v}_o \tag{23}$$

The terms $A_i(s)$, $B_i(s)$, $C_i(s)$, $A_o(s)$, $B_o(s)$ and $C_o(s)$ are called input and output characteristic coefficients respectively, R_L is the load resistor, $Gmod$ is the gain of modulator and $Reg(s)$ represents the transfer function of any type of controller.

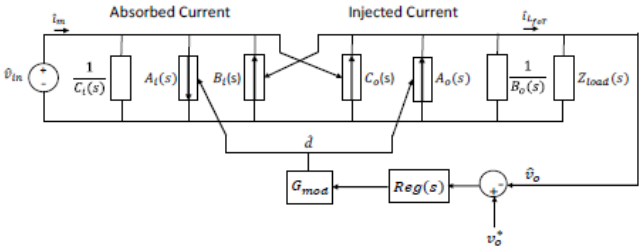

Figure 6: Representative circuit of the classical model of injected-absorbed current method.

Therefore, from the expressions (21), (22) and (23) the following transfer functions are obtained:

Control to output voltage:

$$G_{vd}(s) = \frac{A_o(s) \cdot Gmod}{B_o(s) + \frac{1}{Z_{load}(s)}} \tag{24}$$

Control to output voltage considering the input filter:

$$G_{vd\_if}(s) = \frac{A_o(s) \cdot Gmod - \frac{C_o(s) \cdot Gmod \cdot A_i(s)}{Ci(s) + \frac{1}{Zg(s)}}}{B_o(s) + \frac{1}{Z_{load}(s)} - \frac{C_o(s) \cdot B_i(s)}{Ci(s) + \frac{1}{Zg(s)}}} \tag{25}$$

In (25) the term $Z_g(s)$ represents the equivalent impedance of the input filter.

B. Small signal of PS-FBC

Taking as starting point, the small signal model of Phase-Shift full bridge converter that is shown in Fig. 7.

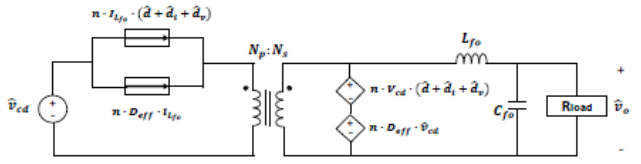

Figure 7: Small-signal of Phase-Shift Full Bridge Converter.

Where $\hat{d}_i$ represents the perturbation of duty cycle due to the change of the output filter inductor current [11].

$$\hat{d}_i = -\frac{R_d}{n \cdot V_{cd}} \cdot \hat{\imath}_{Lfo} \tag{26}$$

And, $\hat{d}_v$ represents the perturbation of duty cycle due to the change of the input voltage [11].

$$\hat{d}_v = \frac{R_d \cdot I_{Lfo}}{n \cdot V_{cd}^2} \cdot \hat{v}_{cd} \tag{27}$$

C. Small signal of PS-FBC based on ISOPOS architecture

Using the small signal of PS-FBC it can derive the small signal model of ISOPOS which is shown in fig. 8. From (26) and (27) is defined:

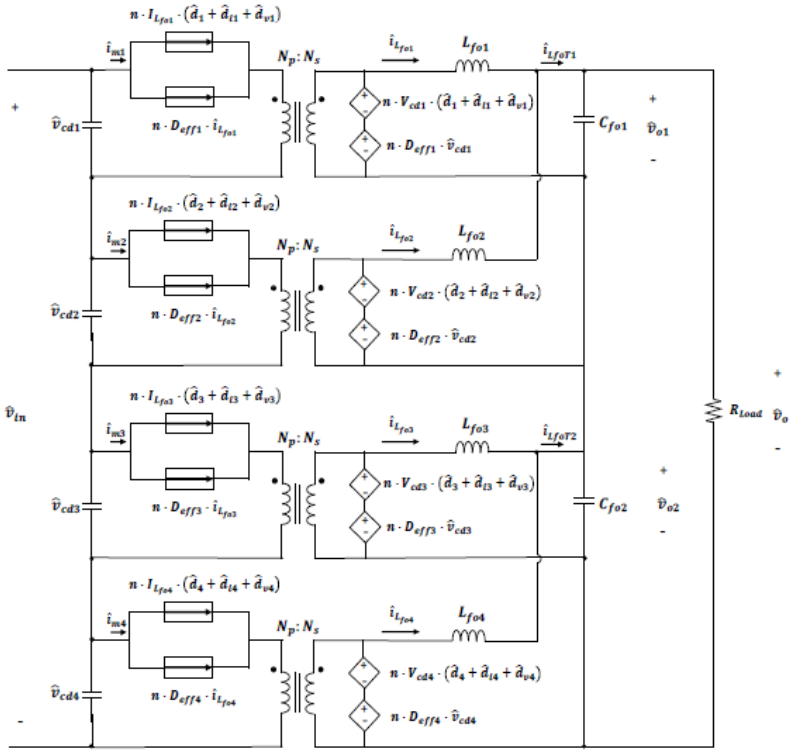

Figure 8: Small-signal model of phase-shift full bridge based on ISOPOS architecture

$$\hat{d}_{i_x} = -\frac{R_d}{n \cdot V_{cd_x}} \cdot \hat{\imath}_{Lfo_x} \tag{28}$$

$$\hat{d}_{v_x} = \frac{R_d \cdot I_{Lfo_x}}{n \cdot V_{cd_x}^2} \cdot \hat{v}_{cd_x} \tag{29}$$

Assuming that all modules have identical components (ideal case), the equations corresponding to this model are in (30) and (31) and the characteristic coefficients for the ISOPOS converter are determined. These coefficients will be used for the validation of the model.

The following equations represent the small signal model of the PS-FB based on ISOPOS architecture:

$$\hat{\imath}_{LfoT}(s) = \frac{2 \cdot n \cdot V_{cd}}{(s \cdot L_{fo} + R_d)} \cdot \hat{d} - \frac{1}{(s \cdot L_{fo} + R_d)} \cdot \hat{v}_o + \frac{X_o}{2 \cdot (s \cdot L_{fo} + R_d)} \cdot \hat{v}_{in} \tag{30}$$

$$\hat{\imath}_m(s) = \left(n \cdot I_{Lfo} + \frac{Y_o \cdot n \cdot V_{cd}}{s \cdot L_{fo} + R_d}\right) \cdot \hat{d} - \frac{Y_o}{2 \cdot (s \cdot L_{fo} + R_d)} \cdot \hat{v}_o + \left[\frac{R_d \cdot I_{Lfo}^2}{4 \cdot V_{cd}^2} + \frac{Y_o \cdot X_o}{4 \cdot (s \cdot L_{fo} + R_d)}\right] \cdot \hat{v}_{in} \tag{31}$$

$$X_o = n \cdot D_{eff} + \frac{R_d \cdot I_{Lfo}}{V_{cd}} \tag{32}$$

$$Y_o = n \cdot D_{eff} - \frac{R_d \cdot I_{Lfo}}{V_{cd}} \tag{33}$$

From (30) output characteristic coefficients are obtained:

$$A_o(s) = \frac{2 \cdot n \cdot V_{cd}}{(s \cdot L_{fo} + R_d)} \tag{34}$$

$$B_o(s) = \frac{1}{(s \cdot L_{fo} + R_d)} \tag{35}$$

$$C_o(s) = \frac{X_o}{2 \cdot (s \cdot L_{fo} + R_d)} \tag{36}$$

And from (31) input characteristic coefficients are obtained:

$$A_i(s) = n \cdot I_{Lfo} + \frac{Y_o \cdot n \cdot V_{cd}}{s \cdot L_{fo} + R_d} \tag{37}$$

$$B_i(s) = \frac{Y_o}{2 \cdot (s \cdot L_{fo} + R_d)} \tag{38}$$

$$C_i(s) = \frac{R_d \cdot I_{Lfo}^2}{4 \cdot V_{cd}^2} + \frac{Y_o \cdot X_o}{4 \cdot (s \cdot L_{fo} + R_d)} \tag{39}$$

The model is validated by simulation using the "ac_sweep" function of PSIM. Fig. 9a shows the frequency response of the control to output voltage G_{vd} transfer function obtained using the model of fig. 8.

In the case of the input filter, the term $Z_g(s)$ and $Z_{load}(s)$ is given by:

$$Z_g(s) = Z_{Lif}(s) \parallel \left(4 \cdot Z_{Cif}(s)\right) \tag{40}$$

$$Z_{load}(s) = R_{Load} \parallel \left(2 \cdot Z_{Cfo}(s)\right) \tag{41}$$

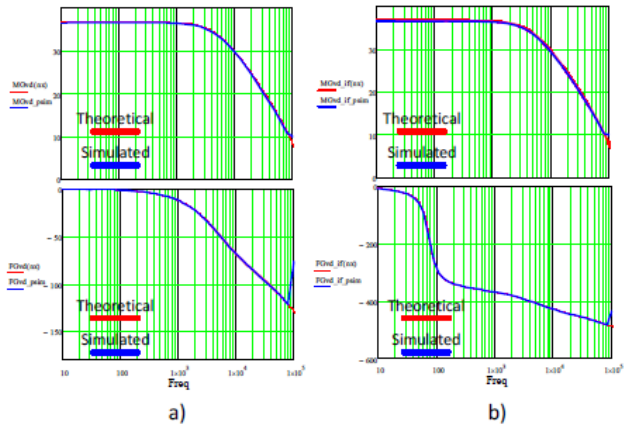

Figure 9: Frequency response of a) G_{vd} b) G_{vd_if}.

From fig. 9b it can be demonstrated that input filter has a great influence on the stability of the entire converter since the phase shows a change of 360° at the natural frequency of the input filter.

To analyze the interaction of the input filter with the system there are different criteria that analyze the stability of the system, for this reason in [12] a review of these criteria is shown.

III. Controller Design

To design the control loop of ISOPOS architecture, it will be used the transfer function G_{vd_if} that includes the effect of the input filter to ensure the stability of the system since it has a great influence on the phase of control to output voltage transfer function. The main parameters of the ISOPOS converter are in table I.

Parameter	Value
Input voltage	400 V
Output voltage	48 V
Switching Frequency	100 kHz
Output filter inductance	$36\ \mu H$
Transformer turns ratio	0.6667
Output filter Capacitor	$4\ 7\ \mu F$
Input filter inductance	$38\ mH$
Input filter Capacitor	$470\ \mu H$
Leakage inductance	$3\ \mu H$
Load resistor	$0.s8\ n$

Table I: Specifications for simulation of ISOPOS converter

As a design tool, SmartCtrl software is used, since by inserting the transfer function in the equation editor a solution map with possible regulator parameters is generated. In this case a PI controller is selected since it is the most used in the industrial sector. The natural frequency of the input filter is approximately 75Hz, the selected crossover frequency is 25 Hz since it is under the frequency range where the input filter has influence. This strategy is generally applied to the buck converter with input filter [13]. Frequency response of open loop system is in fig. 10.

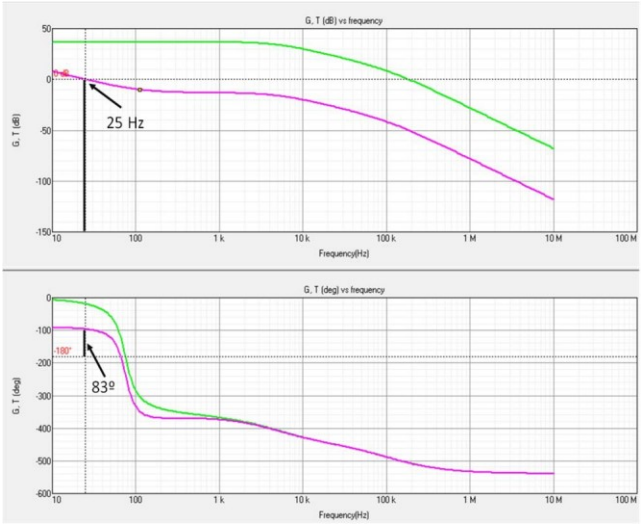

Figure 10: Frequency response of G_{vd_if} in SmartCtrl.

To verify that the technique applied to the traditional buck converter ensures stability in ISOPOS architecture, the simulation of the schematic of fig. 11 is performed.

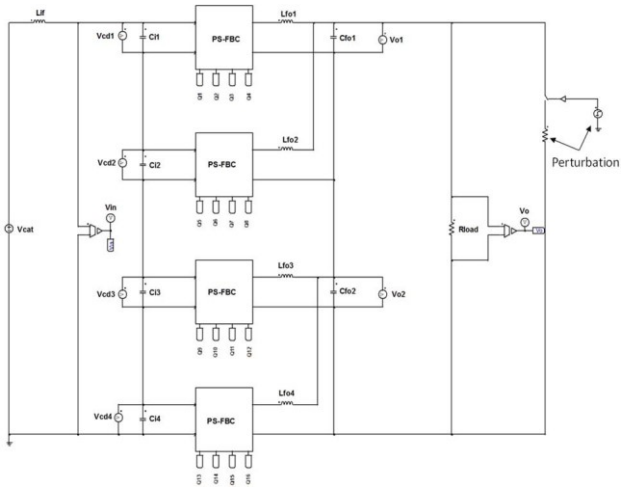

Figure 11: Psim scheme of ISOPOS converter with load perturbation.

Fig. 12 shows a step response of the control loop when a load perturbation is applied. The response of the controller is slow in order to stabilize the input voltage. To improve the response of the controller it is necessary to try to implement other control techniques.

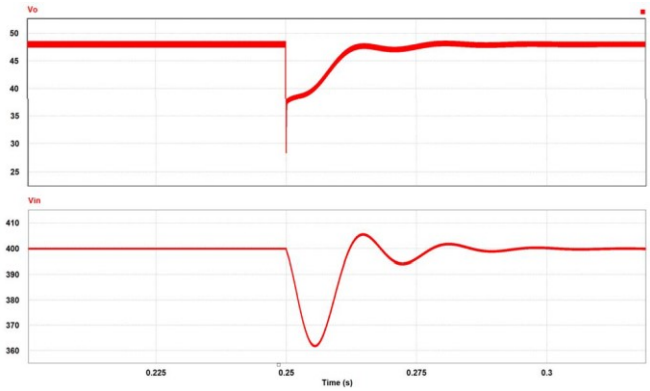

Figure 12: Transient response of ISOPOS converter with input filter.

IV. Conclusions

In this paper, a new architecture has proposed for railway applications or high power-high voltage converters in which the high voltage intermediate DC bus is still required. It has been demonstrated the natural balancing mechanism of the proposed ISOPOS architecture under common-duty-cycle operation. The complete small signal model including G_{vd} and G_{vd_if} have been developed.

Furthermore, it is demonstrated that the same criteria and techniques used in traditional converters to ensure stability can be applied to the proposed architecture when considering an input filter.

Acknowledgment

This work is partially supported by the Ministry of Economy and Competitiveness and FEDER funds through the research project "Storage and Energy Management for Hybrid Electric Vehicles based on Fuel Cell, Battery and

Supercapacitors" - ELECTRICAR-AG- (DPI2014-53685-C2-1-R).

This work is partially supported by the Ministry of Economy and Competitiveness, the State Research Agency and FEDER funds through the research projects "Modelling and control strategies for the stabilization of the interconnection of power electronic converters" - CONEXPOT-2- (DPI2017-84572-C2-2-R) (AEI/FEDER, UE).

REFERENCES

[1] J. Shi, J. Luo, X. He, "Common-Duty-Ratio Control of Input-Series Output-Parallel Connected Phase-shift Full-Bridge DC-DC Converter Modules", *lEEE Transactions on Power Electronics* 2011, vol 26, no 11.

[2] P. Zumel, E. Ona, C. Fernandez, M Sanz, A. Lazaro, A. Barrado, "Analysis and modeling of a modular ISOP Full Bridge based converter with input filter", *lEEE Applied Power Electronics Conference and Exposition (APEC),* 2016.

[3] Y. Lian G. Adam, D. Holliday, S. Finney, "Active Power Sharing in Input-Series-Input-Parallel Output-Series Connected DC/DC Converters", *lEEE Applied Power Electronics Conference and Exposition (APEC),* 2015.

[4] L. Wang, X. He, "Input-Series and Output-Parallel Connection Modular DC-DC Converters with Interleaved Constant Duty Cycle Control Strategy" *The 33rd Annual Conference of the lEEE lndustrials Electronics Society (lECON),* 2007.

[5] Y. Lian, D. Holliday, S. Finney, "Dual-Active Bridge Converter with Input-Series-Input-Parallel Output-Series Connection", *8th lET lnternational Conference on Power Electronics, Machines and drives,* 2016.

[6] F. Schmid, C. J. Gooman, "Electric Railway Systems in Common Use", 4th Institution of Engineering and Technology Professional Development Course on Railway Electrification Infrastrucutre and Systems, 2009, pp. 6-20, ISBN: 9781849191333, ISSN: 0537-9989.

[7] R. Khanna, "Various control methods for DC-DC buck converter," in *Power lndia Conference, 2012 lEEE Fifth*, 2012, pp. 1-4.

[8] A. Kislovski, R. Redl, N. Sokal, "Dynamic Analysis of Switching-Mode DC/DC Converters", Springer Science & Business Media, 2012.

[9] X. Ruan, W. Chen, L. Cheng, K.T. Chi, H. Yan and T. Zhang, "Control strategy for input-series-output-parallel converters," IEEE *Trans.lnd.Electron.*, vol. 56, no. 4, pp. 1174-1185 2009.

[10] J. Sabate, V. Vlatkovic, R. Ridley, F. Lee and B. Cho, "Design considerations for high-voltage high-power full-bridge zero-voltage-switched PWM converter," in *Proc. lEEE APEC*, 1990, pp. 275-284

[11] V. Vlatkovic, J.A. Sabate, R.B. Ridley, F.C. Lee and B.H. Cho, "Small-signal analysis of the phase-shifted PWM converter", IEEE Transactions on power electronics, vol. 7, no. 1, pp. 128-135 1992

[12] A. Riccobono, E. Santi, "Comprehensive Review of Stability Criteria for DC Power Distribution Systems", *lEEE Transactions on lndustry Applications* 2014, vol 50, no 5.

[13] R. W. Erickson, D. Maksimovic, iccobono, "Fundamental of Power Electronics", *Springer Sience & Bussiness Media,* 2007.