Linearization of Time-encoded ADCs Architectures for Smart MEMS Sensors in Low Power CMOS Technology

by

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Published and submitted content

- R. Garvi, J. Granizo, E. Gutierrez, V. Medina, A. Wiesbauer and L. Hernandez, "A VCO-ADC linearized by a capacitive frequency-to-current converter," *IEEE Transactions on Circuits and Systems II: Express Briefs*.

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  The material from this source included in this thesis is not singled out with typographic means and references.

- C. Perez et al., "A VCO-based ADC with direct connection to a microphone MEMS, 80dB peak SNDR and 438μW power consumption," *IEEE Sensors Journal*.

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Other research contributions

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Abstract

In the last few years, the development of mobile technologies and machine learning applications has increased the demand of MEMS-based digital microphones. Mobile devices have several microphones enabling noise canceling, acoustic beamforming and speech recognition. With the development of machine learning applications the interest to integrate sensors with neural networks has increased. This has driven the interest to develop digital microphones in nanometer CMOS nodes where the microphone analog-front end and digital processing, potentially including neural networks, is integrated on the same chip.

Traditionally, analog-to-digital converters (ADCs) in digital microphones have been implemented using high order Sigma-Delta modulators. The most common technique to implement these high order Sigma-Selta modulators is switched-capacitor CMOS circuits. Recently, to reduce power consumption and make them more suitable for tasks that require always-on operation, such as keyword recognition, switched-capacitor circuits have been improved using inverter-based operational amplifier integrators. Alternatively, switched-capacitor based Sigma-Delta modulators have been replaced by continuous time Sigma-Delta converters. Nevertheless, in both implementations the input signal is voltage encoded across the modulator, making the integration in smaller CMOS nodes more challenging due to the reduced voltage supply.

An alternative technique consists on encoding the input signal on time (or frequency) instead of voltage. This is what time-encoded converters do. Lately, time-encoding converters have gained popularity as they are more suitable to nanometer CMOS nodes than Sigma-Delta converters. Among the ones that have drawn more interest we find voltage-controlled oscillator based ADCs (VCO-ADCs). VCO-ADCs can be implemented using CMOS inverter based ring oscillators (RO) and digital circuitry. They also show noise-shaping properties. This makes them a very interesting alternative for implementation of ADCs in nanometer CMOS nodes. Nevertheless, two main circuit impairments are present in VCO-ADCs, and both come from the oscillator non-idealities. The first of them is the oscillator phase noise, that reduces the resolution of the ADC. The second is the non-linear tuning curve of the oscillator, that results in harmonic distortion at medium to high input amplitudes.

In this thesis we analyze the use of time encoding ADCs for MEMS microphones with special focus on ring oscillator based ADCs (RO-ADCs). Firstly, we study the use of a dual-slope based SAR noise shaped quantizer (SAR-NSQ) in sigma-delta loops. This quantizer adds and extra level of noise-shaping to the

modulator, improving the resolution. The quantizer is explained, and equations for the noise transfer function (NTF) of a third order sigma-delta using a second order filter and the NSQ are presented.

Secondly, we move our attention to the topic of RO-ADCs. We present a high dynamic range MEMS microphone 130nm CMOS chip based on an open-loop VCO-ADC. This dissertation shows the implementation of the analog front-end that includes the oscillator and the MEMS interface, with a focus on achieving low power consumption with low noise and a high dynamic range. The digital circuitry is left to be explained by the coauthor of the chip in his dissertation. The chip achieves a 80dBA peak SNDR and 108dB dynamic range with a THD of 1.5% at 128 dBSPL with a power consumption of $438\mu W$.

After that, we analyze the use of a frequency-dependent-resistor (FDR) to implement an unsampled feedback loop around the oscillator. The objective is to reduce distortion. Additionally phase noise mitigation is achieved. A first topology including an operational amplifier to increase the loop gain is analyzed. The design is silicon proven in a 130 nm CMOS chip that achieves a 84 dBA peak SNDR with an analog power consumption of $600\mu W$. A second topology without the operational amplifier is also analyzed. Two chips are designed with this topology. The first chip in 130 nm CMOS is a full VCO-ADC including the frequency-to-digital converter (F2D). This chip achieves a peak SNDR of 76.6 dBA with a power consumption of $482\mu W$. The second chip includes only the oscillator and is implemented in 55nm CMOS. The peak SNDR is 78.15 dBA and the analog power consumption is $153\mu W$.

To finish this thesis, two circuits that use an FDR with a ring oscillator are presented. The first is a capacity-to-digital converter (CDC). The second is a filter made with an FDR and an oscillator intended for voice activity detection tasks (VAD).

Resumen

En los últimos años, el desarrollo de las tecnologías móviles y las aplicaciones de machine-learning han aumentado la demanda de micrófonos digitales basados en MEMS. Los dipositivos móviles tienen varios micrófonos que permiten la cancelación de ruido, el beamforming o conformación de haces y el reconocimiento de voz. Con el desarrollo de aplicaciones de aprendizaje automático, el interés por integrar sensores con redes neuronales ha aumentado. Esto ha impulsado el interés por desarrollar micrófonos digitales en nodos CMOS nanométricos donde el front-end analógico y el procesamiento digital del micrófono, que puede incluir redes neuronales, está integrado en el mismo chip.

Tradicionalmente, los convertidores analógicos-digitales (ADC) en micrófonos digitales han sido implementados utilizando moduladores Sigma-Delta de orden elevado. La técnica más común para implementar estos moduladores Sigma-Delta es el uso de circuitos CMOS de capacidades conmutadas. Recientemente, para reducir el consumo de potencia y hacerlos más adecuados para las tareas que requieren una operación continua, como el reconocimiento de palabras clave, los convertidores Sigma-Delta de capacidades conmutadas has sido mejorados con el uso de integradores implementados con amplificadores operacionales basados en inversores CMOS. Alternativamente, los Sigma-Delta de capacidades conmutadas han sido reemplazados por moduladores en tiempo continuo. No obstante, en ambas implementaciones, la señal de entrada es codificada en voltaje durante el proceso de conversión, lo que hace que la integración en nodos CMOS más pequeños sea complicada debido a la menor tensión de alimentación.

Una técnica alternativa consiste en codificar la señal de entrada en tiempo (o frecuencia) en lugar de tensión. Esto es lo que hacen los convertidores de codificación temporal. Recientemente, los convertidores de codificación temporal han ganado popularidad ya que son más adecuados para nodos CMOS nanométricos que los convertidores Sigma-Delta. Entre los que más interés han despertado encontramos los ADCs basados en osciladores controlados por tensión (VCO-ADC). Los VCO-ADC se pueden implementar usando osciladores en anillo (RO) implementados con inversores CMOS y circuitos digitales. Esta familia de convertidores también tiene conformado de ruido. Esto los convierte en una alternativa muy interesante para la implementación de convertidores en nodos CMOS nanométricos. Sin embargo, dos problemas principales están presentes en este tipo de ADCs debidos ambos a las no idealidades del oscilador. El primero de los problemas es la presencia de ruido de fase en el oscilador, lo que reduce la

resolución del ADC. El segundo es la curva de conversion voltaje-frecuencia no lineal del oscilador, lo que causa distorsión a amplitudes medias y altas.

En esta tesis analizamos el uso de ADCs de codificación temporal para micrófonos MEMS, con especial interés en ADCS basados en osciladores de anillo (RO-ADC). En primer lugar, estudiamos el uso de un cuantificador SAR con conformado de ruido (SAR-NSQ) en moduladores Sigma-Delta. Este cuantificador agrega un orden adicional de conformado de ruido al modulador, mejorando la resolución. En este documento se explica el cuantificador y obtienen las ecuaciones para la función de transferencia de ruido (NTF) de un sigma-delta de tercer orden usando un filtro de segundo orden y el NSQ.

En segundo lugar, dirigimos nuestra atención al tema de los RO-ADC. Presentamos el chip de un micrófono MEMS de alto rango dinámico en CMOS de 130 nm basado en un VCO-ADC de bucle abierto. En esta tesis se explica la implementación del front-end analógico que incluye el oscilador y la interfaz con el MEMS. Esta implementación se ha llevado a cabo con el objetivo de lograr un bajo consumo de potencia, un bajo nivel de ruido y un alto rango dinámico. La descripción del back-end digital se deja para la tesis del couator del chip. La SNDR de pico del chip es de 80dBA y el rango dinámico de 108dB con una THD de $1,5\%$ a 128 dBSPL y un consumo de potencia de $438\mu W$.

Finalmente, se analiza el uso de una resistencia dependiente de frecuencia (FDR) para implementar un bucle de realimentación no muestreado alrededor del oscilador. El objetivo es reducir la distorsión. Además, también se logra la mitigación del ruido de fase del oscilador. Se analyza una primera topologia de realimentación incluyendo un amplificador operacional para incrementar la ganancia de bucle. Este diseño se prueba en silicio en un chip CMOS de 130nm que logra un pico de SNDR de 84 dBA con un consumo de potencia de $600\mu W$ en la parte analógica. Seguidamente, se analiza una segunda topología sin el amplificador operacional. Se fabrican y miden dos chips diseñados con esta topologia. El primero de ellos en CMOS de 130 nm es un VCO-ADC completo que incluye el convertidor de frecuencia a digital (F2D). Este chip alcanza un pico SNDR de 76,6 dBA con un consumo de potencia de $482\mu W$. El segundo incluye solo el oscilador y está implementado en CMOS de 55nm. El pico SNDR es 78.15 dBA y el el consumo de potencia analógica es de $153\mu W$.

Para cerrar esta tesis, se presentan dos circuitos que usan la FDR con un oscilador en anillo. El primero es un convertidor de capacidad a digital (CDC). El segundo es un filtro realizado con una FDR y un oscilador, enfocado a tareas de detección de voz (VAD).

Contents

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List of Abbreviations

ADC	Analog-to-digital converter
AOP	Acoustic overload point
CDC	Capacitance-to-digital converter
CCO	Current-controlled oscillator
CMOS	Complementary metal oxide semiconductor
DAC	Digital-to-analog converter
DBP	Dual backplate
DR	Dynamic range
ENOB	Effective number of bits
F2D	Frequency-to-digital converter
FDR	Frequency dependent resistor
FM	Frequency modulated
HO	High ohmic resistor
IRPN	Input referred phase noise
LSB	Least significant bit
LS	Level shifter
LDO	Low-dropout regulator
MASH	Multi-stage noise shaping
MEMS	Microelectromechanical system
MSB	Most significant bit
NMOS	Negative channel metal oxide semiconductor transistor
NSQ	Noise shaping quantizer
NTF	Noise transfer function
OSR	Oversampling ratio
PDM	Pulse density modulation
PFM	Pulse frequency modulated
PGA	Programmable gain amplifier
PMOS	Positive channel metal oxide semiconductor transistor
PSD	Power spectral density
PSRR	Power supply rejection ratio
PSS	Periodic steady state
PVT	Process-voltage-temperature
RO	Ring oscillator
SA	Sense amplifier
SAR	Successive approximation register

SBP	Single backplate
SF	Source follower
SNDR	Signal-to-noise and distortion ratio
SNR	Signal-to-noise ratio
SPI	Serial peripheral interface
SQNR	Signal-to-quantization noise ratio
STF	Signal transfer function
VAD	Voice activity detection
VCO	Voltage-controlled oscillator
VUI	Voice user interface

Part I

Introduction

Chapter 1

Capacitive MEMS sensors

1.1 Importance of MEMS microphones in the mobile device ecosystem

In "2001: A Space Odyssey" the crew of the spaceship Discovery One casually chat with the ship's computer, HAL 9000. Today we can put ourselves in the shoes of the Discovery's crew and ask Alexa to play a song or turn on the lights in the comfort of our own home. The advances in artificial intelligence brought by the machine learning revolution have made many things that seemed science fiction a few years ago part of our daily routine. The trend toward human-machine communication has pushed the development of Voice User Interfaces (VUI). But we could not handle over our privacy to the big corporations with artificial intelligence algorithms only. Despite all the advancements in digital technology, the world and our lives remain stubbornly analog. The sound coming out of our mouth is not a digital string of zeros and ones, but a series of analog pressure waves. If we want Alexa to play a song or change the TV channel, we need first to transform these analog signals into a digital code. This is why we need a digital microphone, that can translate the sound pressure waves into a digital signal, ready to be digitally processed, analyzed and stored.

But digital microphones have other uses aside from sparing us of the effort of using buttons. With the mobile devices industry reaching maturity companies are looking for new ways to increase sales. High quality audio, smart assistants, wireless headphones, all of them require the use of digital microphones. These digital microphones are combined with audio processing functions such as blind source separation, beamforming, etc, to implement active noise cancellation [1]. Among other technologies that are being developed we find 360º audio recording and transparent hearing modes. The first of these allows to record immersive audio experiences using very low noise floor microphones, while the second help us in hearing things such as an approaching car or someone calling our name while using earbuds. This requires microphones with a low noise floor that can be placed in arrays comprising from 2 up to 32 microphones. Also low power consumption is required to install those microphones in wireless battery-powered devices such as True Wireless Stereo (TWS) earbuds.

But how do we make a digital microphone? In our task to convert a sound wave into digital we need to perform several actions using different devices. Firstly we need a transducer, a device that converts a physical magnitude (measurand) like the sound, into an analog electrical signal. One of the most used transducers in state-of-the-art digital microphones are MEMS capacitive sensors [2]. Then we need to convert this analog electrical signal into a digital signal. For that we will have to use an analog-to-digital converter (ADC). The first step in this process involves adapting the signal coming out the transducer. This process of adaptation may include things like transforming a current into a voltage, amplifying the signal or establishing the adequate impedance to guarantee the correct functioning of the transducer. After that is done, the signal, still in analog form, has to be sampled. The typical way to do this task is to use a sample and hold circuit (S/H). After the sample and hold, our signal is now a discrete signal. This means that unlike an analog signal that has a value for every time instant, our signal now only has values for some time instants, i.e, we have taken samples of the analog signal with a constant time interval, the sampling period, T_S. The inverse of this sampling period is the sampling frequency, f_S, and is equal to the number of samples we have taken per second.

The next station in our trip from the analog world to the digital world is the quantization of the discrete signal. Although the discrete signal exist only at certain time instants, its value (for instance its voltage) can still take as many decimals as needed, i.e, it has and infinite resolution. This is not exactly true, as any real world signal have noise, coming from both the environment and the electrical devices. But let's not concern ourselves with this just yet. The need to quantize the discrete signal comes from the fact that any digital word has a finite number of bits, and thus a finite number of combinations of zeros and ones, which means that we can only represent a limited number of values. Thus the process of quantization consist on taking our value with an infinite amount of decimals, and approximate it to the closest value that can be represented with a certain number of bits digital word. After we have done this, we finally have a digital signal, that is discrete and quantized. The number of bits of the digital words composing the digital signal will be the number of bits of our ADC.

With this we may consider our trip from the analog world to the digital world finished. There is one more step that may be necessary. As we usually convert an analog magnitude into digital, so we can digitally process, store and transmit that magnitude, we still need to deal with interfacing our signal with the rest of the digital world. The last part thus consist on sending out our digital signal using a standard communications protocol. With this last step the trip from the analog world to the digital world reaches its terminal station and our digital microphone is finished. Let's take a look now to each one of the devices conforming our digital microphone with a bit more detail.

1.2 Summary of microphone technology. Structure of a MEMS microphone.

The first device of a digital microphone is the transducer. As mentioned before, this device will convert the different pressure waves conforming the sound into an electrical magnitude. Although the whole digital microphone contains more parts as it has already been stated, we will refer to this transducer as microphone for now on, for the sake of simplicity.

Microphones can be implemented using several technologies, such as carbon microphones [3], [4], condenser microphones [4], [5] dynamic microphones, electret microphones [6], fiber-optic microphones [7], [8], piezoelectric microphones and MEMS microphones. Carbon microphones were very popular in the early days of electronics due to its low cost and robustness. They were used in telephone systems until the 1980s. They have a limited frequency response and bad audio quality. These microphones are build placing carbon granules between two conducing plates. A voltage is then applied between the plates, which causes a current to flow trough the carbon granules. When the sound waves incise on the plate that serves a diaphragm, this compresses the carbon granules, changing the resistance between the plates. Nowadays carbon microphones have been discontinued.

Condenser microphones, also known as capacitor microphones were invented in the early 20th century. Their name comes from the fact that capacitors used to be called condensers. They are constructed with two parallel conductive plates separated by a dielectric material forming a capacitor. One of the plates serves as the diaphragm while the other is fixed. The audio waves change the distance between the plates, which in turn changes the capacitance. Electret and MEMS microphones are based in the same principle. In electret microphones, the capacitor is made using and electret material as the dielectric. An electret material [9] is a type of dielectric that can be permanently charged. This eliminates the need to apply an external bias charge to the capacitor. The acronym MEMS stands for Microelectromechanical systems. MEMS technology allows to build sensitive to pressure capacitors directly into a silicon wafer, which greatly reduces its size and allows for integration in a single package with an analog font-end and analog-to-digital (ADC) converter.

Dynamic microphones also known as moving-coil microphones use the phenomena of electromagnetic induction to convert sound into an electrical magnitude. A mobile coil attached to a diaphragm is placed inside a magnetic field. In this configuration, the sound pressure waves move the coil inside the magnetic field, causing a current flow in the coil. In the case of optical fiber-optic microphones, the movement of a reflective diaphragm is measured by sensing the intensity of an incident light. Several methods are used such as interferometric techniques or diffractive lens. Finally, piezoelectric microphones made use of a piezoelectric crystal to convert acoustic waves into an electrical magnitude.

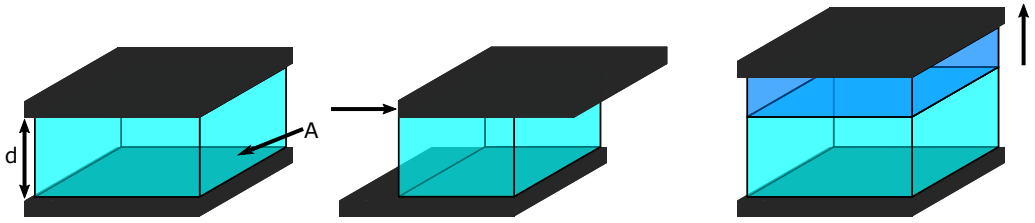

FIGURE 1.1: Parallel plates capacitor

In these microphones, the piezoelectrical crystal is compressed by the acoustic waves, wich makes it to generate a voltage proportional to the pressure.

1.2.1 Operating principle of capacitive microphones

In this section we will focus on MEMS microphones. MEMS microphones are interesting as transducers for digital microphones due to its small size, and capability to be placed in a single package together with the readout circuits as was mentioned before. MEMS microphones are based in the same principle that condenser microphones. They convert the audio signal into an electrical signal by means of a variable capacitance. The capacitance (C) of the parallel plate capacitor shown in Fig 1.1 is given by

$$C = \frac{\epsilon_r \epsilon_0 A}{d} \tag{1.1}$$

where ϵ_r is the relative permittivity of the dielectric between the plates, ϵ_0 is the permittivity of space and equal to 8.854 pF/m, A is the overlapping area of the plates and d is the distance between the plates. From (1.1) it can be seen that either by changing the the overlapping area or the distance between the plates we can change the capacitor value. If we change the overlapping area between the plates, by fixing one of the plates and displacing the other along the horizontal axis, we get a linear relationship between the value of the capacitance and the value of the measurand, or audio signal in the case of a microphone. Alternatively, we can fix one of the plates while the other plate will move in the vertical axis in response to the measurand. In this case we see from 1.1 that the capacitance varies inversely proportional to the distance between the plates.

Differential configurations are a way to improve sensitivity and reduce distortion. A differential capacitor sensor can be built by placing a third metal plate between the two original plates. In this configuration the two outermost plates are fixed, while the third metal plate placed in between is mobile, forming two

variable capacitors. When the central plate moves, one of the capacitors is increased, while the other is decreased depending on the direction of the movement following:

$$C_p = \frac{\epsilon_r \epsilon_0 A}{d_p + \Delta d} \tag{1.2}$$

$$C_n = \frac{\epsilon_r \epsilon_0 A}{d_n - \Delta d} \tag{1.3}$$

Capacitive microphones usually use the configuration were the movable plate displaces along the vertical axis in response to changes in the measurand. This plate serves as the diaphragm. As audio signals consist on changes in the air pressure, a reference pressure is needed for its measurement. The diaphragm or movable plate has to be placed between a reference pressure chamber and a hole connecting to the the outside, from were the sound pressure waves come into the microphone. This way the diaphragm displaces depending on the difference of pressures, and the capacitance varies inversely proportional to this difference. The direction of this variation depends on the position of the fixed plate of the capacitor (inside the reference chamber or in the hole connecting to the outside) and whether the external pressure is bigger or smaller than the reference pressure. If two fixed plates are placed, one in the reference chamber and other in the hole, then a differential sensor is constructed.

1.2.2 Fabrication of MEMS microphones

All the above discussion is valid for any capacitive sensor. The difference of MEMS capacitive microphones versus conventional condenser or electret microphones is its miniaturized size, as MEMS microphones are directly etched over a silicon wafer using semiconductor fabrication techniques. The development of these techniques has allowed to build micrometer devices with movable parts. Two types of MEMS microphones are the more commonly used, single backplate (SBP) and dual backplate (DBP) MEMS, that corresponds to the single ended and differential configurations described previously.

Figure 1.2 a) shows the cross section of a SBP MEMS microphone. The structure contains a hole, a membrane serving as the diaphragm and a backplate. The backplate is usually perforated to allow the air flow. By placing another backplate in the other side of the hole a DBP MEMS is constructed (1.2 b)). In both configurations the backplates are perforated to allow the flow of air. Also to reject slow pressure variations caused by meteorological changes or differences of altitude, the membrane is perforated with very small holes. This holes allow for the pressure of the reference chamber to balance with the external pressure, but only over a long time. This way the reference chamber pressure can not change with the fast pressure changes caused by audio signals, which allows the microphone to operate properly.

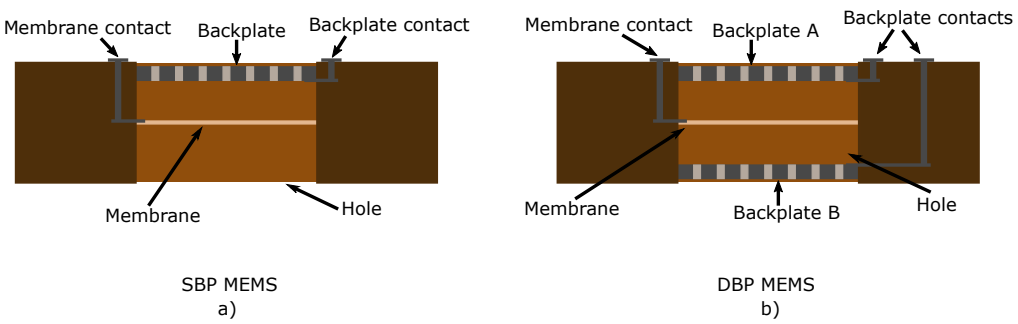

FIGURE 1.2: Cross section of a) a single backplate MEMS (SBP) and b) a dual backplate MEMS (DBP)

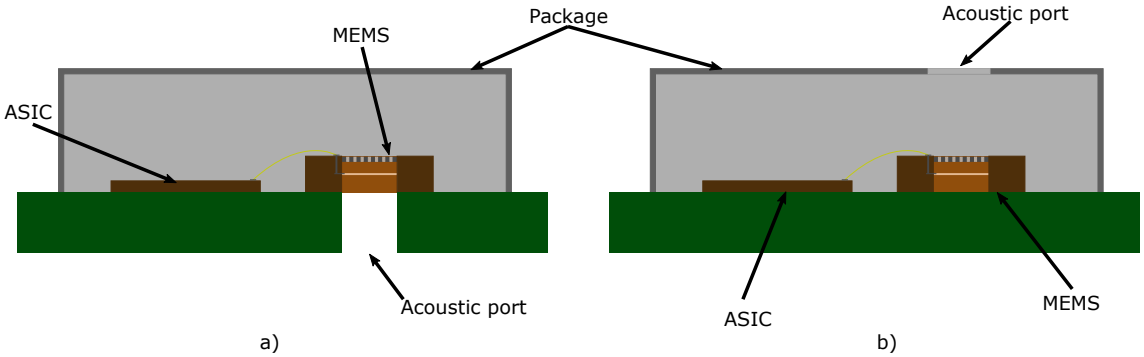

FIGURE 1.3: Cross section of a MEMS package and ASIC with a) PCB acoustic port b) package acoustic port

MEMS microphones are usually composed of a chip containing the MEMS capacitor and a second chip containing the readout circuit. Those two chip are placed over a PCB board that serves as a substrate and bonded together using gold wires. This pair of chips is then placed in the same package. Aside from protecting the chips and offering an interface to connect with other devices over a PCB board, the package also serves an important acoustic function. The acoustic properties of the package are mostly determined by the volume of the package and the position of the acoustic port. Figure 1.3 shows two configurations of acoustic packages. In Fig 1.3 a) the acoustic port is drilled in the PCB board, and the volume of the package serves as the reference pressure chamber. On the other hand, the configuration shown in Fig 1.3 b) has the acoustic port placed in the package itself. In this case the reference chamber is the volume between the membrane and the PCB substrate.

An electrical model of a SBP MEMS is shown in Fig 1.4 a). Capacitor C_{MEMS} is the variable capacitor formed by the membrane and the backplate. Both the backplate and the membrane are made of poly silicon and their resistance is represented as R_{bp} and R_m respectively. Another resistance R_{leak} is placed between the membrane and the backplate. It represents the leakage resistance between

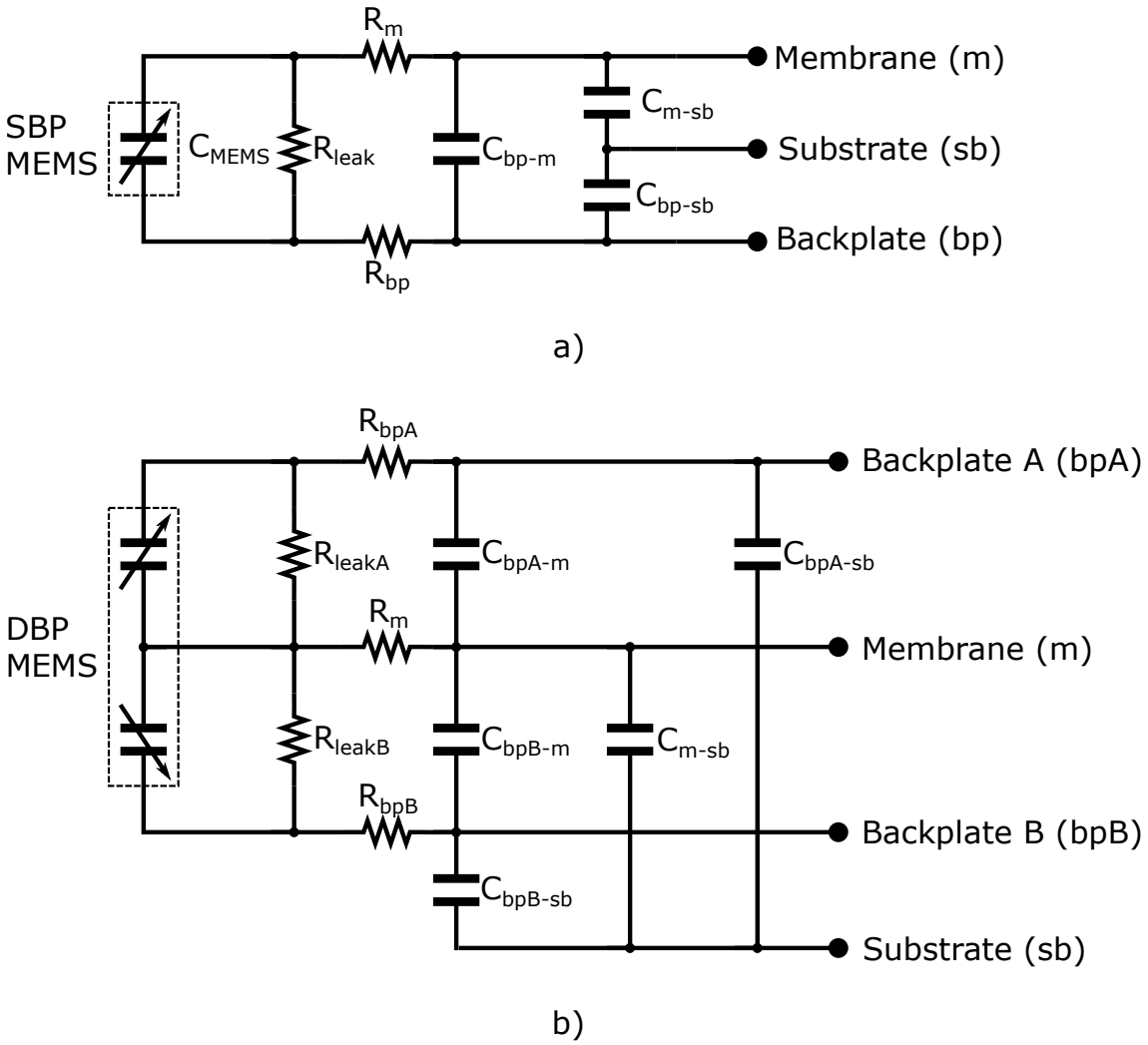

FIGURE 1.4: Electrical model of a) a SBP MEMS b) a DBP MEMS

both terminals and is in the order of hundreds of gigaohms. Three parasitic capacitors exits, one between the backplate and the membrane terminals, C_{bp-m}, another between the membrane and the substrate, C_{m-sb}, and a last one between the backplate and the substrate, C_{bp-sb}.

For the DBP the electric model is shown in Fig 1.4 b). Now the MEMS have two backplates, backplate A (bpA) and backplate B (bpB). The two backplates together with the membrane forms the two variable capacitors that conforms the sensor. R_{bpA} and R_{bpB} are the resistance of backplate A and B respectively while R_m is the same resistance of the membrane that in Fig 1.4 a). Instead of one leakage resistance from the backplate to the membrane, now two leakage resistances are present, R_{leakA} which is the leakage resistance from the backplate A to the membrane and R_{leakB} that is the one from the backplate B to the membrane. Finally the number of parasitic capacitors are increased from three to

five. The parasitic capacitor from the backplates to the membrane are C_{bpA-m} and C_{bpA-m}, corresponding to the ones formed from the bpA to the membrane and from bpB to the membrane respectively. Each of the three terminals, bpA, bpB and membrane exhibits a parasitic capacitance to the substrate. These are named C_{bpA-sb}, corresponding to the capacitance between the backplate A and the substrate, C_{bpB-sb} corresponding to the one from backplate B to the substrate, and C_{m-sb} corresponding from the one from the membrane to the substrate.

1.3 Prior art readout circuits: Switched capacitor ADCs, PGA+SAR ADCs, VCO-ADCs, Industry standard digital interfaces

After the transducer a readout circuit is needed. This readout circuit must adapt the output electrical signal from the transducer to be used in the following stages. Two types of readout circuits can be distinguished depending on whether its output is in the analog domain or the digital domain. According to these two types, and referring to microphones specifically, we have two types of microphones, analog microphones and digital microphones. In both types of microphones the transducer is the same, what changes is the readout circuit. Analog microphones provide an output voltage or current (usually a voltage) in the analog domain. For this their readout circuit must perform two main tasks. The first task is to eliminate any loading effect in the transducer caused by the readout circuit, proportioning the right input impedance to the readout circuit. The second task is to adapt the electrical signal for the needs of any subsequent circuit. Doing this implies amplifying, filtering the signal and transforming either from current-to-voltage or from voltage-to-current. It is also necessary that the readout circuit has the adequate output impedance. This way the output of the microphone would comply with any of the industrial standards, making it usable with other electronic components to make a whole system.

Digital microphones must have a readout circuit performing the aforementioned tasks, but in addition they must convert the analog signal coming from the transducer into a digital word with a certain number of bits. As it has been already discussed, this involves the use of an ADC that must perform two interconnected operations, sample and hold and quantize the analog signal. Several architectures can be used to implement an ADC. The more straight forward way to implement an ADC consist on comparing the input voltage signal with several reference voltages using a series of comparators. When the signal is above a certain reference voltage the output of the comparator corresponding to that reference voltage and all of those with a smaller reference voltage are set to one, while the outputs of the comparators connected with a bigger reference voltage are set to zero. The output of this array of comparators is a digital word with a

number of bits equal to the number of comparators coded in thermometric code. This is what is called an uniform quantizer.

Thermometric code is a coding scheme to digitally represent a magnitude, where the number of possible combinations, i.e. values that can be coded, is equal to the number of bits plus one. This coding scheme is named thermometric due to its similarity with a thermometer where the mercury fills the tube until a certain mark depending on temperature. As in a thermometer, the ones fill the digital word depending on the value that is being coded. This coding scheme does not use all the possible combinations of zeros and ones, and thus uses more bits than necessary to represent values with a certain resolution. Binary code uses all the possible combinations that can be found in a digital word with a certain number of bits, allowing to represent a value with a certain resolution using less bits than with thermometer code. Because of this, the thermometer code coming out the comparator array is decoded to binary code. The number of bits of this binary code is equal to $ceil(log_2(N+1))$, where N is the number of bits of the corresponding thermometric code. The circuit described above is known as a flash-ADC.

There are many other different architectures used to implement ADCs. The Flash converter described above can be implemented using a two step approach, where the input magnitude is quantized with a certain number of bits and then turned it back into analog using a digital-to-analog converter (DAC). This is subtracted to the input amplitude and the result is amplified and converted into digital. The final digital word is the combination of the bits from both processes. The most significant bits (MSBs) are obtained from the first conversion, while the least significant bits (LSBs) are obtained form the second conversion. Pipeline converters do this process with a number of stages equal to the number of desired bits. Instead of obtaining half of the bits in one stage and the other half in the other as in two step converters, each stage provides one single bit. Integrating ADCs are another type of ADC and will be explained in next chapters. The last two main types of ADCs are successive approximation register ADCs (SAR-ADCs) and oversampling converters, that include Sigma-Delta modulators and voltage-controlled oscillator ADCS (VCO-ADC). A more detailed look to these will be taken, given its importance for this dissertation.

But before we take a deeper look to these architectures, one more classification of ADCs must be explained. In the previous paragraphs, ADCs have been described according to its topology. Another classification is made according with the relationship of the sampling frequency and the bandwidth of the sampled signal. Under this classification two types of ADCs exit, nyquist rate ADCs and over-sampled ADCs. Nyquist rate ADCs operate at a sampling frequency two times the signal bandwidth (in practical implementations it is usually closer to five or ten times) following the Nyquist criterion. Oversampling converters operate at a sampling frequency several times higher than the signal bandwidth. The relationship between the sampling frequency and the Nyquist frequency (two

times the signal bandwidth) is called the oversampling ratio (OSR). The use of oversampling allows to reduce quantization noise. Quantization noise derives directly from the quantization error which is what determines the resolution of a digital signal and is dependent on the number of bits. Sigma-Delta modulators and VCO-ADCs are a specific type of oversampling converters, that further improves the quantization noise by performing noise-shaper.

1.3.1 Successive approximation register ADC

Successive approximation register ADCs (SAR-ADCs) are one of the most popular ADC topologies thanks to its simple design. This allows for a high resolution and speed while maintaining small area and power consumption. They have been used in low SNR MEMS applications such as voice recognition and similar tasks. To interface with the MEMS a programmable gain amplifier (PGA) is usually placed before the SAR-ADC. The SAR-ADC performs the analog-to-digital conversion through a binary search algorithm. The block diagram of the converter is shown in Fig 1.5. It is composed of a S/H circuit to sample the input voltage, a comparator, a DAC and a successive approximation register (SAR). The SAR controls the DAC, which in turn generates the voltage that will be compared with the input voltage to be converted. The conversion have three phases called sampling, hold and redistribution. This last phase is performed in several steps. In each of these steps the input voltage is compared with a reference voltage, and the result of this comparison determines one of the outputs bits of the ADC.

The conversion begins with the sampling phase. During this phase the S/H samples the input signal. After this the input signal is hold during the hold phase. The next phase is the redistribution phase. At the beginning of this phase the SAR's MSB is set to one, while the other bits are set to zero. Then the digital word contained in the SAR is converted into an analog voltage by the DAC and compared with the input voltage. If the reference voltage is higher than the input voltage the output of the comparator is zero, while the opposite case yields a one. The output of the comparator is then assigned to the MSB,and the described process is repeated with the next bit, which is set to one while the already converted bits (the MSB only in the second step) keep the set value, and the rest of the bits are turn to zero. This process is repeated until all the bits of the ADC are set.

The more popular type of SAR-ADC is the charge-distribution SAR-ADC. This architecture uses a binary-weighted capacitor array and a comparator as is shown in Fig 1.6. The binary-weighted capacitor array serves two purposes, it is both the DAC and S/H. To simplify the following explanation, let's call the plates of the capacitors connected to the input of the comparator the top plates and the others the bottom plates. The first step of a conversion consist on connecting the top plates to ground, while the bottom plates are connected to V_{in}. This samples V_{in}. After that the top plates are disconnected from ground, while the bottom

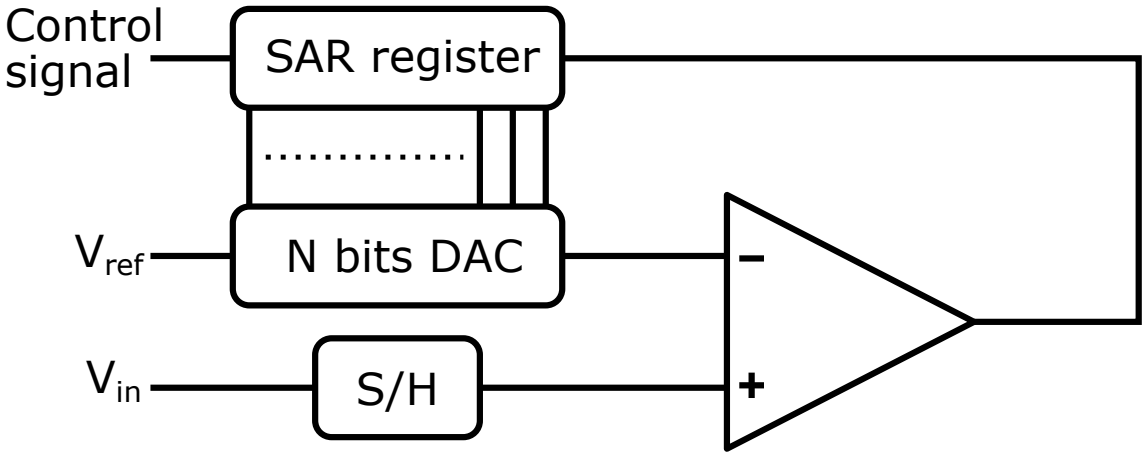

FIGURE 1.5: Block diagram of SAR converter

plates are connected to ground. This sets a voltage $-V_{in}$ at the input of the comparator (in the top plates). Then the bottom plate of the capacitor corresponding to the MSB is connected to V_{ref}. The voltage at the input of the comparator (V_{comp}) is then:

$$V_{comp} = -V_{in} + \frac{V_{ref}}{2} \tag{1.4}$$

The output of the comparator is the value of the MSB, zero if (1.4) is negative and one if it is positive. After the MSB is converted the conversion for the next bit begins. The steps used to determine the value of the next bit are the same that with the MSB, with the difference that the MSB is set to the value resulting for the conversion while remaining non converted bits are set to zero as explained in the general description above. The value V_{comp} for this conversion is:

$$V_{comp} = -V_{in} + B_{M-1}\frac{V_{ref}}{2} + \frac{V_{ref}}{4} \tag{1.5}$$

Where B_{N-1} in (1.5) is the value of the MSB set in the previous conversion and M is the number of bits of the ADC. The procedure is then repeated for the following bits until all bits have been determined. The value for V_{comp} during the conversion of the N^{th} bit is:

$$V_{comp_{N^{th}}} = -V_{in} + \sum_{i=1}^{N-1} B_{M-i}\frac{V_{ref}}{2^i} + \frac{V_{ref}}{2^N} \tag{1.6}$$

Once the LSB bit has been determined, the conversion process begin again taking a new sample of the input voltage. The elapsed time between the sampling phase and the end of the distribution phase is equal to the sampling period. The minimum number of clock cycles during a sampling period is equal to M+1 for a M bits ADC. The generation of non-overlapping control signals is also

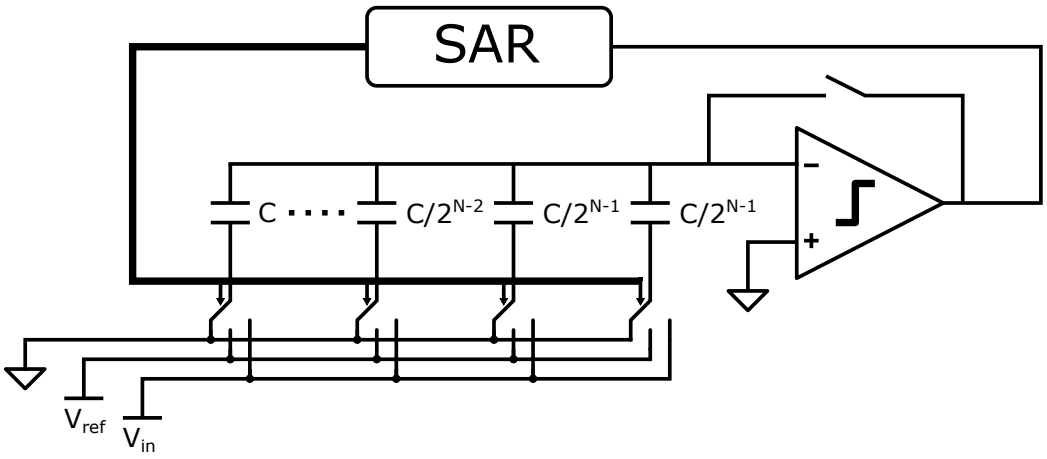

FIGURE 1.6: Circuit schematic of a SAR converter

needed. SAR-ADCs can be used as Nyquist-Rate ADC [10]–[12] and as quantizers in Sigma-Delta converters [13]–[15].

1.3.2 Sigma-Delta modulators

Today the most common approach to implement MEMS digital microphones is to use discrete-time Sigma-Delta ADCs. Quantization noise was mentioned in the introduction of this section. Before understanding Sigma-Delta modulators is of interest to give a deeper look to what quantization noise is. As it has been already explained, one of the steps to convert an analog signal into a digital one consist on quantizing the analog value into the closest possible digital values. As digital words have a finite number of bits they also have a finite number of values. The difference between the quantized digital value and the original analog value is called the quantization error. This error limits the resolution of the ADC and is clearly linked with the number of bits. The higher the number of bits the lower the quantization error. This is what we find in Nyquist-rate converters. Now if we sample the analog signal at a rate much higher than the one required by the Nyquist theorem, i.e with a high OSR, and then look at the power spectral densty (PSD) of the quantization error, it can be observed that this quantization error looks like white noise (although it is not as the quantization error is correlated with the input signal). This is what is called quantization noise.

To get this quantization "noise" we had to oversample the signal. In order to get the output digital signal we have to reduce the sampling rate to the Nyquist rate. For this we run the moving average of the samples and then take one of every several samples, i.e decimate, the output signal to reduce the output rate to the Nyquist rate. By doing this it can be observed that the resolution of the digital

signal is improved. Then the resolution of an oversampling converter is not given only by the number of bits of the quantizer, but by the ratio between the power of the signal and the power of the quantization noise, what is known as Signal-to-quantization-noise ratio SQNR. This concept is similar to the signal-to-noise ratio (SNR) on amplifiers and other analog circuits.

The increase of the resolution of the ADC by using oversampling is evaluated by comparing the SQNR of a Nyquist-rate ADC, with a certain number of bits in the quantizer (N), excited by a sinusoidal input and the SQNR of the oversampling converter ($SQNR_{ov}$) with the same sinusoidal input. This way the equivalent number of bits (ENOB) of the oversampling converted is calculated, as the number of bits (N) that produces the same SQNR in the Nyquist-rate converter.

$$ENOB = \frac{SQNR_{ov} - 1.76}{6.02} \tag{1.7}$$

$$SQNR_{ov} = 6.02N + 1.76 + 10log(OSR) \tag{1.8}$$

As shown by 1.8 the improvement of the number of bits by bare oversampling is limited. Using an OSR=10 increases the ENOB by 1.7 bits, while using an OSR=100 increases the ENOB by just 3.32 bits. A more effective way to improve the ENOB is to use noise-shaping in addition to oversampling. This is what Sigma-Delta modulators do. This type of oversampling ADCs shape the PSD of the quantization noise, "moving" it out of the frequency band of interest. The effect is similar to high-pass filtering the quantization noise, except for band-pass modulators where the behaviour resembles that of a notch filter. This is done while letting the signal unaffected. The amount of ENOB improvement that can be achieved with a Sigma-Delta modulator is much higher that with simple oversampling and depends on both the OSR and the order of the modulator.

The more simple Sigma-Delta modulator is the first order Sigma-Delta, shown in Fig 1.7 a). As can be seen in Fig 1.7 b) a linear model of the converter can be obtained by linearizing the quantizer as a random noise source, i.e a quantization noise source. By using this linear model the transfer function of both the input signal and the noise are given by:

$$Y(z) = X(z)Z^{-1} + E(x)(1 - z^{-1}) \tag{1.9}$$

Where $E(z)$ represents the quantization noise due to the limited number of quantization levels of the quantizer. In 1.9 the term associated with the quantization noise is a first-order discrete high pass filter. This term is also known as the noise transfer function (NTF), while the term associated with the the input signal ($X(z)$) is called the signal transfer function (STF). It is evident from 1.9 that the STF is just a time delay, and thus the signal is not affected by the noise-shaping filter. The SQNR of a first order Sigma-Delta is given by:

$$SQNR = 6.02N + 1.76 - 5.17 + 30log(OSR) \tag{1.10}$$

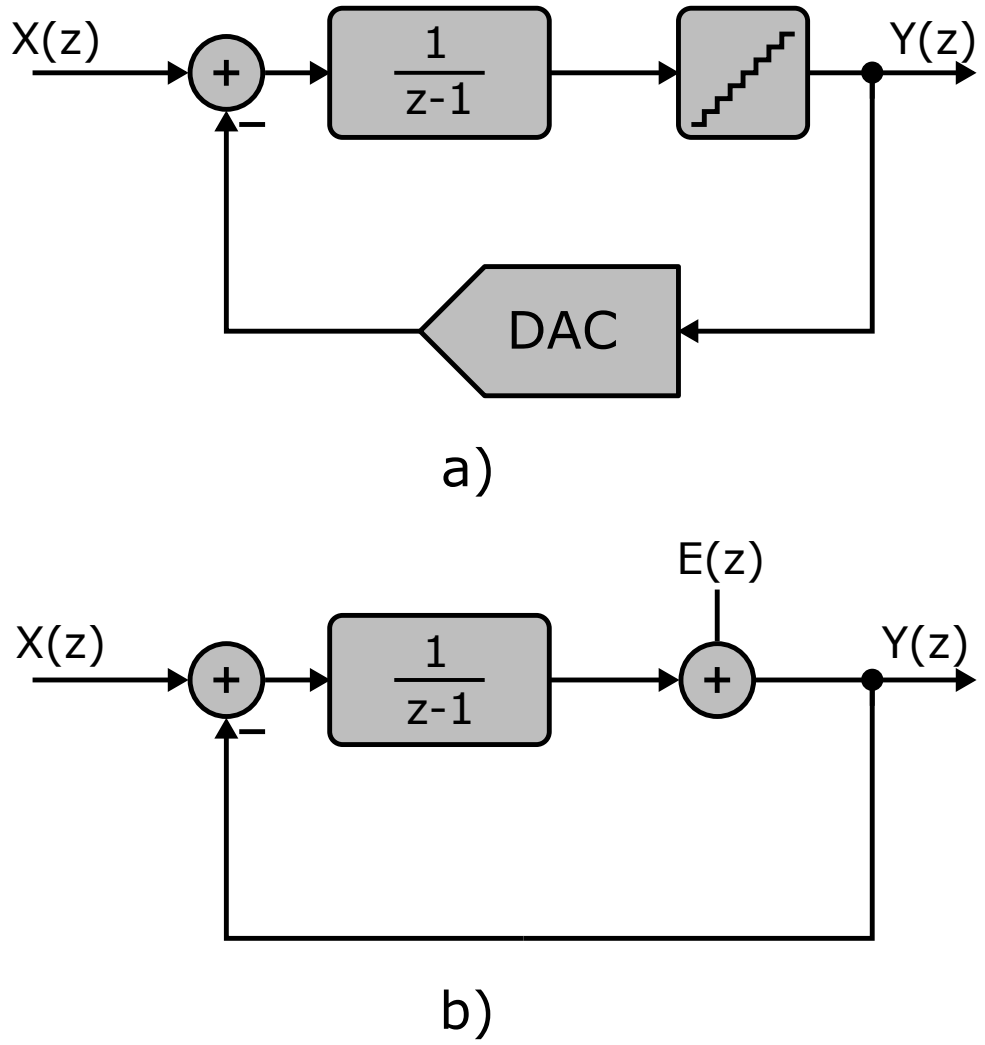

FIGURE 1.7: a) First order Sigma-Delta ADC. b) Linear model.

The SQNR can be improved by increasing the order of the modulator. If we use a 2^{nd} order filter for the NTF, as shown in Fig 1.8, then the noise and signal transfer function of the converter and the SQNR are given by:

$$Y(z) = X(z)Z^{-1} + E(x)(1 - z^{-1})^2 \tag{1.11}$$

$$SQNR = 6.02N + 1.76 - 12.9 + 50log(OSR) \tag{1.12}$$

Higher order filters can be used. Figure 1.9 shows the general topology of a Sigma-Delta modulator of n^{th} order. The transfer function is given by:

$$Y(z) = X(z)Z^{-1} + E(x)(1 - z^{-1})^n \tag{1.13}$$

As mentioned before, aside for a high pass filter the NTF can be realized with

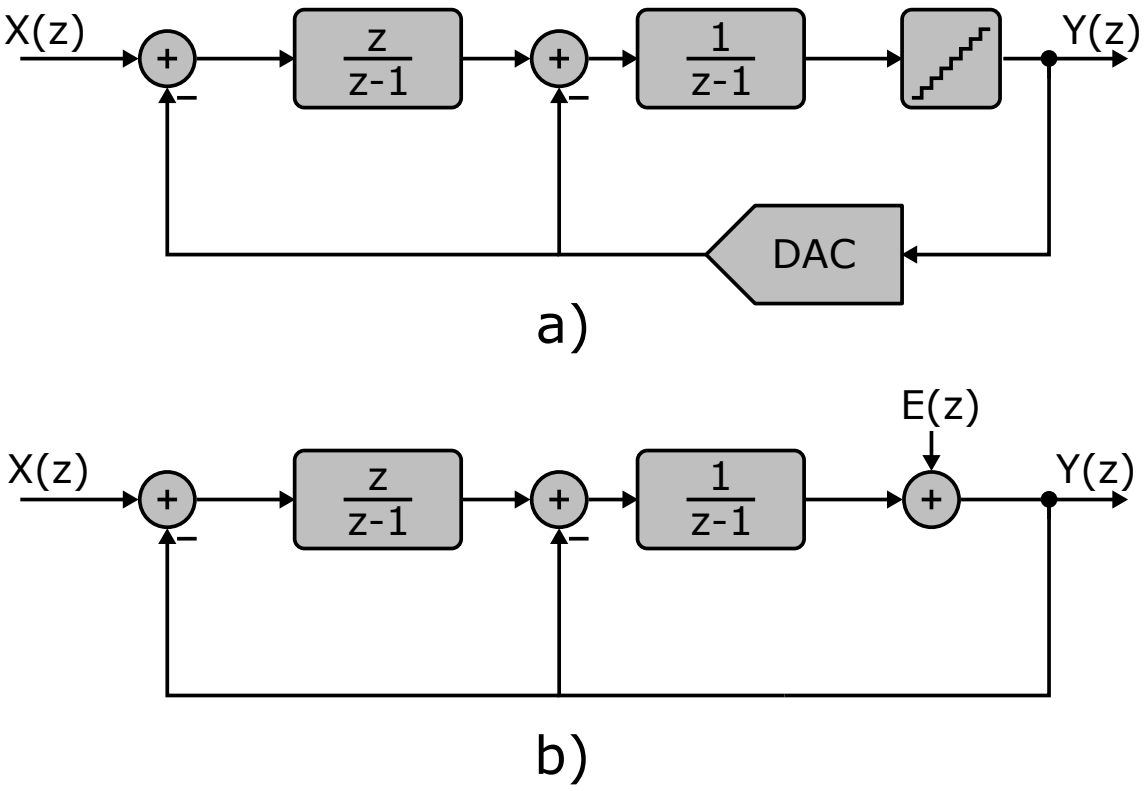

FIGURE 1.8: a) Second order Sigma-Delta ADC b) Linear model.

other type of filters, like a notch filter for bandpass Sigma-Delta converters. Regardless of the shape and the order of the NTF and the STF the general equation for a Sigma-Delta modulator is:

$$Y(z) = X(z)STF + E(x)NTF \tag{1.14}$$

As it can be seen from (1.10) and (1.12) in combination with (1.7), a Sigma-Delta converter with a single bit quantizer can have a multibit ENOB. This allows the implementation of ADC converters with less complex analog circuitry at the price of an increased digital complexity. Given that the CMOS new nodes are better suited for digital processing, this trade-off becomes more desirable as technology progresses. Nevertheless, Sigma-Delta modulators still require high gain analog circuits like operational amplifiers (Miller opamps) and operational transconductance amplifiers (OTA). Also, the state variable in the integrators of the filter is in the voltage domain, and its level must track that of the imput signal. These facts make the design of conventional Sigma-Delta modulators challenging in submicron nodes with inherently lower gain transistors and a small supply voltage.

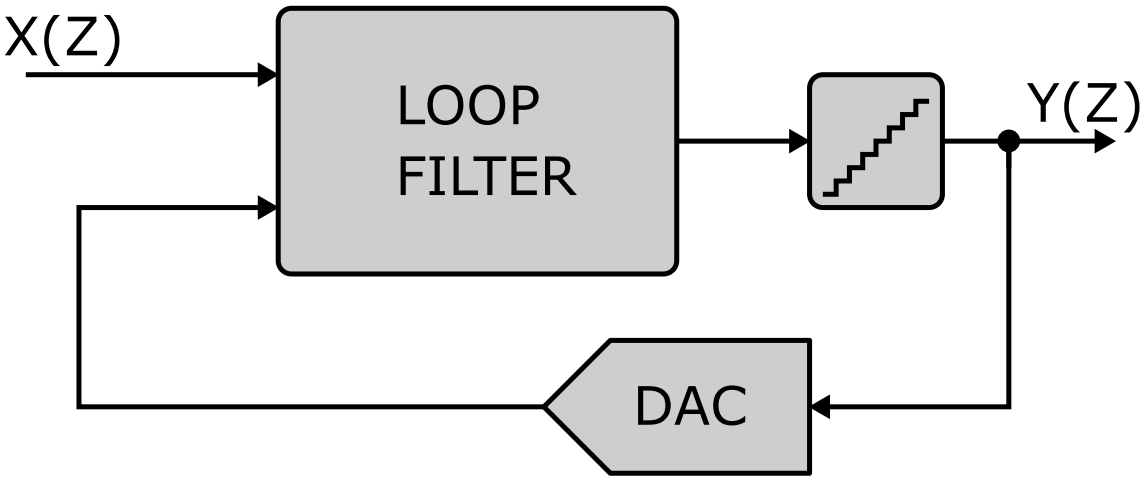

FIGURE 1.9: N^{th} Order Sigma-Delta ADC

1.3.3 VCO based ADCs

VCO based ADCs are another type of analog to digital converters. They are usually implemented with ring oscillators (RO). The ring oscillator based ADC (RO-ADC) is an alternative to the Sigma-Delta modulator that tries to overcome the problems faced when designing in smaller nodes. RO-ADCs converters [16] show noise shaping properties similar to Sigma-Delta modulators. Unlike a conventional Sigma-Delta modulator and the other previously mentioned converters (except for integrating ADCs) which are voltage-encoding converters, the RO-ADC is a time-encoding converter. In time-encoding converters, the input signal is encoded in time domain instead of voltage domain before conversion. But this is not the only important characteristic of the RO-ADC, as like the Sigma-Delta modulator, the RO-ADC also show noise-shaping behaviour.

The basic building blocks of an RO-ADC are an inverted based ring oscillator and a frequency-to-digital converter (F2D). The inverter based ring oscillator frequency encodes either an input voltage signal or current signal. When the input signal is in the form of a voltage, the ring oscillator is called voltage-controlled oscillator (VCO), while in the case of an input current the oscillator is a current-controlled oscillator (CCO). The output of the inverter based ring oscillator is a square signal whose frequency depends on the input signal following:

$$f_{RO}(t) = f_0 + k_{RO}X(t) \tag{1.15}$$

Where $f(t)$ is the RO output frequency, f_0 is the RO oscillation frequency when no input signal is applied, k_{RO} is the RO input-to-frequency gain and $X(t)$ is the input signal.

Figure 1.10 shows the basic structure of an RO-ADC. This structure is known as the open-loop RO-ADC as opposed to the closed-loop RO-ADC that employs a feedback loop. The difference between these topologies will be explained later in

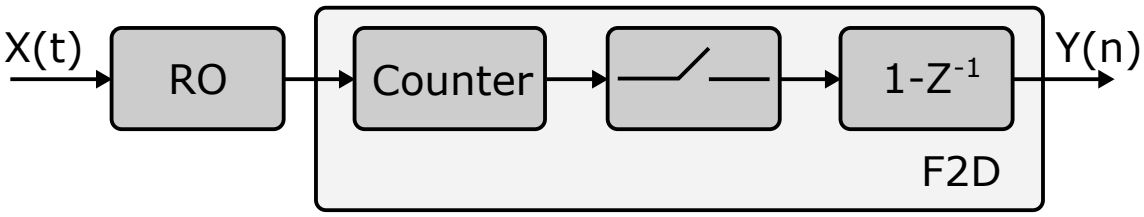

FIGURE 1.10: Ring oscillator based ADC

this dissertation. For now we will focus on the open-loop RO-ADC for the shake of simplicity. The RO-ADC of Fig 1.10 is composed of an RO, a counter, a sampler and a first difference block. The counter, sampler and first difference block forms the F2D. For the following explanation the counter will be considered an infinite counter. As stated above, the input signal $X(t)$ is frequency encoded by the RO. Once the input signal is encoded in frequency, the F2D counts the number of periods that happen during a certain time interval. This time interval is equal to the sampling period. The number of oscillator periods in the sampling interval is the sampled value, and depends on the input signal as shown by (1.15). After this the value of the current sample is first differentiated with the value of the previous sample.

Let's dive a little bit more in what it is happening. If we assume that the oscillator is perfectly linear (which it really is not but more on that later) then the input signal is perfectly mapped into frequency by (1.15). If we could measure the frequency with an infinite resolution then our digital signal would not have any quantization error. Of course to represent this ideal digital value we would need an infinite number of bits.

As previously stated, a way to measure the frequency of a square wave signal is to count the number of edges during a certain period of time. This will give the number of oscillator periods happening during this period of time, that is the sampling period. The problem is that as the number of periods is not necessarily a multiple of the sampling period, then we will be counting either one extra period, or one period less. This is the source of the quantization error in an RO-ADC. If the quantization error is the difference between the analog value and the digital value then the frequency of the RO (f_{RO}) at a given sample, n, is:

$$f_{RO}(n) = [N_{count}(n) - N_{count}(n-1)] \cdot f_S + e(n) - e(n-1) \tag{1.16}$$

Where f_s is the sampling frequency, N_{count} is the number of edges counted and,e is the quntization error. Notice how the first difference has already been performed in (1.16). This is because we need to know the number of edges since the last sample to calculate the oscillation frequency, not the total number of edges that have been detected during the current sampling period and the previous ones. Taking this into account we can rewrite (1.15) calling $N_{period}(n)$ to the number of periods that happened in the sampling interval n

$$f_{RO}(n) = N_{period}(n) \cdot f_S + e(n) - e(n-1) \tag{1.17}$$

It is clear from 1.17 that the quantization noise is first order noise-shaped. This expression also shows that noise-shaping is performed by the F2D block, as this is the block that counts the number of edges and computes the first difference.

Another way to analyze oscillator based ADCs is proposed in [17], [18]. The RO-ADC is analyzed as a pulse frequency modulator (PFM). According to this the oscillator modulates the frequency of the pulses with the input signal. The frequency components of the PFM are then filtered by a sinc filter with zeros at multiples of T_S, and then sampled. The resulting alias that fall into the 0 to $f_S/2$ frequency band increase with frequency following a 20dB/decade slope. This results in a spectrum similar to that of a Sigma-Delta modulator. The noise-shaped quantization noise is the sinc-shaped aliases of the PFM side bands. This analysis allows to theoretically predict the frequency components and maximum SQNR of a RO-ADC with precision unlike the random quantization noise approach.

Aside to implement first order noise-shaping ADCs, open loop RO-ADCs can also be used as the quantizer on conventional Sigma-Delta modulators. In this case the quantizer adds an extra noise-shaping order to the converter. Finally higher order modulators can be implemented using digitally controlled ring oscillators DCOs in closed-loop topologies.

1.4 Introduction to the objectives of this thesis

The main objectives of this dissertation are:

- Explore different topologies of time-encoding ADCs with noise shaping with special focus on voltage controlled oscillator based ADCs (VCO-ADCs).
- Analyze VCO-ADCs open-loop architectures to implement high dynamic range MEMS digital microphones.
- Develop, fabricate and measure experimentally a reference design of a high dynamic range MEMS digital microphone based on an open-loop VCO-ADC.
- Propose and prove experimentally solutions for the non-linear tuning curve of VCOs in ADC applications using frequency encoded feedback architectures.
- Explore the use of frequency-to-current converters together with VCOs in alternative applications.

Chapter 2

Dual slope ADC architectures for capacitive MEMS sensors

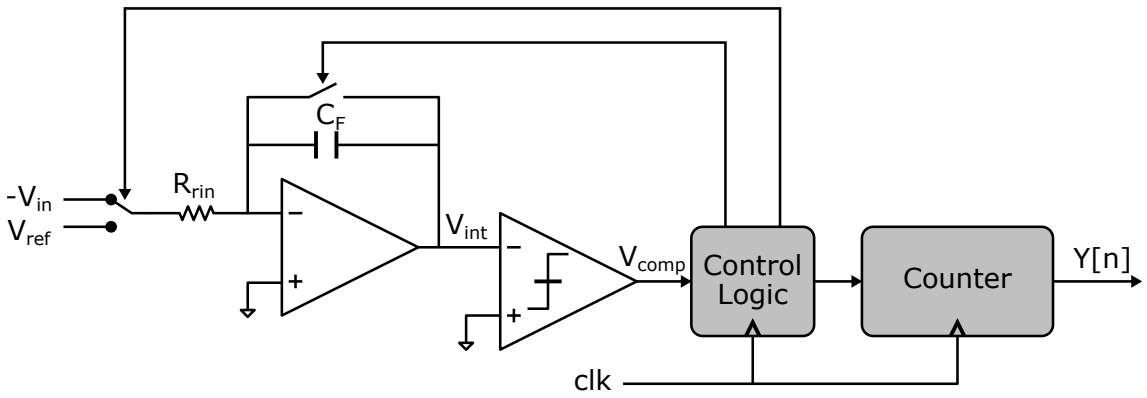

FIGURE 2.1: Schematic of a dual-slope ADC

Dual-slope ADCs are a type of ADCs known also as integrating converters [19]. This type of converters was mentioned first in section 1.3 of the present document. The structure of a dual-slope ADC is shown in Fig 2.1. As it can be seen from the figure, the hardware used in this converter is very simple. It has an operational amplifier based analog integrator, a comparator, an analog switch and some digital circuitry to control the operation. The basic building blocks are the same than in a 1 bit first order Sigma-Delta modulator.

Dual slope ADCs operate in two phases. Each phase last for half a sampling period, T_s. During Phase I, the analog switch is connected to the input voltage to be converted. This causes the input voltage to be integrated in the capacitor C_F through resistor R_{in}. The voltage at the output of the integrator at the end of Phase I is then proportional to the input voltage. Once Phase I has finished, the analog switch is connected to a reference voltage, V_{ref}. This discharges capacitor C_F with a constant slope during Phase II. In Phase II, the number of clock cycles during witch the output of the integrator is above the reference level of the comparator is counted. The result of this count is the output digital value. Once the comparator threshold is reached, the integrator is reset. This operation is depicted in the time diagram of Fig 2.2.

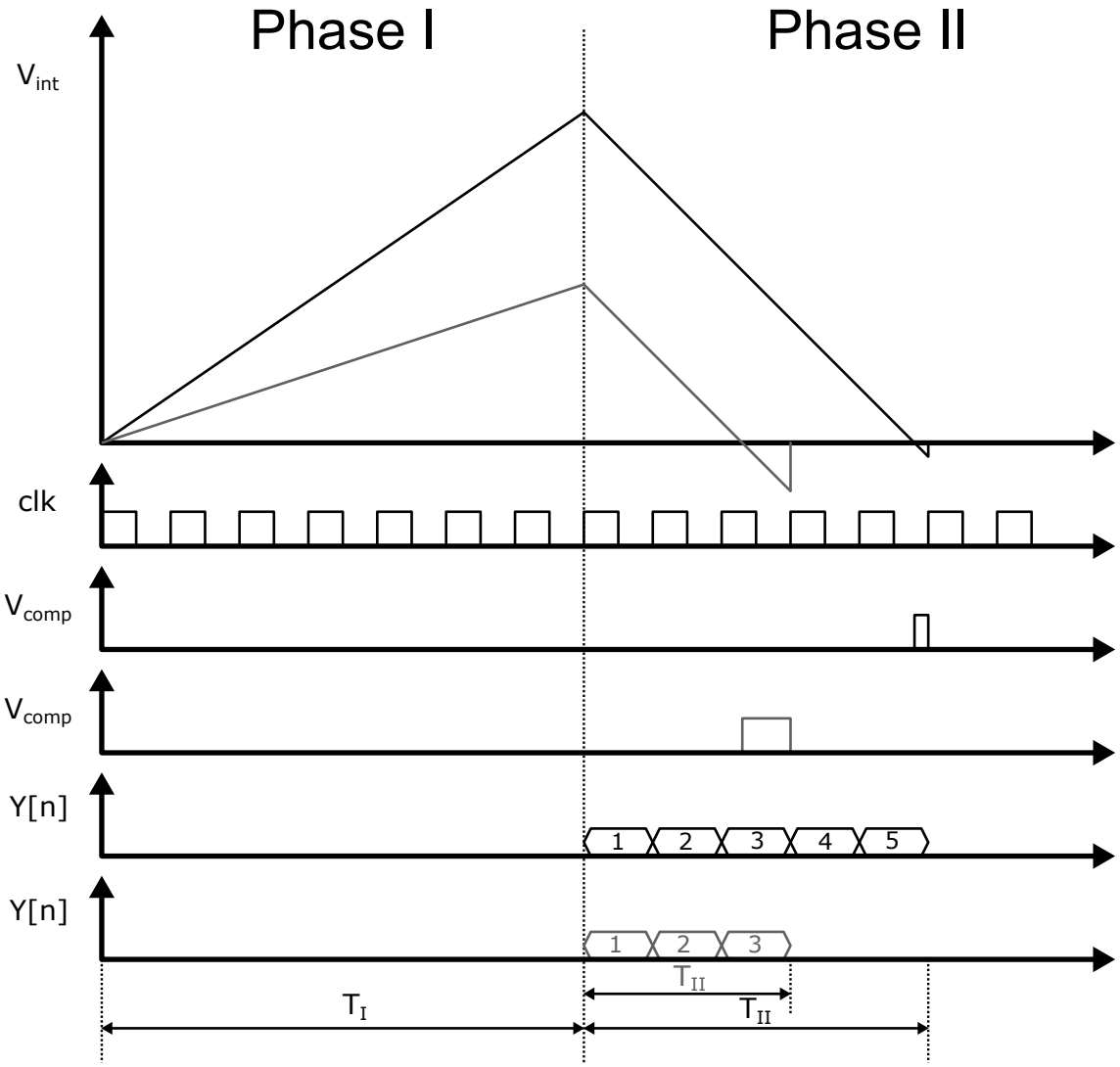

FIGURE 2.2: Conversion cycle of a dual-slope ADC, for two different input signals (Black and grey).

The voltage at the integrator at the end of Phase I is given by the following expression:

$$V_{int} = \frac{V_{in}}{R_{in}C_F}T_I \tag{2.1}$$

Where T_I is the time interval of Phase I, whose length is given by:

$$T_I = 2^{N_{bits}}T_{clk} \tag{2.2}$$

Being N_{bits} the number of bits of the converter, and T_{clk} the period of the clock given by:

$$T_{clk} = 2^{N_{bits}+1}T_s \tag{2.3}$$

The maximum time length of Phase II, T_{IImax}, is also given by expression 2.2. According to Fig 2.2 the value of V_{int} at the end of Phase II must be zero plus a certain voltage. This residual voltage is the quantization error. This quantization error comes from the fact that the circuit is controlled with a clock with a certain period. The smaller the clock period is compared to the maximum time length of Phase II, the higher the number of clock cycles during Phase II and thus the resolution. This clock frequency also determines the number of bits of the counter, which are the same than the number of bits of the converter. To calculate the time it takes to discharge capacitor C_F during Phase II we assume the initial value of V_{int} at the beginning of Phase II is the one given by (2.1), while the final value is zero. From this we get:

$$T_{II} = T_I \frac{R_{in} C_F V_{in}}{R_{in} C_F V_{ref}} = T_I \frac{V_{in}}{V_{ref}} \tag{2.4}$$

One of the main advantages of this kind of converters is that resistor R_{in} and integrating capacitor C_F are present in both phases, as it is shown by expression 2.4 . Thanks to this the digital output does not depend on the value of these components. Another advantage is that the dual slope ADC has a built in input filter that eliminates the requisite of an anti-aliasing filter. This input filter has nulls at integer multiples of $1/T_I$, and has the following transfer function:

$$|H(f)| = \left| \frac{sin(\pi f T_I)}{\pi f T_I} \right| \tag{2.5}$$

The anti-alias filter defined by (2.5) is present when the converter is implemented in continuous time. For switched-capacitor implementations an actual anti-alias filter is needed before sampling. The main drawback of this ADC, is that the resolution is determined by the time length of Phase II versus the clock frequency. This imposes either a very fast clock or a small sampling frequency. Is because of this that this type of converter is used to convert signals with a very low bandwidth when high precision is required.

2.1 The noise-shaping dual-slope 1^{st} order ADC architecture

A way to solve the these limitations is to use the aforementioned property of the residual voltage in the integrator at the end of Phase II being the quantization error in voltage [20]. Using this property and a slightly different operation than the one shown in Fig. 2.2, the dual-slope converter can be turned into an oversampling converter showing first order noise-shaping properties. Capacitor-to-digital converters, (CDCs), using a 1^{st} order noise saped dual-slope has been shown in the literature [21], [22]. The later of these works shows the possibility to couple a MEMS pressure sensor directly to the noise-shaping dual-slope

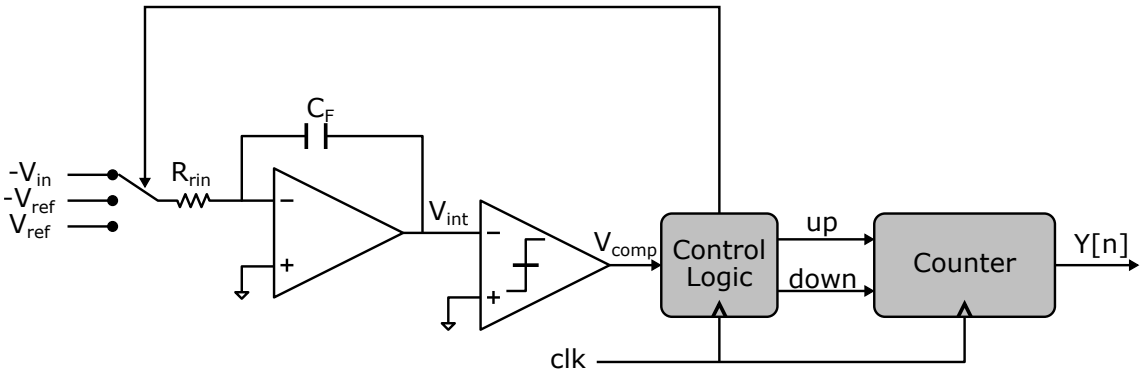

FIGURE 2.3: Schematic of the noise-shaping dual-slope ADC

ADC, without the need of any extra analog front-end. The fact that the voltage in the integrator at the end of Phase II is directly the quantization error in voltage, makes this circuit an interesting alternative to implement the first stage of Sigma-Delta multi-stage architecture (MASH). This property has been exploited in some works [23], [24].

The schematic of this topology is shown in Fig 2.3. The circuit is similar to the conventional dual-slope ADC (Fig. 2.1), with some minor changes. In the noise shaped-dual-slope ADC, the switch that resets the integrator at the end of Phase II is omitted, as now the value stored in capacitor C_F is the quantization error, that is subtracted from the input in the following conversion. The other change consist on adding a negative reference voltage, $-V_{ref}$. The operation of this noise-shaping dual-slope converter is shown in Fig 2.4.

The Phase I operation is similar to the one described in the previous section (Fig. 2.2). The differences are found in Phase II. In the noise-shaping dual-slope, instead of resetting the integrator once the value has crossed the comparator reference voltage (0 V in the presented examples of this document), the voltage in the integrator is left oscillating until Phase II reach the maximum number of cycles. The negative reference voltage, $-V_{ref}$, is used to perform this oscillation. The digital value is obtained using a counter. At the end of Phase I, the counter has a value of zero. With each clock edge during Phase II, the counter either adds +1 or -1 depending on whether the output of the comparator is a low level or a high level respectively. This is shown in the signal $Y[n]$ of the time diagram of Fig.2.4.

Although not shown in Fig. 2.4, the value of V_{in} can have both polarities, and the converter can produce both positive and negative digital outputs. Is because of this that the counter has to be able to count both negative and positive numbers. Thus the total number of bits in the counter are $N_{bits} + 1$. Finally, it is interesting to note that this converter can be implemented either in continuous time or with a switched-capacitor circuit (discrete time). In the case of the former, the intrinsic sinc filter mentioned in the previous section and given by expression (2.5), can be used as an anti-alias filter. For the switched-capacitor version this

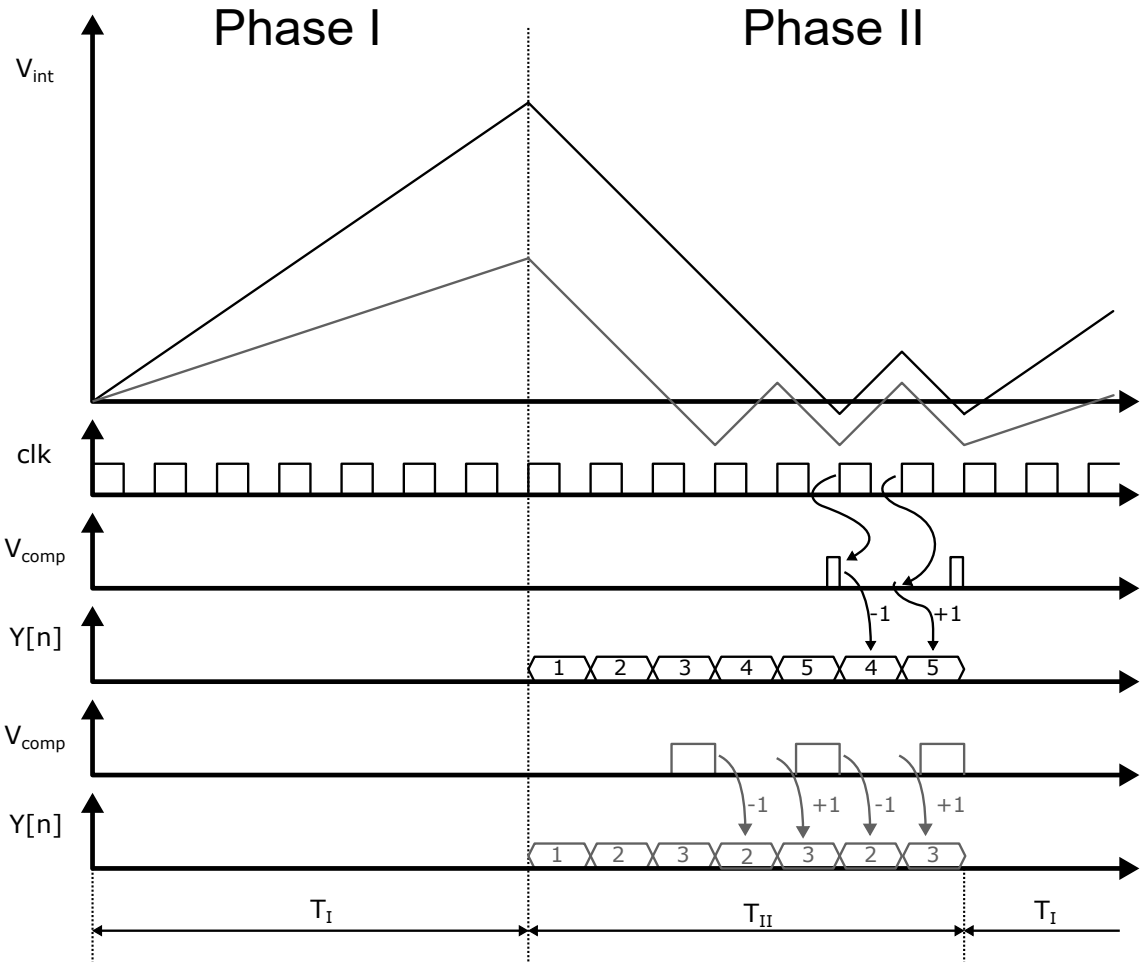

FIGURE 2.4: Conversion cycle of a noise-shaping dual-slope ADC, for two different input signals (Black and grey).

property can not be used as the sampling happens before the ADC.

This converter is equivalent to a first order sigma-delta with a multi-bit quantizer. The number of bits in the quantizer is given by:

$$N_{bits} = log_2 \frac{T_I}{T_{clk}} \tag{2.6}$$

This architecture has a limitation, specially when converting signals with wide bandwidth or when using high oversampling ratios. In both cases the sampling frequency has to be high, limiting the amount of clock periods in Phase I and Phase II, and thus the number of bits of the quantizer. This limits the maximum achievable SQNR, as the converter has only first order noise-shaping.

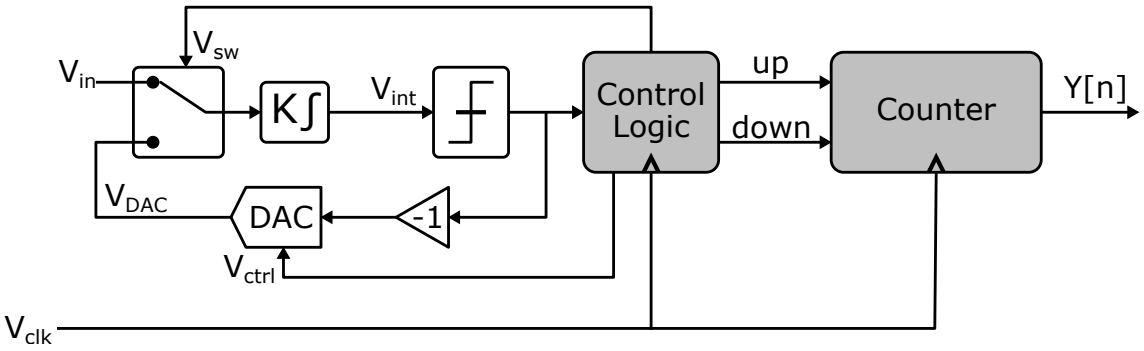

FIGURE 2.5: Behavioural schematic of the SAR noise-shaping quantizer

2.2 The integrating SAR noise-shaping quantizer

A way to improve the resolution of the noise-shaping dual-slope converter is to implement a multi-bit feedback with a DAC [25]. This quantizer is similar to an integrating ADC where the charge stored in the integration phase is afterwards measured with a SAR algorithm. As with the noise-shaping dual-slope ADC, the charge residue present at the integrator after a measurement cycle is stored for the next conversion, providing first-order noise shaping. Also, as with that architecture, the quantization error is available as a voltage at the end of the conversion, which is useful to implement multistage topologies. Nevertheless, the advantage shown by expression 2.4 is lost, as the resistor used during Phase I (or capacitor in a discrete time implementation), can not be the same that the one used during Phase II. This is obviously due to the fact that a DAC and not a simple resistor is used during Phase II, to implement the multi-bit feedback.

Figure 2.5 shows the block diagram of the SAR noise-shaping quantizer. It is composed of an integrator, a switch, a single bit comparator, a multi-bit binary weighted DAC and digital logic to control the operation of the circuit. Its operation is divided in two phases: Phase I and Phase II. If we assume a clock period T_{clk} and that Phase I and Phase II last M and N clock cycles respectively, an equivalent sampling period of $T_s = (M+N)T_{CLK}$ can be defined. During Phase I, signal V_{sw} toggles the switch to connect the input voltage of the quantizer to the integrator. A charge proportional to the input voltage is stored in the integrator during M clock periods. During Phase II the switch controlled by V_{sw} change to the binary multi-bit DAC. In this phase the digital control calculates the N bits of the signed output code as the successive outputs of the comparator, in the same way a SAR ADC does. The DAC output will be updated and held each clock cycle T_{clk} until the end of Phase II with successive binary weighted values proportional to M. Finally, the charge residue present at the integrator after a measurement cycle T_s is stored for the next conversion, providing first-order noise shaping.

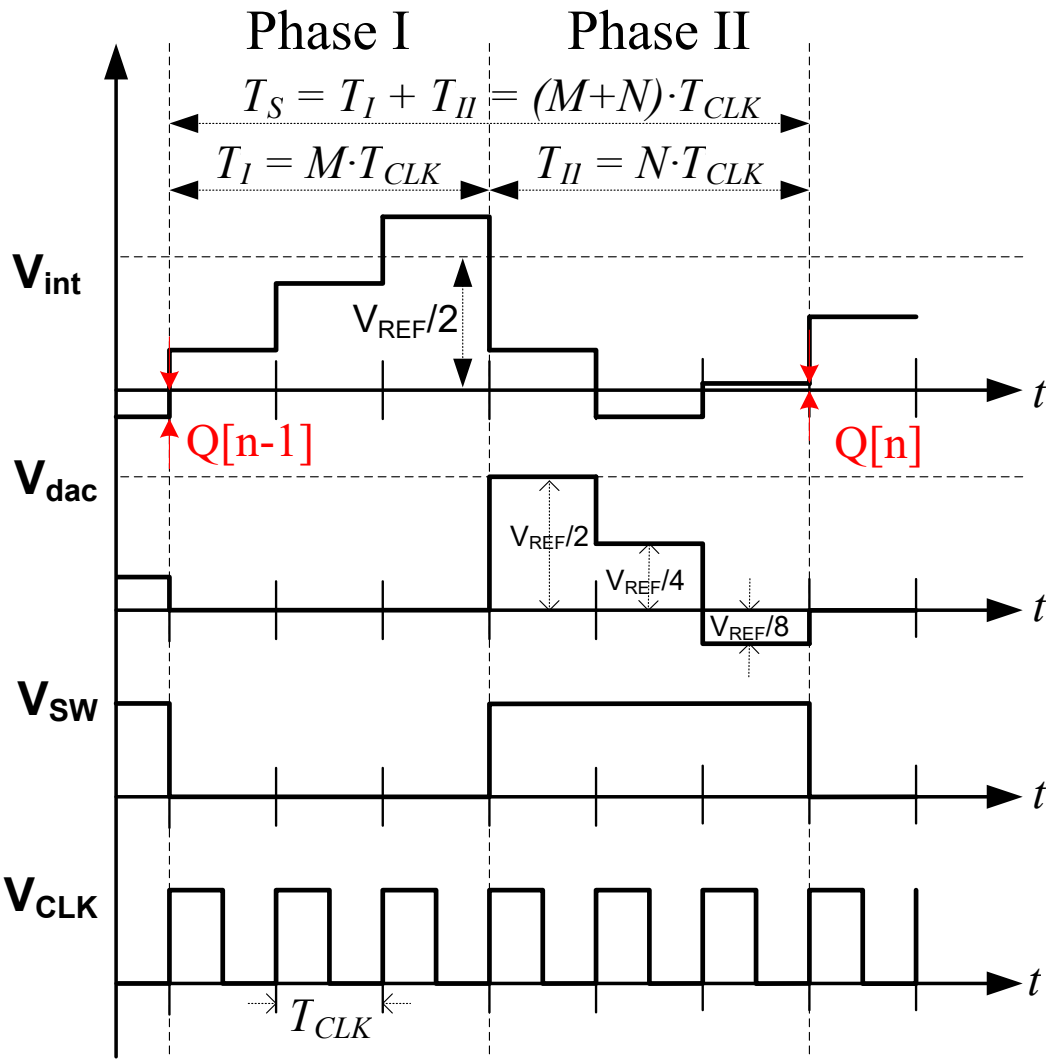

FIGURE 2.6: Conversion cycle of the SAR noise-shaping quantizer

To illustrate with more detail the operation of the quantizer, a complete conversion cycle is depicted in Fig. 2.6. This figure shows the integrator voltage V_{int}, the DAC voltage V_{DAC}, the control signal of the switch V_{sw} and the clock signal V_{clk} during one sampling period. V_{REF} in this figure is given by the relationship:

$$V_{REF} = \frac{V_{FS}}{2} \tag{2.7}$$

where V_{FS} is the full scale of the quantizer. At the beginning of the sampling period, the value of V_{int} holds the value of the quantization error of the previous conversion. To compute the value of V_{int} at the end of Phase I an auxiliary voltage is defined:

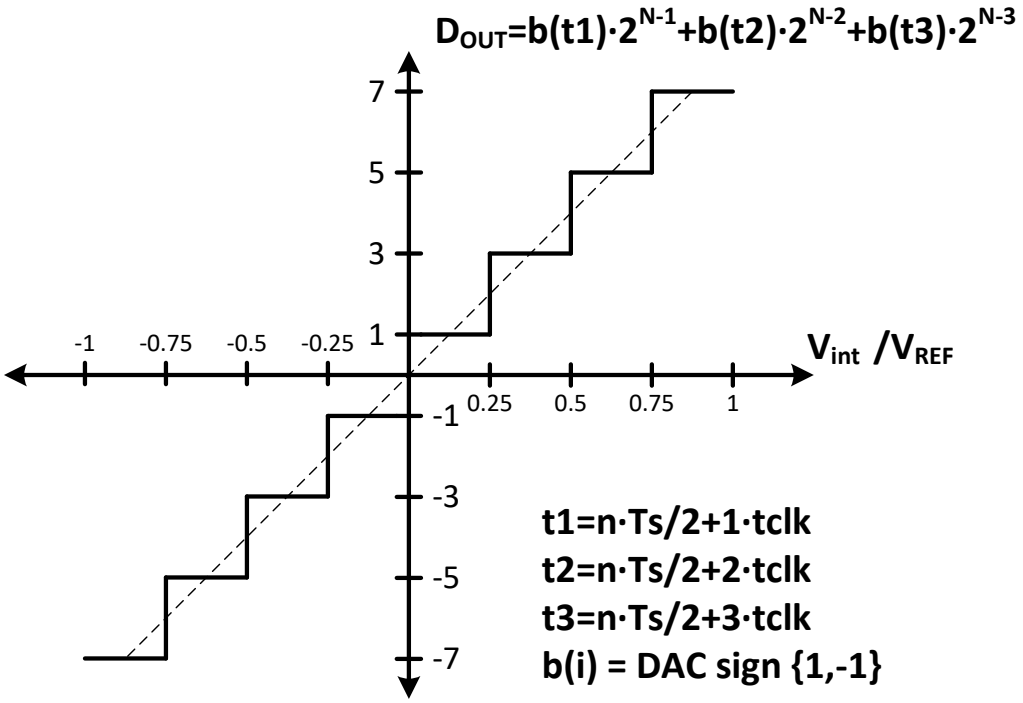

FIGURE 2.7: SAR noise-shaping quantizer transfer function

$$V_{aux}((n+1)T_s) = \frac{1}{M}\sum_{j=1}^{M} V_{in}((nT_s) + jT_{clk}) \tag{2.8}$$

with j representing the number of each clock cycle during Phase I. Using (2.8), the value of V_{int} at the end of Phase I is given by:

$$V_{int}((nT_s) + MT_{clk}) = K \cdot M \cdot V_{aux}((n+1)T_s) + V_{int}(nT_s) \tag{2.9}$$

If an auxiliary voltage for the DAC is defined as follows:

$$V_{DACaux}((n+1)T_s) = \frac{V_{FS}}{2}\sum_{i=1}^{N} \frac{b_i}{2^i} \tag{2.10}$$

where b_i in (2.10) is the digital output of the single bit comparator during the i^{th} clock period of Phase II. The digital output takes the value of 1, if the voltage V_{int} is above zero, or -1 if the voltage V_{int} is below zero. Using (2.9) and (2.10) the voltage V_{int} at the end of the n^{th} cycle of conversion is defined as:

$$V_{int}((n+1)T_s) = V_{int}(nT_s + T_I) - KV_{DACaux}((n+1)T_s) \tag{2.11}$$

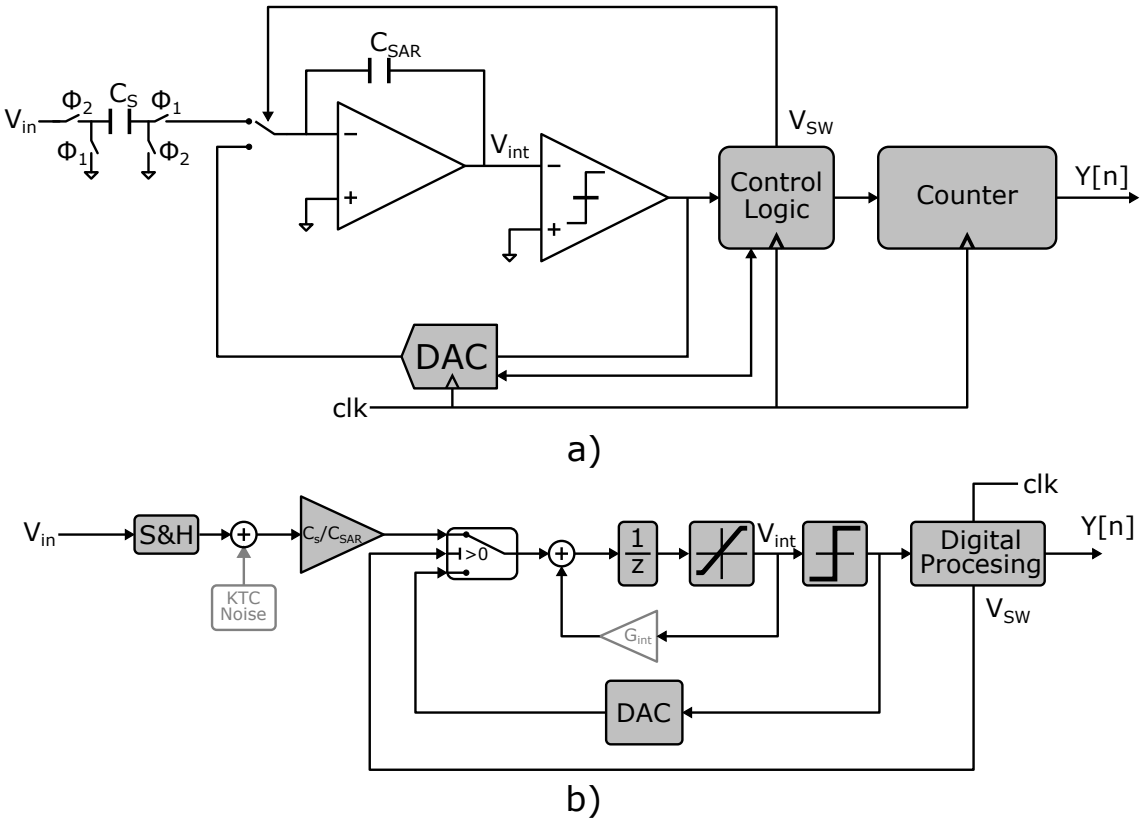

FIGURE 2.8: a) Example of circuit implementation of the NSQ with a switch capacitor technique. b) Model of the NSQ

where K is the gain of the integrator. Rearranging (2.11) and taking the Z-transform, equation 2.12 is obtained:

$$\frac{1}{M}V_{DACaux}(z) = V_{aux}(z) - \frac{V_{int}}{KM}(1 - z^{-1}) \tag{2.12}$$

Equation 2.12 shows that the quantization error is first order noise shaped and given by $-V_{int}/KM$.

The transfer function of the quantizer is shown in Fig. 2.7. For this example the quantizer of Fig. 2.7 has a value N=3, equivalent to 3 bits of resolution. This result in eight quantization levels. In order to calculate the digital value of the quantizer, the outputs of the comparator are summed as shown:

$$D_{out} = \sum_{i=1}^{N} b_i 2^{N-i} \tag{2.13}$$

where b_i is given by:

$$b_i = sign(V_{int}(nT_s + (M+i)T_{clk})), -1, 1 \tag{2.14}$$

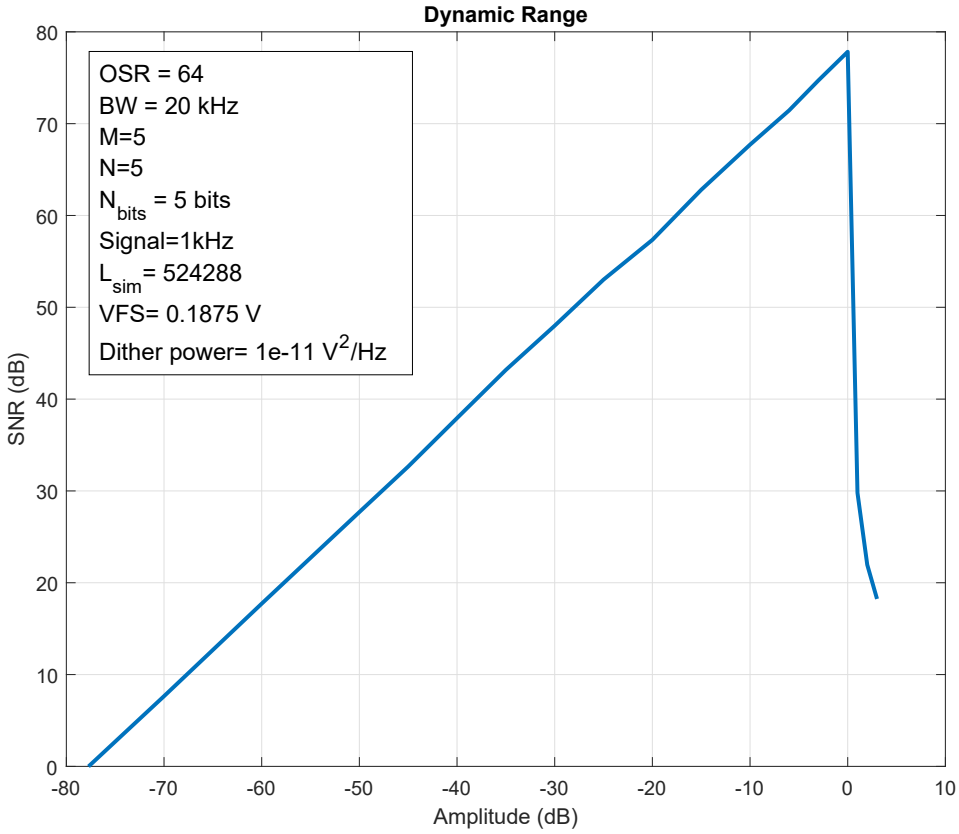

FIGURE 2.9: Simulated dynamic range of the SAR-NSQ using the ideal model of Fig.2.8 b)

with i being the number of clock cycles in Phase II for which b_i is computed. D_{out} in equation 2.13 represents the digital value proportional to the input voltage V_{int} at the end of Phase I. The maximum input signal of the quantizer in order to have a correct noise-shaping operation is given by:

$$V_{aux(max)} = \frac{V_{FS}}{2M} \sum_{i=1}^{N-1} \frac{1}{2^i} \tag{2.15}$$

Using the least significant bit, $LSB = \frac{1}{2^N}$, expression 2.15 can be rewritten as:

$$V_{aux(max)} = \frac{V_{FS}}{2M}(1 - 2 \cdot LSB) \tag{2.16}$$

A way to implement the circuit of the NSQ using a switched-capacitor technique is shown in Fig.2.8 a). Figure 2.9 shows the simulated dynamic range using an ideal behavioural model as the one shown in Fig 2.8 b). As shown in the figure, this model includes also the effect of KT/C noise of the sampling capacitor and

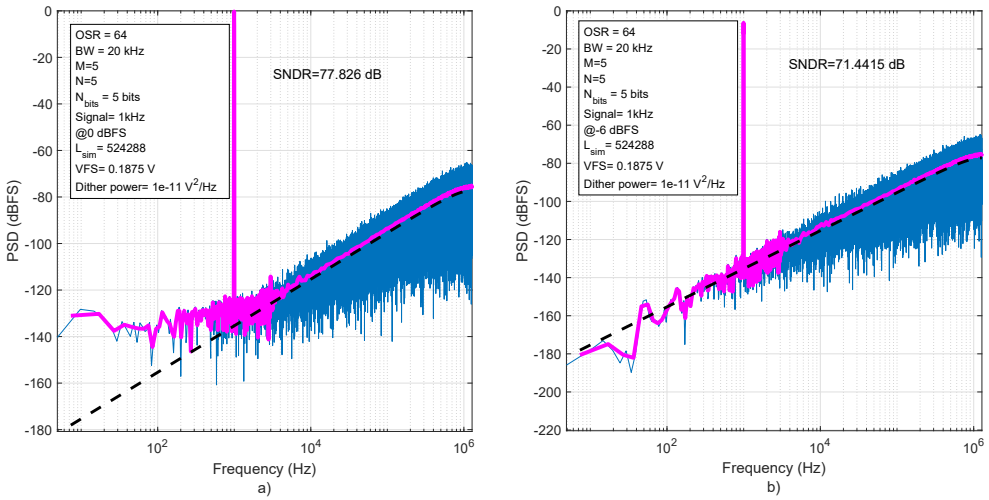

FIGURE 2.10: PSD of the output of the NSQ simulated using the behavioural model of Fig. 2.8 b) with a 0dBV input signal b) with a -6dBV input signal

the limited gain in the amplifier. These circuit impairments are used later. The simulation has been done for a 5 bits DAC. Thus the number of cycles in Phase I and Phase II is 5 in both, and the total number of cycles during a sampling period is 10. For the simulation an audio bandwidth of 20kHz has been chosen, with an oversampling ratio of 64. The sampling frequency is set to 2.56MHz, which requires a clock of 25.6 MHz. The full scale has been set using equation 2.16. The simulation shows that above 0 dB input amplitude, the SNDR falls sharply. This is due NSQ being saturated, as the input amplitude is higher than the maximum stable amplitude.

The PSD of the output data in two points, 0dB and -6dB input amplitude, is plot in Fig 2.10. In blue the FFT of the output data using a hanning window is plotted. Pink shows the smoothed FFT, while in black the noise transfer function is plotted.

In order to analyze the circuit impairments, the thermal noise contributed by the sampling capacitor and the effects of limited gain in the operational amplifier have been added to the behavioural model of Fig 2.8. To model these circuit limitations, the approach shown in [26] has been used. From a simulation for a OSR=64, BW=20kHz and 5 bits quantizer with the aforementioned impairments the DR plotted in Fig 2.11 have been obtained. The thermal noise used in this simulation is the one given by a 2pF sampling capacitor. Two DRs are shown in Fig 2.11. The blue line, shows the DR obtained for an operational amplifier with 90dB gain. The results for this gain are very close to the ideal DR shown in Fig 2.9. The red line show the DR for an operational amplifier with a 70dB gain. The peak SNDR for this case is 3 dB lower. The integrating capacitor, C_{SAR} has been

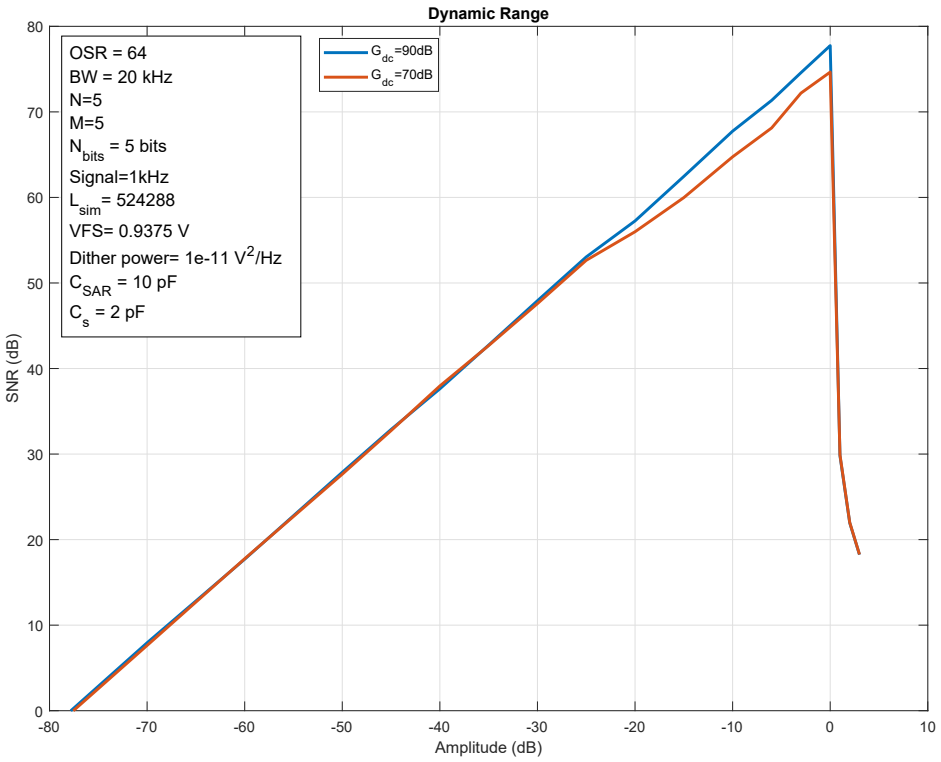

FIGURE 2.11: Simulated dynamic range of the SAR-NSQ including the effects of thermal noise in the 2pF sampling capacitor and the effects of limited gain in the amplifier G_{dc}. Blue line shows the results with an $G_{dc} = 90dB$ amplifier, while red line shows the results for a $G_{dc} = 70dB$ amplifier.

chosen to have the required gain following:

$$C_{SAR} = M \cdot C_s \tag{2.17}$$

The PSDs for the two cases plotted in Fig 2.11 are shown in Fig 2.12. The input tone used for these simulations is -6dBV amplitude. Fig 2.12 a) shows the PSD for the case of an operational amplifier with a gain of only 70 dB, showing multiple odd harmonics. The PSD for the case of an amplifier with 90 dB of gain is shown in Fig 2.12 b). In this case only the 3^{rd} harmonic is present (Although at closer look fifth harmonic can also be observed). Thus the SNDR for this case is 3dB above, and close to the ideal achievable SNDR shown in Fig 2.10 b).

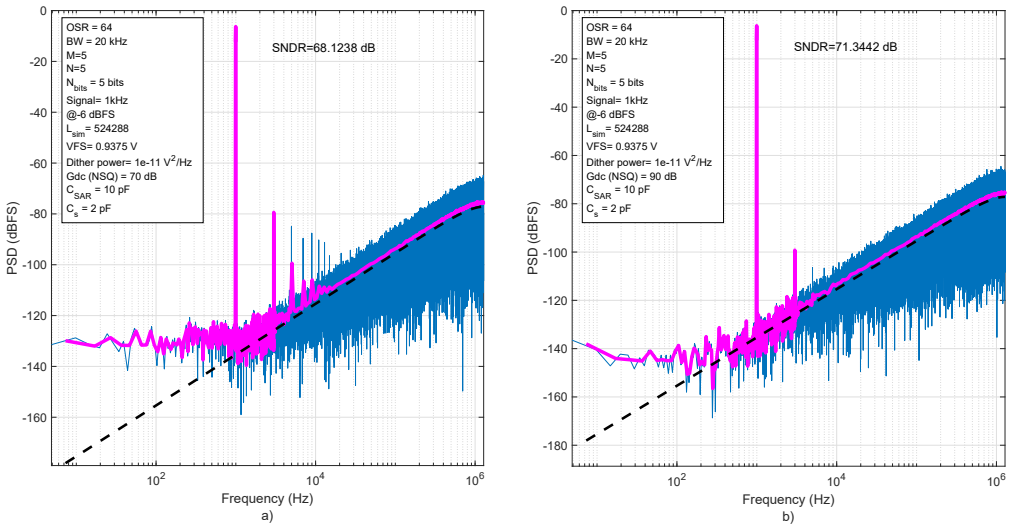

FIGURE 2.12: PSD of the output of the NSQ simulated with 2pF sampling capacitor noise and a) 70dB amplifier gain b) 90 dB amplifier gain.

2.3 First order noise-shaping filter plus SAR noise-shaping quantizer

In order to increase the resolution of the converter, or to reduce the clock frequency, the order can be increase. A second order delta-sigma can be implemented by placing an integrator before the NSQ.

The block diagram of the proposed second order multibit delta-sigma converter is shown in Fig. 2.13. The integrating SAR noise shaped quantizer is shown inside a dashed line. A second order Sigma-Delta modulator is realized placing a single integrator before the integrating SAR noise-shaping quantizer. In this configuration, the signal used to discharge the integrator in the quantizer is used as a feedback signal for the Sigma-Delta modulator, as it contains the information of the quantization error. This provides second order noise shaping following next equation:

$$Y(z) = X(z)(1 - z^{-1})^{-1} + Q(z)(1 - z^{-1})^2 \tag{2.18}$$

where $Y(z)$, $X(z)$ and $Q(z)$ represents the z-transform signal of the output D_{out}, the input V_{in} and the quantization error respectively. In a second order sigma-delta the full scale is set by the DAC. In the case of the integrating SAR noise shaped quantizer of Fig 2.13 The DAC is only activated during Phase II, which last for N clock cycles. Thus to correctly set the full scale of the ADC, gain G of Fig.2.13 must be equal to $G = 1 + M/N$.

Figure 2.14 a) shows the simulated dynamic range obtained from a behavioural model of the converter of Fig2.13. This simulation includes the effect of KT/C

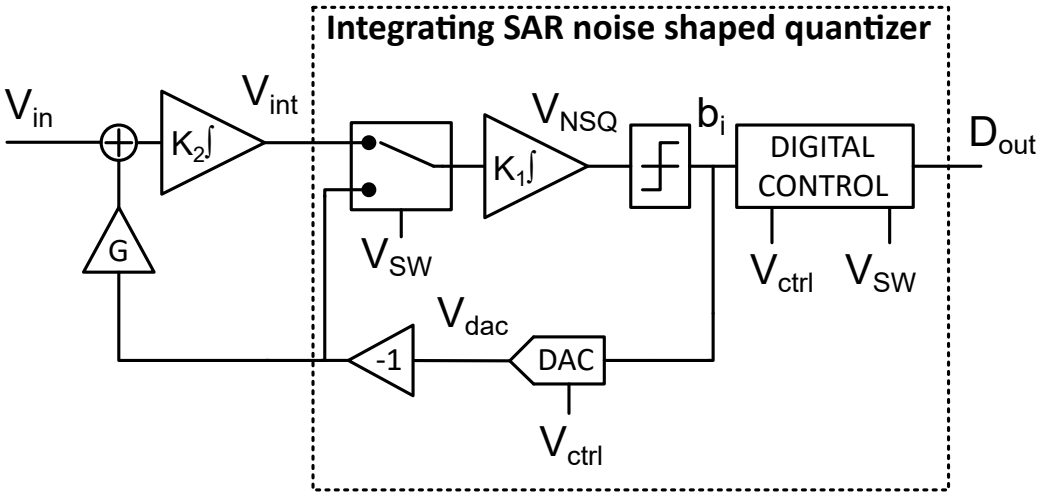

FIGURE 2.13: Schematic of the first order noise-shaping filter plus SAR-NSQ.

noise in both integrators, K_1 and K_2, and the effect of limited gain in the amplifiers. The gain of the NSQ integrator, K_1, and the gain of the integrator, K_2, are given by the following expressions:

$$K_1 = \frac{C_{S_{NSQ}}}{C_{SAR}} = \frac{1}{M} \tag{2.19}$$

$$K_2 = \frac{C_{S_{INT}}}{C_{INT}} = \frac{1}{M+N} \tag{2.20}$$

The KT/C noise of capacitor $C_{s_{INT}}$ dominates, as it is added outside of the loop, but KT/C noise from capacitor $C_{S_{NSQ}}$ is also modeled. The gain of the amplifier in the NSQ is $G_{dc}(NSQ)$, while the gain of the amplifier in the integrator is $G_{dc}(INT)$. An OSR of 64 and 3 bits have been used to convert a signal with a $20kHz$ bandwidth. The sampling frequency is, f_s is $2.56MHz$ making the required clock to be $15.36MHz$. The peak SNDR is above $80dB$ even with a $70dB$ gain amplifier in the integrator. The PSDs for a $-6dBV$ input signal and $90dB$ gain in the amplifier of the integrator and $70dB$ gain in the amplifier of the NSQ are shown in fig.2.14 b). It can be seen that the noise is shaped with a 40dB/decade slope.

2.4 Second order noise-shaping filter plus SAR noise-shaping quantizer

The order of the noise shaping can be increased even more by placing a higher order filter before the NSQ. In this section a third order sigma-delta converter using a second order loop filter and the NSQ will be analyzed.

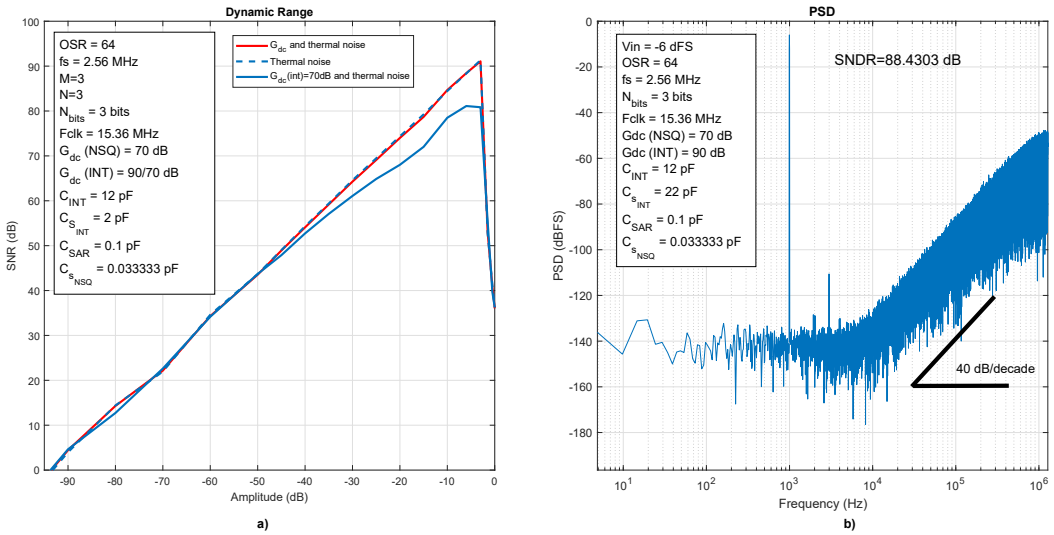

FIGURE 2.14: a) Dynamic range of the second order dual-slope ADC with binary weighted DAC and circuit impairments. b) PSD for -6 dBFS, 90dB gain in the amplifier of the integrator and 70 dB gain in the amplifier of the NSQ.

While the use of the SAR-NSQ together with a first order sigma-delta filter to achieve a total second order as shown in the previous section is straightforward (once the right gain in the feedback branch has been set), using a higher order in the filter require a careful design to ensure stability. Two main topologies are used to design loop filters in sigma-delta converters, cascade-of-integrator feedback (CIFB) and cascade-of-integrator feedfordward (CIFF).

The CIFB topology requires a feedback path and a DAC to each integrator of the loop filter, while the CIFF requires a single feedback path and a DAC to the first integrator. In the later topology, the output of each integrator is feed to the quantizer's input, where all the feedfordward paths are added together. Thus and adder before the quantizer is needed.

The NSQ can perform the addition operation, thus it is interesting to use it with a CIFF topology. Figure 2.15 a) shows the topology of a third order sigma-delta converter using a second order CIFF filter plus the SAR-NSQ. The first step to implement this topology is to design the NTF, from the linearized model shown in Fig. 2.15 b). For this purpose any of the available tools to design NTFs can be used. After that, the coefficients shown in Fig.2.15 can be calculated using the following expression:

$$NTF(z) = \frac{z^3 - 3z^2 + 3z - 1}{z^3 + (G_2 - 3)z^2 + (3 - 2G_2 + c_1a_1G_1)z + (G_2 - 1 + c_1c_2a_2G_1 - c_1a_1G_1)} \tag{2.21}$$

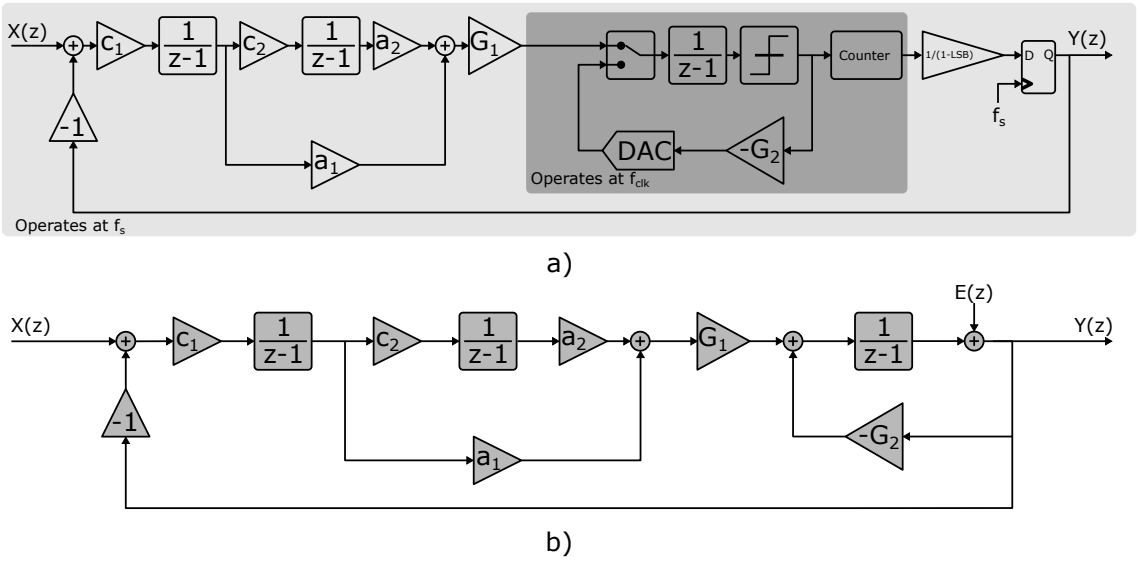

FIGURE 2.15: a) Block diagram of the SAR-NSQ plus 2^{nd} order CIFF filter. b) Equivalent linear model of the SAR-NSQ plus 2^{nd} order CIFF filter used to calculate the NTF.

Notice that in Fig. 2.15 a) two clock domains are present (Red and blue). The clock rates are the f_s (Red) and f_{clk} (Blue), which are related as explained in section 2.2 ($T_s = (M+N)T_{CLK}$).

A system level simulation of the topology of Fig. 2.15 has been performed. Figure. 2.16 a) shows the pole-zero map of the second order filter placed before the NSQ. The pole-zero map of the overall NTF, including the second-order filter and the NSQ, is shown in Fig.2.16 b). The NTF(z) for this particular case is given by:

$$NTF(z) = \frac{1}{M}\frac{z^3 - 3z^2 + 3z - 1}{z^3 + 2z^2 + 1.448z - 0.3628} \tag{2.22}$$

With M=3 and using the coefficients shown in the following table:

TABLE 2.1: Values of the coefficients used for the second-order plus SAR-NSQ design

Coefficient	**Value**	**Coefficient**	**Value)**
a1	1.2701	a2	1.3536
c1	0.3529	c2	0.1788
G1	(1-LSB)/M	G2	1

Notice that the gain in the feedback of the NSQ has been set to 1. This has been done to facilitate the scaling of the gains in the filter loop to guarantee that

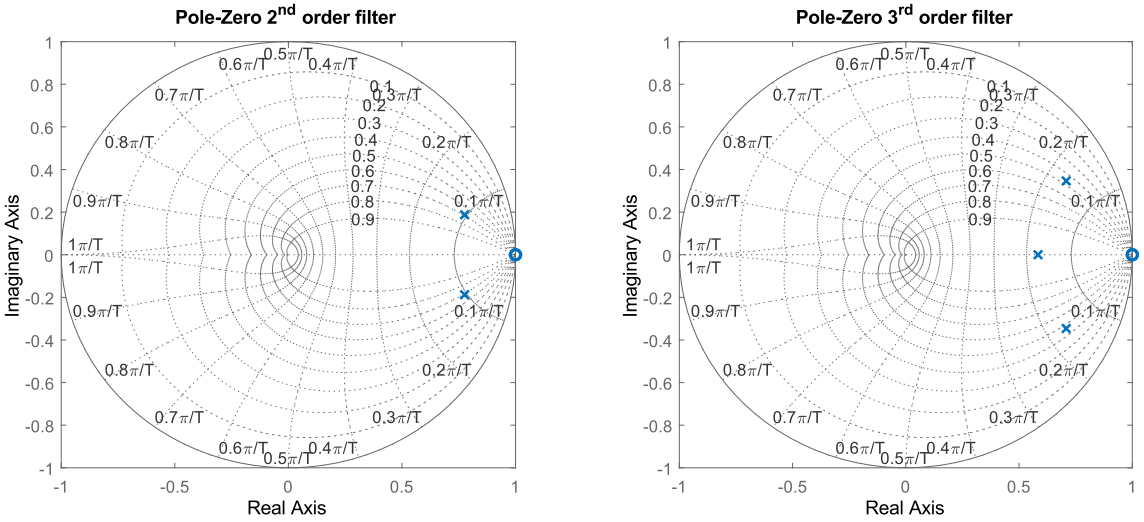

FIGURE 2.16: a) Pole-zero map of the second order CIFF filter. b) Pole-zero map of the third order delta-sigma (second order CIFF filter plus NSQ)

the signals always fall within the dynamic range of the NSQ. This limits how aggressive the NTF can be and thus the achievable SNR. Nevertheless, with proper scaling of the state variables, more aggressive NTFs can be implemented.

Results of an ideal system level simulation are shown in Fig.2.17. The PSD for a -6dBS is shown in Fig.2.17 a). The raw result of the FFT is shown in blue, while the pink line shows this results after being processed to smooth the line. The black line overlays the theoretical NTF of equation 2.22 over the simulation results. This shows a good matching between the simulation results and the designed NTF.

In Fig.2.17 b) the dynamic range obtained from the aforementioned simulations is plotted. The maximum SNDR reaches in this case 100dB at -3dBV. The number of bits used in this design is 3, with an OSR of 64 and a 20kHz bandwidth. The sampling frequency, f_s, is 2.56MHz and the clock frequency is 15.36MHz.

2.5 Conclusions

In this chapter topologies of Sigma-Delta converters using a NSQ have been analyzed. The analysis has focused mostly in the system level design of these type of Sigma-delta converters and its equivalence to conventional Sigma-Delta converters. The effect of thermal noise in the sampling capacitor and limited gain in the amplifiers have been also analyzed for some of the topologies.

Compared with dual-slope converters with noise shaping, the use of a multibit DAC in the feedback branch of the NSQ allows for a reduction of the necessary clock frequency for the same number of bits of resolution. The fact that the NSQ

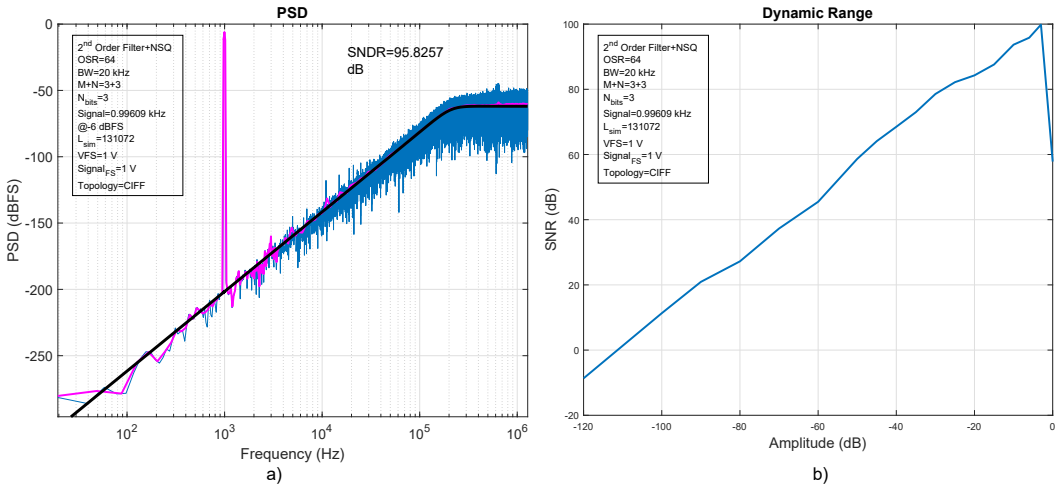

FIGURE 2.17: a) Simulated PSD with a -6dBFS input tone. b) Simulated dynamic range with a 1kHz input tone.

can perform the add operation without the need of further hardware, makes this type of noise-shaping quantizer interesting to implement CIFF topologies.

Chapter 3

VCO-ADC architectures for high impedance MEMS sensors

In chapter 1 the concept of a VCO-ADC was introduced. This family of converters make use of time-encoding instead of voltage-encoding techniques, making their implementation at lower supply voltages easier. Furthermore, the VCO can be implemented with CMOS inverters functioning as the delay cells of a ring oscillator (R0). This enables a mostly digital implementation of the ADC, which is desirable when working in submicron CMOS nodes. Finally, VCO-ADCs show first order noise shaping. These characteristics make VCO-ADCs an attractive choice to implement converters in submicron CMOS nodes. In this chapter we will review the main aspects related with the design of VCO based ADCs.

Due to the implementation of the VCO as a ring oscillator, we will be referring them as RO-ADCs for the rest of the chapter. There is another reason for this. As the RO can be controlled by either current of voltage, the use of RO-ADC is more general than VCO-ADC.

3.1 The RO-ADC as a first order sigma delta modulator

The basic structure of an RO-ADC was shown in Fig 1.10. This structure is known as open-loop RO-ADC as there is no feedback. Despite of the lack of feedback the open-loop RO-ADC shows first order noise-shaping of the quantization noise.

Figure 3.1 is useful to understand why this converter shows noise-shaping properties. In Fig 3.1 the RO is modeled as an integrator that integrates the frequency. As the frequency is the derivative of the phase, the output of the integrator is thus the phase. After the integrator the phase is quantized. The quantized phase, ϕ_q is then sampled and first differentiated. The signal, ϕ_q is given by [27]:

$$\phi_q[n] = \omega_0 n T_s + k_{RO} \int_{-\infty}^{nT_s} x(t)\, dt \; + q[n] \tag{3.1}$$

The output, $Y(n)$ is obtained by performing the first difference to $\phi_q[n]$ [27]:

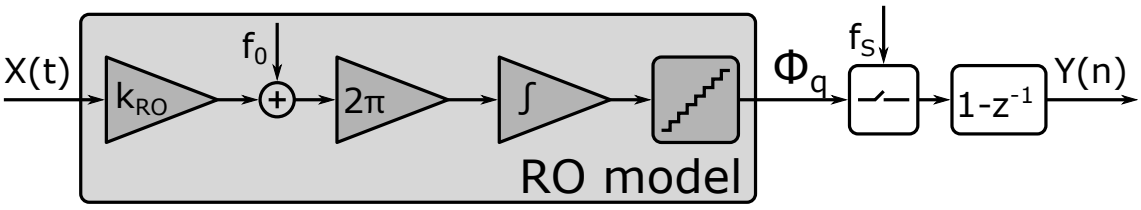

FIGURE 3.1: Ring oscillator based ADC

$$Y[n] = \omega_0 T_s + k_{RO} \int_{(n-1)T_s}^{nT_s} x(t)\, dt \; + q[n] - q[n-1] \tag{3.2}$$

The term $q[n] - q[n-1]$ accounts for the first order noise-shaping of the quantization noise as in (1.9). The reader should notice that (3.2) is similar to (1.17) obtained in Chapter 1. In the reasoning followed to derive (1.17) we considered the use of a counter to count the number of edges of the oscillator output square wave. We used then the number of edges during a fixed time period, the sampling period T_s, to determine the frequency of oscillation.

The obvious question now, is how is this counter represented in the model of Fig 3.1. At first glance, one might be tempted to consider that the counter is represented by the integrator because this counter is accumulating the number of edges of the oscillator. However, the integrator in Fig 3.1 is integrating the frequency of the oscillator, not the number of edges. That is, the output of the integrator is the phase of the oscillator as previously stated. This phase is then quantized by the following block. If we analyze what the counter in the model of Fig 1.10 does we can see that it is quantizing the phase of the oscillator. We previously stated that the counter counts the edges coming out of the oscillator. If we have an inverter-based RO, the output signal is a square wave with edges separated by π radians in phase.

A counter can be implemented to count rising edges, falling edges or both. If the counter counts either falling or rising edges it will behave like a phase quantizer with a quantizing step of 2π radians. If the counter is able to count both rising and falling edges, the resolution of the quantizer will be π radians. The quantizer in the model of Fig 3.1 performs a similar task. It quantizes the output phase of the oscillator with either a π or 2π radians resolution. The equivalence between the counter in Fig 1.10 and the quantizer in Fig 3.1 is shown in Fig 3.2. Figure 3.2 a) shows how the phase is quantized in steps of 2π radians by the quantizer in Fig 3.1, while Fig 3.2 b), shows how a sensitive to falling and rising edges counter quantizes the phase of the RO of Fig 1.10. As can bee seen the behaviour of the qunatizer and counter is similar.

From the previous discussion it can be seen that the resolution in phase of the quantizer of an RO-ADC can only by either π or 2π radians. This is true as long as we are counting the edges in one single square wave of the RO. But ROs are made connecting several delay stages one after the other forming a ring as

shown in Fig 3.3. Looking at the oscillator output signals ϕ_0, ϕ_1 and ϕ_2 in Fig 3.3 we see that they have a phase-shift equal to $\frac{2}{3}\pi$. If we count the both the rising and falling edges in every phase of the oscillator, the phase resolution of our quantizer will be $\frac{\pi}{3}$, or $\frac{2}{3}\pi$ if we only count either the falling or rising edges. The reader might note that if we count the edges in all the phases in the oscillator of Fig 3.3, the resulting value at the counter at the end of a sampling period will be the same that the one obtained counting the edges of a single output of an oscillator oscillating at three times the frequency. What this is telling us is that what sets the number of bits of our RO-ADC is the number of edges per second.

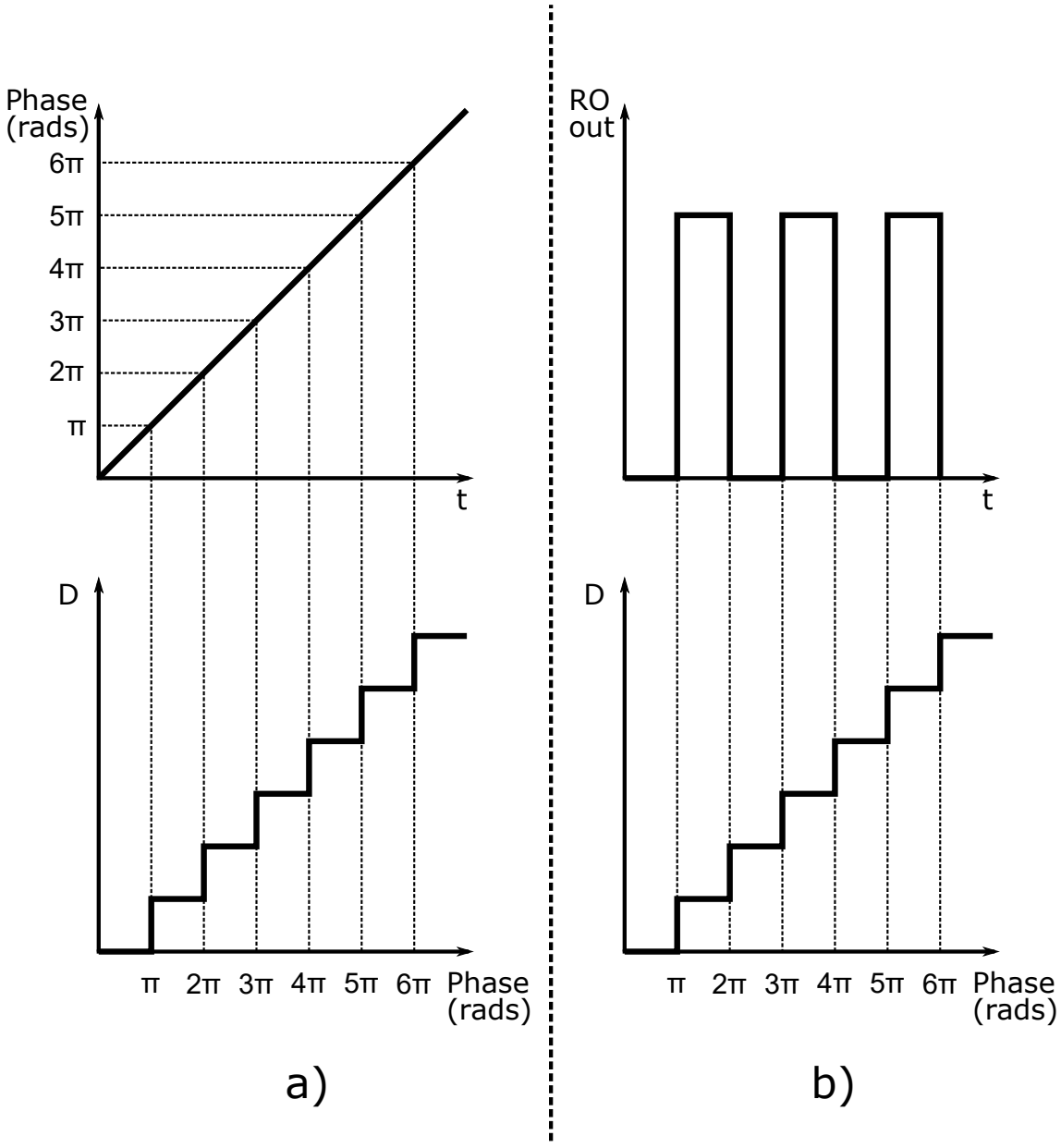

FIGURE 3.2: Equivalence between quantizer a) and counter b)

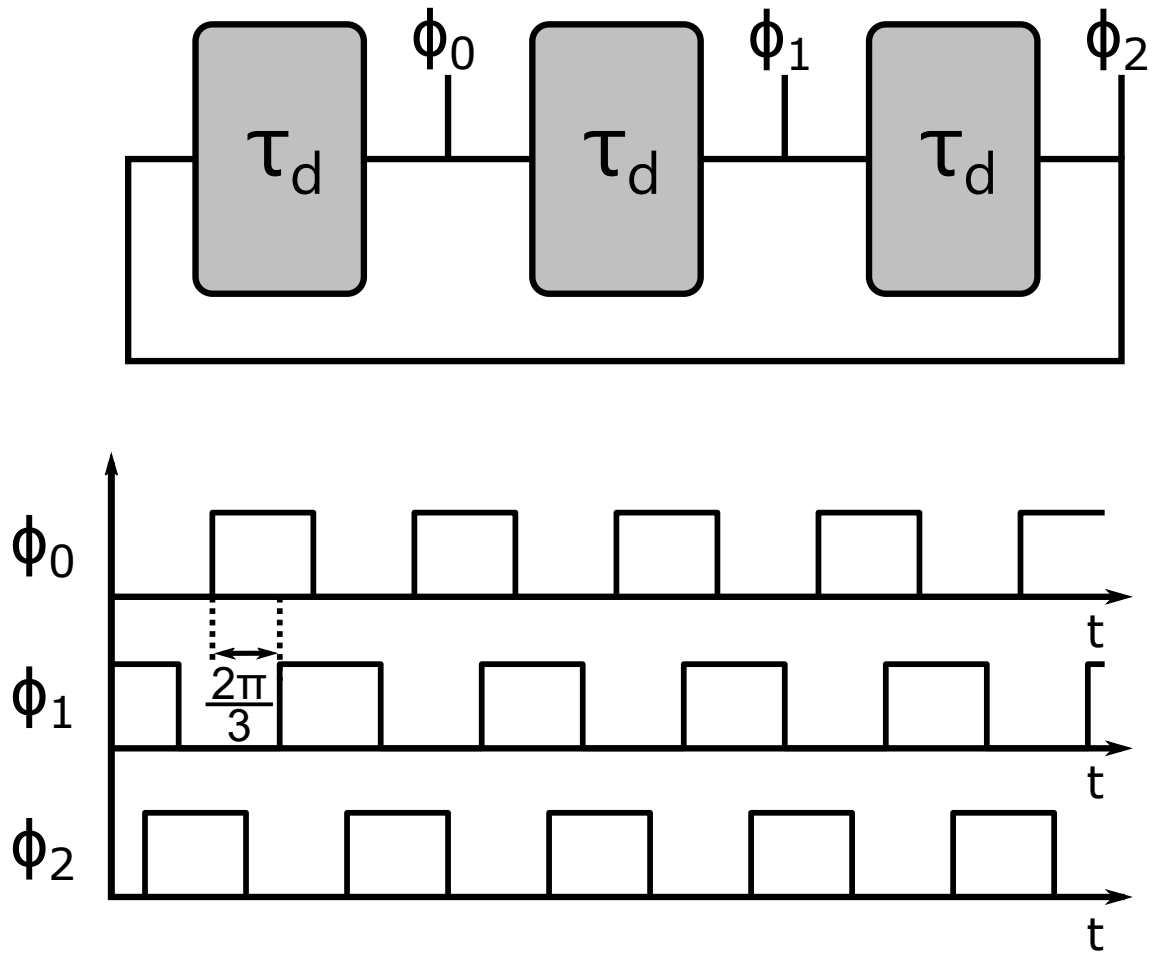

FIGURE 3.3: Phase of a ring oscillator with 3 delay cells.

After this explanation we are ready to understand the different design options to obtain a certain quantization noise in an RO-ADC. It is important to remember that RO-ADCs also performs first-order noise-shaping as Sigma-Delta modulators. Thus the performance of those converters must be analyzed using the SQNR. The SQNR of an RO-ADC is given by:

$$SQNR(dB) = 6\log_2\left(\frac{2f_0}{f_s}\right) + 1.76 - 5.17 + 30\log_{10}(OSR) \tag{3.3}$$

The first term on the right side of 3.3 accounts for the number of bits of the RO-ADC, given by the ratio between the frequency swing of the oscillator, $2f_0$, and the sampling frequency, f_s. The reader should remember that we have called RO-ADCS time-encode converters. The reason for it is clear here. In this term, the sampling time is equivalent to the full-scale voltage, V_{FS}, of a flash converter, while the the inverse of the frequency swing is equivalent to the least significant bit, V_{LSB}. The other terms in the right side of 3.3 accounts for the increase of the SQNR due to first order noise-shaping.

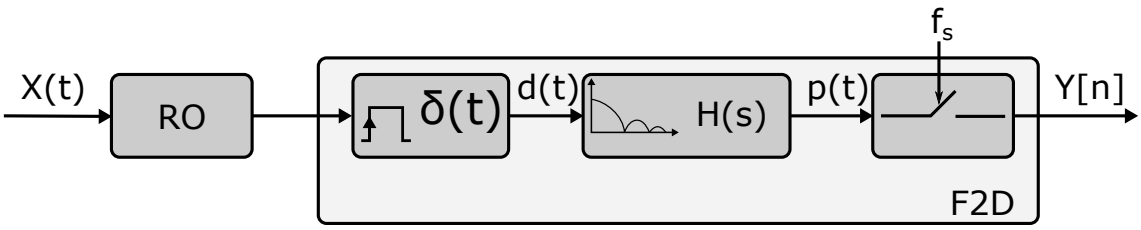

FIGURE 3.4: PFM model of the RO-ADC

Lately, PFM theory has been used to analyze RO-ADCs, [17], [18]. This new approach was mentioned in Section 1.3.3 of the present document. While the previously discussed analysis of RO-ADCs is similar to the Sigma-Delta theory and makes use of statistical assumptions about the nature of quantization noise, PFM theory based analysis allows for a precise calculation of the spectral content of the output signal of the RO-ADC. This is done with the use of mathematical expressions and without requiring to make any statistical assumption.

According to this approach the RO behaves as a PFM modulator. Figure 3.4 shows a RO-ADC modeled using the PFM based approach. Under this approach the counter and first difference of Fig 1.10 are modelled as an edge detector followed by a pulse-shaping filter and a sampler. The output Y[n] in Fig 3.4 is equivalent to Y[n] of Fig 1.10.

If we analyze the spectrum of a PFM signal, we see that it contains the signal component, the harmonics of the oscillation frequency and its sidebands. In Fig 3.4 signal d(t), at the output of the edge detector, is a PFM signal. Mathematically, the spectrum of d(t) is given by [18]:

$$D(f) = f_0\delta(f) + \frac{Ak_{RO}}{2}(\delta(f+f_x) + \delta(f-f_x)) + \\ + f_0 \sum_{q=1}^{\infty}\sum_{r=-\infty}^{\infty} J_r\left(\frac{qAK_{RO}}{f_x}\right)\left(1+\frac{rf_x}{qf_0}\right)(\delta(f+(qf_0+rf_x)) + \delta(f-(qf_0+rf_x))) \tag{3.4}$$

After the edge detector, signal d(t) is filtered by the pulse-shaping filter. The frequency response of the pulse-shaping filter is given by the following expression:

$$H(s) = \frac{(1-e^{-sT_s})}{sT_s} \tag{3.5}$$

It is clear form equation 3.5 that the pulse-shaping filter is a sinc filter. The null of the sinc in the pulse-shaping filter fall in multiples of the sampling frequency, f_s. The output of the filter is p(t). This signal is then sampled with a frequency f_s. The output of the RO-ADC is Y[n], the output of the sampler. According to

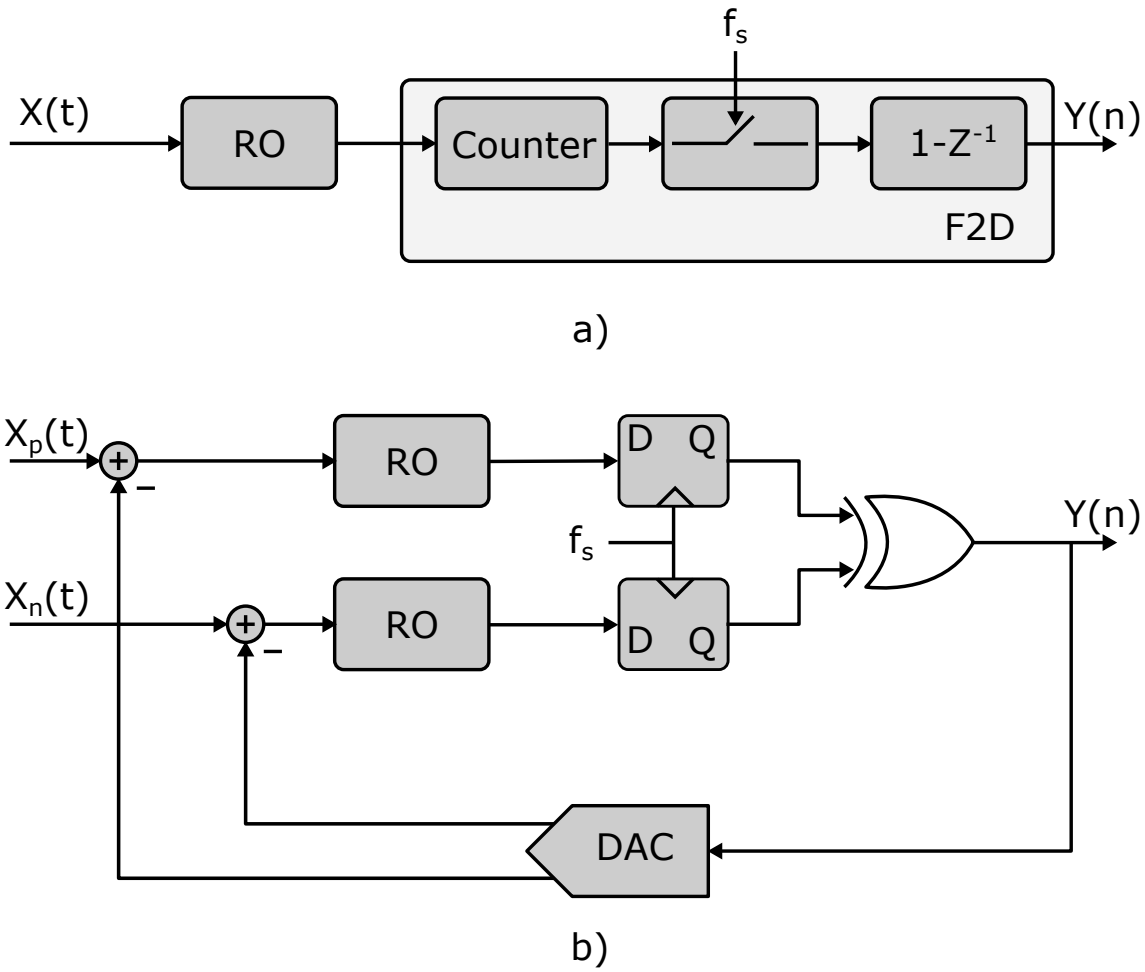

FIGURE 3.5: a) Open-loop RO-ADC architecture. b) Closed-loop RO-ADC architecture.

the PFM model, the quantization noise comes from the aliasing of the modulation sidebands of (3.4) filtered by $H(f)$. This mean that the spectral behaviour of the quantization noise can be obtained from (3.4) and (3.5), for different input frequencies and amplitudes. Another important take away of this model is that aside from the effect of aliasing, part of the first sideband falls in the signal bandwidth, imposing a fundamental SNR limit, depending on the input amplitude and frequency.

3.2 Open-loop and closed-loop VCO-ADC architectures

Until now the discussion about RO-ADC has focused on the open-loop RO-ADC architecture. The structure of the RO-ADC described in Section 3.1 is the basic

open-loop RO-ADC architecture, as no feedback of the sampled output digital value is present. As demonstrated in the aforementioned section, this open-loop structure behaves like a first order Sigma-Selta modulator. An alternative to this architecture is the closed-loop RO-ADC [28]–[31]. Figure 3.5 shows both architectures for comparison. As it can be seen the closed-loop architecture (Fig 3.5 b)) has a feedback-loop with a DAC.

Similarly to the open-loop topology, the closed-loop topology has first order noise-shaping. The reader should notice that by closing the loop, no extra order of noise-shaping is achieved. There are ways to increase the order of noise-shaping in a closed-loop topology. One option is to use the RO-ADC as the quantizer in a conventional sigma-delta loop [32]–[35], using a similar approach that the one described in Chapter 2 of this document. Other approach consist on using an input open-loop RO-ADC to control one or more digitally-controlled ring-oscillators, DCO, around which a feedback loop is built. Both of these approaches have drawbacks. In the former approach, the mostly digital nature of the RO-ADC is lost, as analog integrators are needed, while in the later, the input RO-ADC is left outside the feedback loop, its non-linearity uncompensated. As no extra order of noise-shaping is obtained, the interest for this architecture stems from their compensation of the non-linear behaviour of the oscillators. This inherent non-linearity and the use of this architecture to compensate it will be disscused in more detail later in this chapter.

3.3 Circuit implementation of open-loop VCO-ADC architectures

As previously described, RO-ADCs are implemented using several blocks, which are, a ring oscillator (RO) and a frequency-to digital-converter (F2D). Aside from this, an analog input front-end that drives the RO is also needed.

The ROs used in RO-ADCs can be single-ended or differential. Single-ended ROs must have an odd number of stages while differential can have even or odd number of stages. Both types of ROs are shown in Fig 3.6. The delay cells in each type of oscillator are also implemented differently. In the case of single-ended oscillators the delay cells are implemented with CMOS inverters.

Differential oscillators are implemented using differential delay cells [36]. These differential delay cells are implemented using a differential pair and a RC load as shown in Fig 3.7 a). Each of those delay cells are connected in a chain, forming a ring, so the capacitance in the RC load is the input capacitance of the next differential stage. Delay cells in ROs can also be implemented using CMOS inverters. Usually the type of the delay cell is chosen depending on the application. Differential pair based cells are usually used in RF applications, while CMOS cells are commonly used for sensor applications. Fig 3.7 b) shows a differential delay cell implemented using four CMOS inverters [36]. This delay cell have the advantage

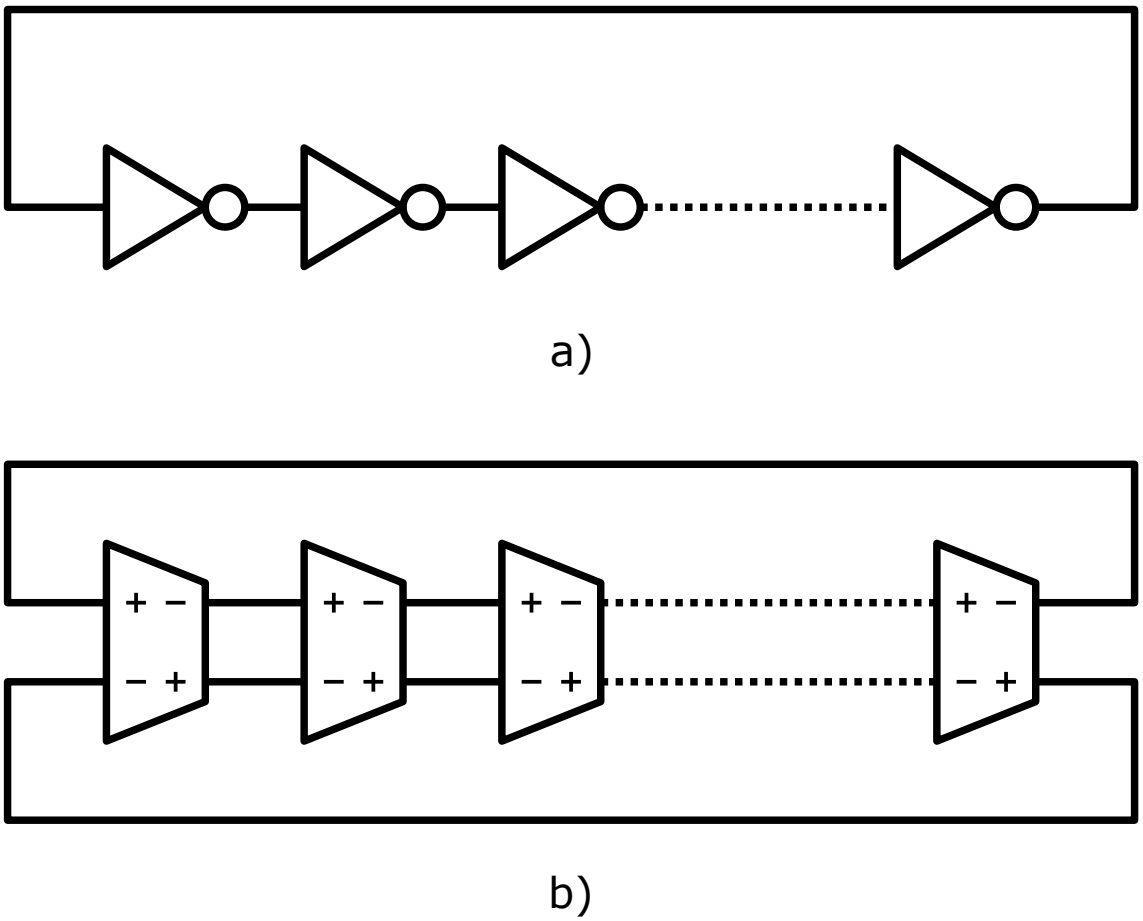

FIGURE 3.6: a) Single-ended inverter-base ring oscillator. b) Differential ring oscillator

of making use of only digital circuits for its implementation, keeping the digital nature of RO-ADCs. Nevertheless, this cell has some drawbacks. First, the cross coupling inverters add a capacitive load to the cell without increasing their driving capacitance. This reduces f_0 compared with a single-ended inverter based RO. Secondly, during the transition, the transistors of the cross-coupled inverters are in the triode zone, which worsen the noise performance of the oscillator [37]. An improvement over this inverter based delay cell is the feed-forward differential delay cell (Fig 3.7 c) and d)) [37]. Implemented also using CMOS inverters the auxiliary inverters in this delay-cell are connected to the input of the previous stage. The auxiliary inverters in the feed-forward delay cell pre-charge the outup of the cell, increasing f_0 without increasing consumption. It also shows better noise performance than the direct cross-coupled delay cell [37]. In this dissertation we will focus on single-ended inverter based RO [38] due to its better noise efficiency.

After the description of the types of oscillators and the delay cells that can be used to implement RO-ADCs has been finished, the other two main blocks need

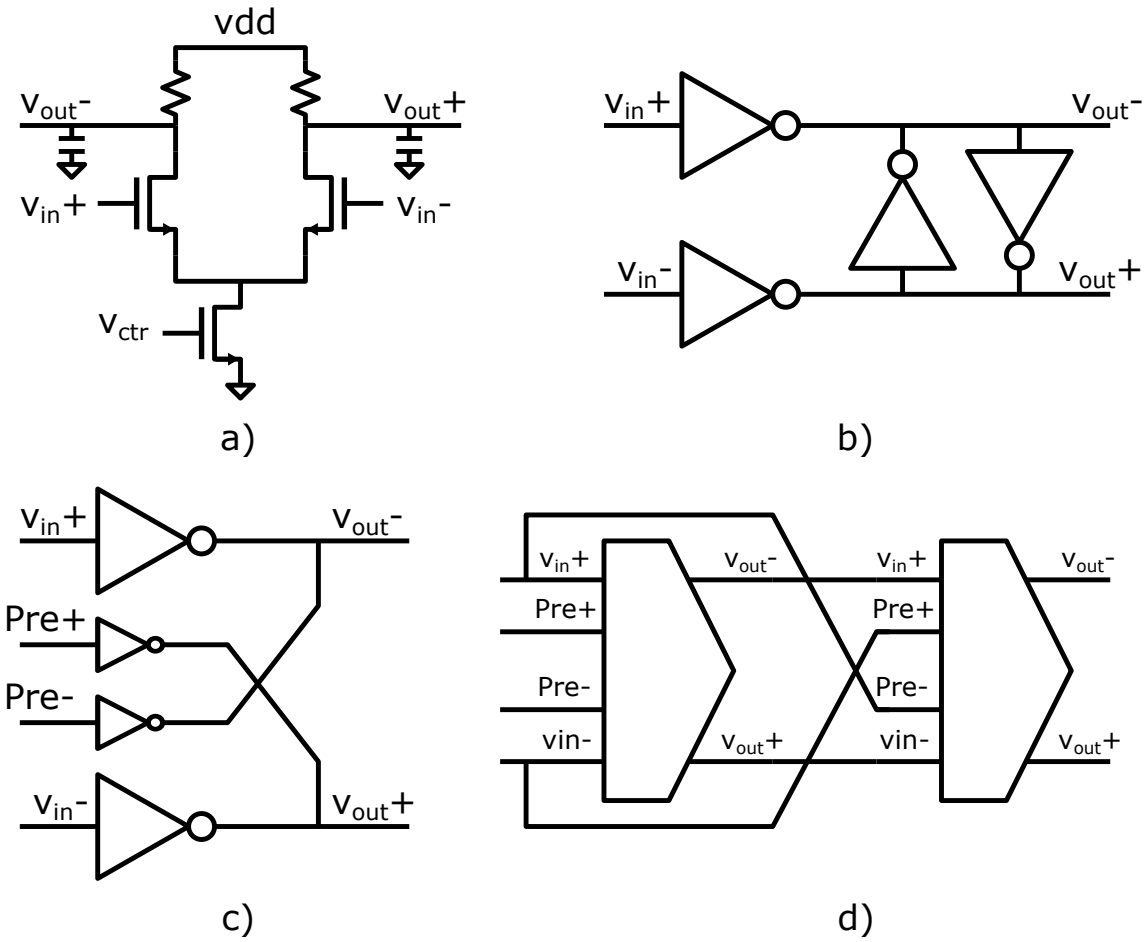

FIGURE 3.7: Delay cells for differential ring oscillators. a) Differential and RC based delay cell. b) Inverter based differential delay cell. c) Feed-forward inverter-based differential delay cell. d) Connection of feed-forward inverter-based differential delay cells.

to be explained. The analog input front-end will be described in more detail in the following chapter. Suffice to say here that this block is needed to generate the driving voltage or current in the oscillator, and to provide the necessary input impedance of the ADC. Thus we will focus now on describing the different ways to implement the frequency-to-digital converter.

3.3.1 Frequency-to-Digital conversion block: XOR decoder, coarse-fine decoder.

The frequency-to-digital converter (F2D) is the block that makes the RO-ADC. The RO is just an oscillator that encodes the input current or voltage into a frequency, but the conversion into a digital value is done in the frequency-to-digital converter. Following the phase approach to understand RO-ADCs described in

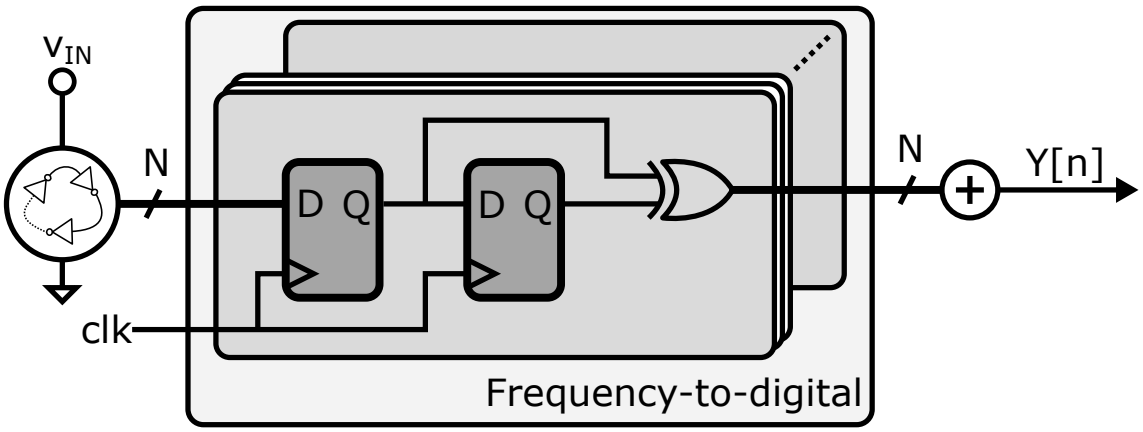

FIGURE 3.8: XOR decoder for frequency-to-digital conversion

Section 3.1, where the oscillator is seen as a phase integrator, the frequency-to-digital converter behaves like the quantizer of a Sigma-Delta modulator. Is in this block where the quantization noise is added.

But, attending to the PFM based theory for RO-ADCs, it can be observed that the frequency-to-digital converter does more than that. Is in the frequency-to-digital converter where the frequency modulated, FM, signal coming out of the oscillator is converted into a PFM signal and then sampled. Under this approach, is the frequency-to-digital converter and not the oscillator the responsible for the noise-shaping behaviour of RO-ADCs. It is also responsible for the inherent sinc filter of RO-ADCs (see Fig 3.4).

Two ways to implement the frequency-to-digital converter can be found in the literature, the XOR based decoder and the counter based F2D. The XOR based decoder is shown in Fig 3.8. It is composed of two flip-flops and an XOR gate hence its name. A decoder is connected to each of the phases of the oscillator, and the outputs of each decoder are added to obtain the digital word that represents the ADC analog input.

This circuit is often described as a phase sampler and differentiator, as the one shown in Fig 3.1. The first flip-flop serves here as a 1 bit counter, while the XOR performs the first difference of the phase. This circuit can also be understood as a PFM modulator plus sampler. The process of generating the PFM modulation and sampling is done in a single step in the circuit, and thus no PFM signal can be observed. The flip-flops sample, and at the same time the XOR generates a pulse when each flip-flop has a different value, i.e. when a rising or falling edge has happened in the oscillator output during the sampling period. The output signal is thus the same that would be obtained from a sampled PFM signal generated by an edge detector from the oscillator output, and thus has the same spectrum, i.e, a spectrum with first order noise shaping as explained in section 3.1.

As the XOR based decoder is similar to a 1 bit counter that is then sampled and first differentiated, a limitation to sampling frequency required is present.

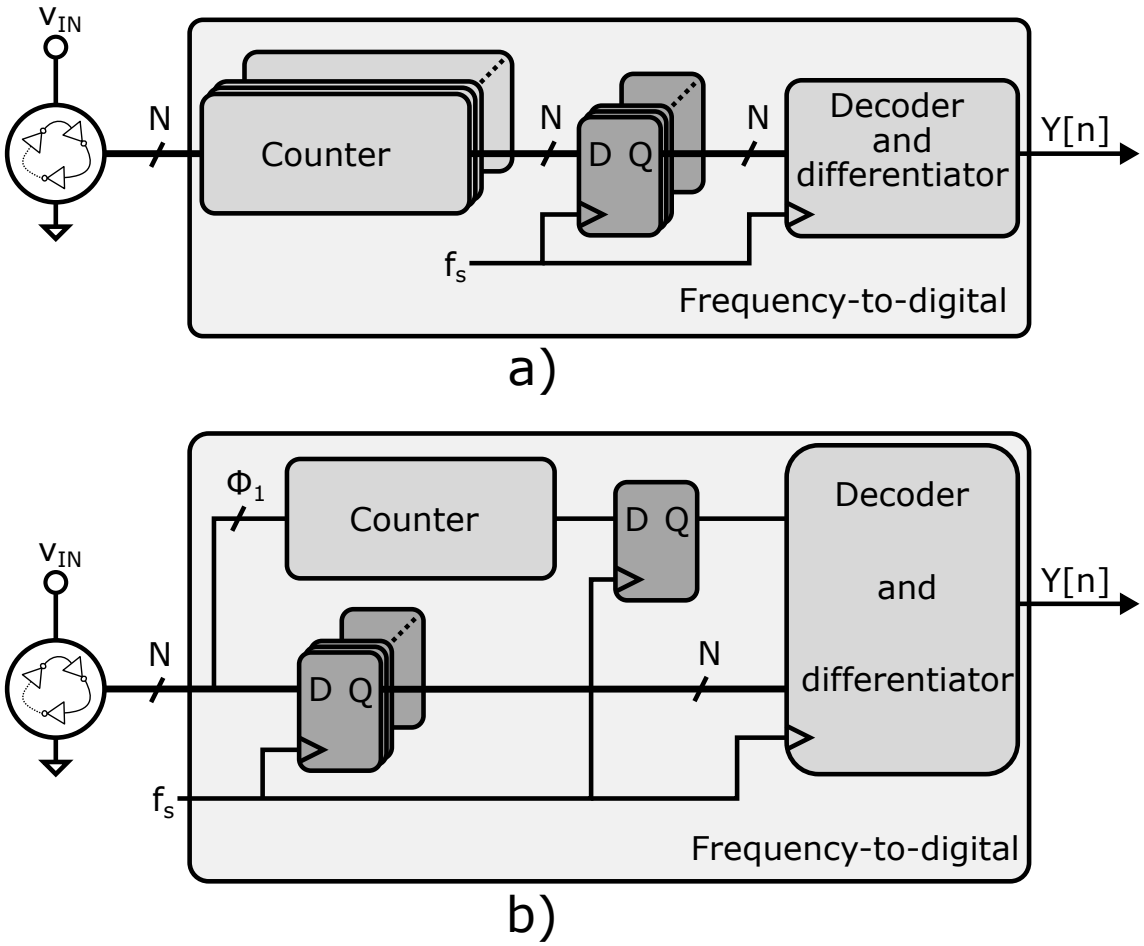

FIGURE 3.9: Counter based frequency-to-digital converters. a) Basic counter based frequency-to-digital converter. b) Coarse-fine architecture for frequency-to-digital converters.

Assuming a normalized input of 1 and a normalized oscillator gain, $k_d = \frac{k_{RO}}{f_0}$, of 1 also, the sampling frequency, f_s must be four times the oscillator frequency, f_0.

As has been said before (Fig 3.5) multi-bit counters can be used to implement the frequency-to-digital converter. The structure of a counter-based F2D is shown in Fig 3.9 a). In this architecture the counter counts the number of edges happening in each tap of the oscillator. Then this value is sampled by a register. Once sampled, the first difference is calculated in the block called decoder and differentiator. This block is also called decoder because the counter can count using a code different to binary code. If the counter is a binary counter, usually only the first difference needs to be performed, as we normally want the output value to be in binary code.

In Fig 3.9 a), a counter is connected to each tap of the oscillator. This can consume a lot of area and power. An alternative is to use a coarse-fine architecture [39]–[44]. The coarse-fine architecture is shown in Fig 3.9 b). This architecture

takes advantage of the fact that in the architecture of Fig 3.9 a) each counter has the same number plus or minus a one. Thank to this, a single counter, the coarse counter, can be connected to a reference tap of the oscillator, while the other taps are sampled. The decoder and differentiator calculates the final value multiplying the value of the coarse counter by the number of taps and using the info from the sampled phases to add the additional edges that have happened. This way only a single counter needs to be used, saving area and power. This type of F2D will be explained with more detail in chapter 4.

There are other ways to implement the frequency-to-digital converter, but they are not used as commonly. One way is to connect a delay line to a tap of the oscillator [45]. This delay line is implemented with a chain of CMOS inverters. The output of each inverter on the chain is then sampled and post-processed. Mismatch in the delays of the chain can lead to a bad performance, specially in long delay lines.

Other way to implement the frequency-to-digital converter is using monostables connected to one or several oscillator's outputs [46]. These monostables generate a pulse for each either rising or falling edge of the oscillator. These pulses generate a real PFM signal, equal to the signal p(t) in Fig 3.4. These signal is then sampled, and if several taps of the oscillator are connected to a similar structure, added together to obtain a multi-bit output signal. The delay of the monostable is difficult to control, and changes on it due to PVT can impact the performance of this circuit.

3.3.2 Ring oscillators. Linearity and Noise

The two main circuit limitations that impact the RO-ADC performance are the non-linear tuning curve and the phase noise. The non-linear tuning curve is considered one of the main weakness of RO based ADCs compared with Sigma-Delta ADCs. It imposes a limitation on the dynamic range of the converter.

Expression 1.15 assumed that the tuning curve of the oscillator is perfectly linear. In reality, the tuning curve of the oscillator is highly non-linear and has to be characterized by a polynomial:

$$f_{RO}(t) = f_0 + k_{RO}(X)X(t) \tag{3.6}$$

Figure 3.10 illustrates this problem. The normalized tuning curves of an oscillator controlled by voltage 3.10 a) and by current 3.10 b) are plotted. In Fig 3.10 a) and b) the Y axes have been normalized to the oscillator rest frequency, f_0, while the voltage in the X axis of Fig. 3.10 a) has been normalized to the oscillator bias voltage, V_{bias} (the one that generates f_0). Likewise, the current in 3.10 b) has been normalized to the bias current, I_{bias}, that makes the oscillator to oscillate at f_0.

Although, not completely evident by looking at the figures (the tuning curve seems quite linear in some regions to the bare eye), even in a small range of operation, compared with the full range show in Fig 3.10, the tuning curve is non-linear,

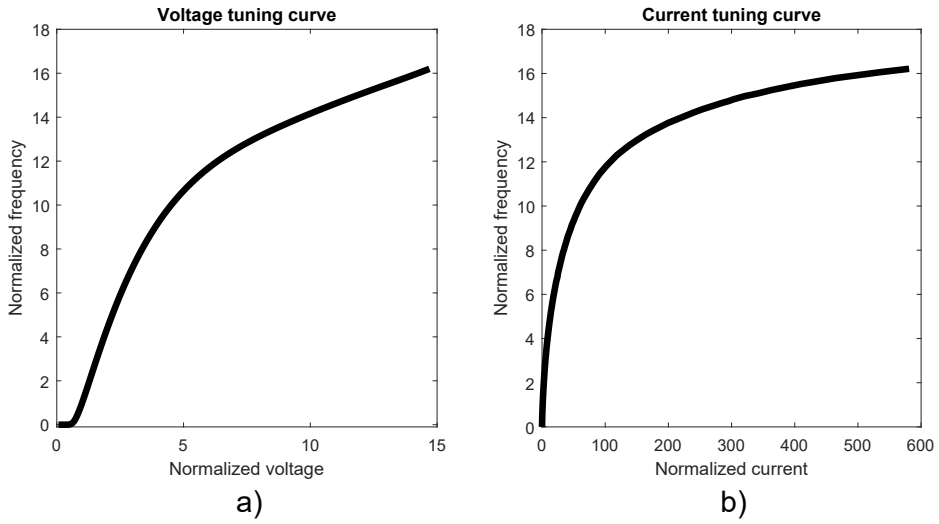

FIGURE 3.10: a) Normalized RO voltage tuning curve. b) Normalized RO current tuning curve.

for both a voltage controlled oscillator (VCO) and a current controlled oscillator (CCO). Furthermore, the non-linearity of the tuning curve is asymmetrical. This gives rise to both even and odd order harmonics, so, the non-linearity can not be fully compensated by simply implementing a differential (or pseudo-differential) circuit.

Other thing that can be deduced from Fig 3.10 is that the tuning curve of an oscillator controlled by voltage and the same oscillator controlled by current is not related by a real number. Recalling Ohm's law, we would expect the tuning curves to be related by:

$$R_{RO} = \frac{k_{CCO}(I)}{k_{VCO}(V)} \tag{3.7}$$

Where R_{RO} is the average resistance seem looking into the oscillator from the control pin. But instead of the relation given by 3.7, the resistance looking into the oscillator is given also by a polynomial. This is shown in Fig 3.11 a), where the normalized resistance (the average resistance looking into the oscillator divided by the average resistance at rest frequency) is plotted as a function of the oscillator frequency, in logarithmic scale in both edges. It can be seen that this resistance is not constant, but depends on the oscillator frequency. Furthermore, this dependence is highly non linear. Fig 3.11 b) shows a detail of the R_{RO} curve, focused on the normal region of operation (between $2f_0 =$ and $0.002f_0$). This plot shows the non-linear behavior of R_{RO} as a function of frequency, even in a small region. The relation between k_{CCO} and k_{VCO} is then given by:

$$R_{RO}(f) = \frac{k_{CCO}(I)}{k_{VCO}(V)} \tag{3.8}$$

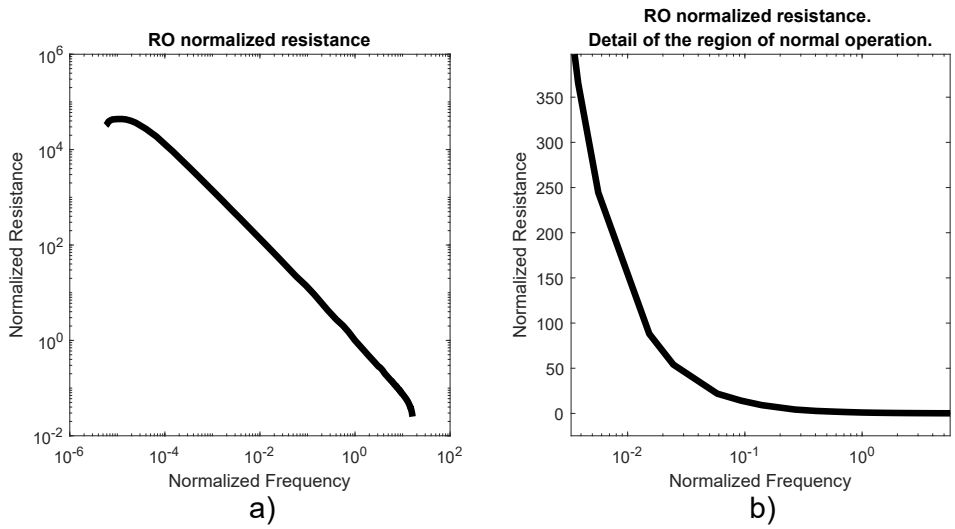

FIGURE 3.11: a) Normalized resistance looking into the RO. b) Normalized resistance looking into the RO in the normal operation region.

Where $R_{RO}(f)$ is the polynomial that can be approximated from a plot like the one of Fig 3.11 a). The non-linear behaviour of R_{RO} stems from the different behaviour of the voltage and current tuning curves (Fig 3.10).

The other element impacting the oscillator performance is noise. There are several noise sources present in ring oscillators. The two most prominent for RO-ADCs, specially those dedicated to convert audio signals, are thermal and flicker noise. The noise in oscillators has been studied in depth and design guidelines for low noise ring oscillators has been outlined [47]. The SSB phase noise due to thermal noise is given by the following expression [47]:

$$\mathcal{L}(f) = \frac{2kT}{I_{RO}} \left(\frac{(V_{RO} \cdot (\gamma_N + \gamma_P)) + V_{RO} - V_{th}}{V_{RO} \cdot (V_{RO} - v_{th})} \right) \left(\frac{f_0}{f} \right)^2 \tag{3.9}$$

Where I_{RO} is the current supplied to the ring oscillator, V_{RO} is the voltage of the RO, V_{th} is the threshold voltage of the transistors and γ is the noise factor of the transistor. The SSB phase noise due to flicker noise is given by [47]:

$$\mathcal{L}(f) = \frac{C_{ox}}{8 N_{RO} I_{RO}} \left(\frac{\mu_N K_{fN}}{L_N^2} + \frac{\mu_P K_{fP}}{L_P^2} \right) \left(\frac{f_0^2}{f^3} \right) \tag{3.10}$$

Where C_{ox} is transistor gate capacitance per unit area, N_{RO} is the number of taps in the RO, k_f is the flicker noise coefficient of the transistors and L is the length of the transistors. Expressions 3.9 and 3.10 give the phase noise at the output of the oscillator. When it comes to the design of RO-ADCs we are interested in how the phase noise compares with our input signal. Thus we need to refer

the noise to the input. A method to refer the oscillator phase noise to the input is given on [48]. The equation that refers the output phase noise to the input is [48]:

$$S_r(f) = \mathcal{L}(f)\frac{2 \cdot f^2}{k_{RO}^2} \tag{3.11}$$

When designing RO-ADC two parameters are key, rest frequency, f_0 and normalized gain, k_d. Remember that he normalized gain is given by:

$$k_d = \frac{k_{RO}}{f_0} \tag{3.12}$$

Both impact the quantization noise. When it comes to phase noise and linearity, the k_d is the most important. High k_d ring oscillators improve noise performance in the same manner that high gain amplifiers do. In the case of inverter-based ROs, high k_d requires short channel lengths in the transistors. So for a given f_0, the oscillator is biased with lower voltages, and thus in a less linear region (See Fig.3.10). Biasing the oscillator with a higher voltage, requires longer transistors, which in turn reduce k_d and the noise performance.

The way to drive the RO has also an impact in noise performance. Analyses have been done on noise performance of the different types of inverter based RO (i.e. single-ended, differential and differential feed-forward) under both current and voltage control modes[38]. According to these analysis, the more efficient implementation of an RO for low noise is the single-ended inverter-based RO, while the less efficient is the differential inverter-based RO.

Also, although equations 3.9 and 3.10 are independent of the control mode, the output noise for a CCO is reported to be somewhat lower. This is due to the fact that the driving current source is forcing a current through the PMOS transistor (or NMOS in the case of bottom drive configuration, when the control node is in the source of the NMOS transistor) which partially cancel the noise in this transistor, depending on the output resistance of the driving current source [38].

When considering the more efficient bias point for low noise, differences between CCOs and VCOs are also found. The more efficient bias point for a CCO is with high bias voltages (as high as possible before reaching velocity saturation), while the more efficient bias point for a VCO is with low bias voltages [38].

3.4 Nonlinearity mitigation techniques

One of the focuses of this dissertation is to investigate ways to mitigate the nonlinearity of RO-ADCs, specifically when used to implement digital microphones. Different techniques to correct the non-linear tuning curve of ROs has been proposed. Both non-linearity and phase noise issues can be corrected by feedback

in a Sigma-Delta loop. Likewise, the main way to improve linearity in an RO-ADC is to implement a closed-loop topology[49], [50]. As mentioned before, this is the main goal of the closed-loop RO-ADCs topologies, as they do not increase the order of the noise-shaping. Although, these topologies show an excellent linearity and power consumption, but are limited by the linearity of the feedback DACs [51] and the oscillator PVT dependence [31]. These topologies would be referred to as sampled closed-loop topologies, as the sampling operation is included within the loop as in Sigma-Delta converters.

An alternative is to implement an unsampled closed-loop RO [52]–[56]. In addition of having the same properties that the sampled closed-loop, such as the linearity and phase noise improvement, this topology have several advantages. Firstly, the need for the DAC is eliminated and thus its linearity is not a limitation anymore. Also the PVT dependence is mitigated. In fact, the unsampled closed-loop RO can be treated from the perspective of sampling like an open-loop RO. The feedback in the unsampled closed-loop RO is in the analog domain, i.e. before any sampling, and thus should have the same properties of analog feedback loops. This includes the stabilization of the gain over PVT, as the gain and rest frequency of the oscillator is now set by the feedback [52].

Other linearization techniques use signal processing or calibration algorithms to compensate non linearity [16], [57]. Also the design of the delay cell can also be improved for better linearity [58]. Finally RO-ADC linearity can be improved by simply optimizing the ring oscillator [59]–[61].

Part II

Building blocks for linear open-loop VCO-ADCs

Chapter 4

Linearization of open-loop VCO-ADCs for MEMS microphones by optimization of VCO driving stages

In this chapter the implementation of high dynamic range RO-ADCs with open-loop topologies for MEMS microphones will be discussed. As an example, the target application will be MEMS microphones. The open-loop architecture is of great interest in the implementation of RO-ADCs due to its simplicity, immunity to clock jitter and inherent stability. Insight on how to efficiently implement high dynamic range open-loop RO-ADCs will be given in the chapter. Different front-ends to directly couple the MEMs with the ADC as well as its pros and cons will be discussed. But most of the chapter will be devoted to present a VCO-ADC based MEMs microphone chip, that shows a high dynamic range with competitive power consumption. The chip is fully MEMs compatible. The focus would be on discussing the analog circuitry of the aforementioned chip, giving only a bird's eye view of the digital components. The digital components are covered in a separated thesis work and collaborative paper. The interested reader is encouraged to check the references for more information about the digital implementation[62].

But before we can dive in the aforementioned topics, a brief introduction of the characteristics and requirements of MEMs based digital microphones is needed, as they would guide the design of the RO-ADC.

4.1 Requirements of MEMS digital microphones and the convenience of open-loop VCO ADCs

Figure 4.1 shows the block diagram of a conventional constant-charge capacitive MEMS digital microphone [63]. The main blocks are a charge pump high-voltage

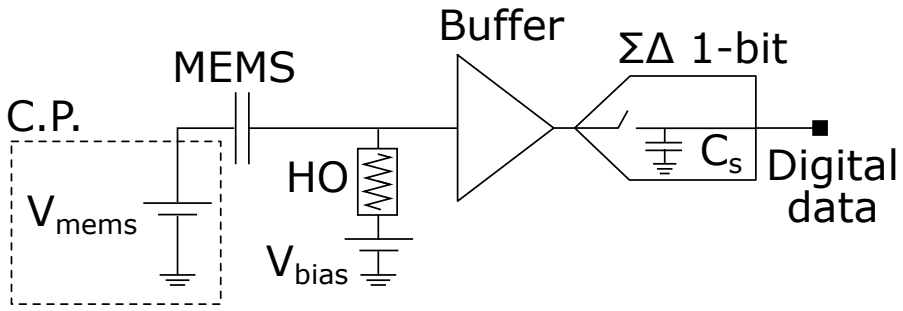

FIGURE 4.1: Conventional digital microphone

generator (CP), a high-ohmic bias resistor (HO), a voltage buffer and the Sigma-Delta modulator [64], [65]. The requirement of always-on operation for keyword recognition demands new microphones with a reduced power consumption. As a consequence, switched-capacitor Sigma-Delta modulators have been improved using inverter-based opamp integrators [66], [67] or replaced by continuous time sigma-delta modulators [68]. However, both switched-capacitor and continuous time Sigma-Delta modulators still require an input buffer [69], [70] to couple the MEMS to the ADC. In switched-capacitor modulators, this voltage buffer is necessary to charge the sampling capacitor C_s (see Fig.4.1(a)), which is on the order of tenths of pF due to kT/C noise limitations. Given the oversampled nature of the Sigma-Delta modulator and the low signal level at the MEMS, this buffer is a critical block requiring high slew rate and very low noise, which results in a significant power consumption. On the other hand, continuous-time Sigma-Delta modulators [68] have a resistive input which also requires a voltage buffer to couple the MEMS high output impedance. Moreover, continuous-time Sigma-Delta modulators are sensitive to clock jitter, which demands special design techniques as for example, using a FIR DAC in the feedback [71].

To explain the requirements of a digital MEMS microphone and the optimizations available using a VCO-based ADC, we show in Fig. 4.2 the typical plots of the Signal to Noise and Distortion Ratio (SNDR) and Signal to Quantization Noise Ratio (SQNR) of a digital microphone, as a function of the input Sound Pressure Level (SPL). The SNDR of a digital microphone is limited by thermal and flicker noises up to a moderate amplitude level (SNDR_{max} around $100dB_{SPL}$ in Fig. 4.2). Thermal noise comes not only from the readout electronics but also from the MEMS sensor[72], [73]. Typically, the MEMS has a very significant contribution to the system noise, therefore it is not practical to improve the readout electronics much beyond that limit, which allows to save power. For input sound pressure levels higher than that producing SNDR_{max}, the SNDR is limited by distortion and drops up to the Acoustic Overload Point (AOP) (AOP=128dB$_{SPL}$ in Fig. 4.2) where the microphone is expected to deliver a much lower SNDR than at SNDR_{max} (40dB in Fig. 4.2). This situation is compatible with human hearing and

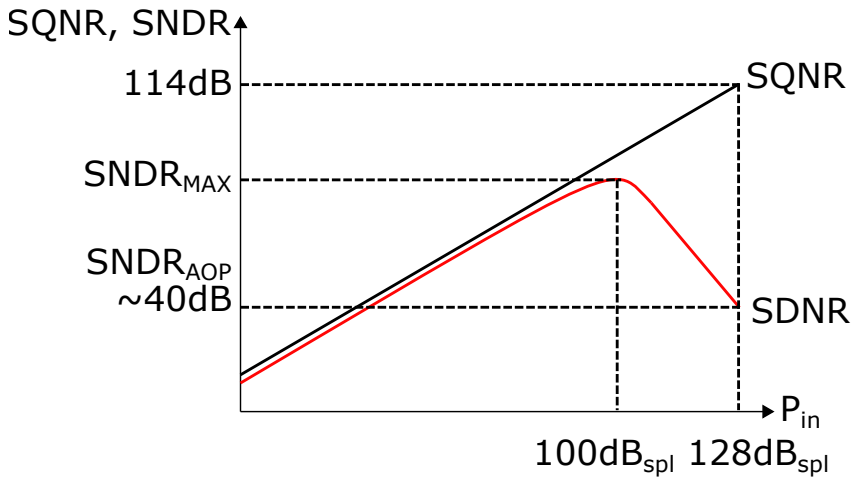

FIGURE 4.2: Typical SNDR and SQNR requirements of a MEMS digital microphone

does not represent a practical limitation, but rather a power optimization opportunity. For instance, a digital calibration algorithm to linearize the VCO-ADC is not mandatory. Nevertheless, quantization noise is designed to be constant such that the maximum SQNR must match with the expected dynamic range of the microphone, which can be in excess of 110dB.

As mentioned previously in this dissertation, VCO-ADCs behave as first-order Sigma-Delta modulators [27], therefore we may use Sigma-Delta theory for their design. Recalling from Chapter 1, the dynamic range (DR) of a first-order Sigma-Delta modulator can be approximated by (4.1), in terms of its Oversampling Ratio (OSR) and the number of bits of its quantizer (N) [27]:

$$DR(dB) = 6 \cdot N - 3.41 + 30 \cdot log_{10}(OSR) \tag{4.1}$$

Using the standard sampling rate for microphones $f_s = 3.072MHz$ and setting $DR = 110dB$, we can calculate $N = 9$ bits as the required quantizer resolution for a $20kHz$ audio bandwidth. As a consequence, a VCO-ADC in a digital microphone must behave as a multibit Sigma-Delta modulator with an unusually large number of quantizer bits, to compensate the limited first-order noise shaping.

As mentioned in Chapter 3 closed-loop VCO-ADCs are supposed to be more linear and power efficient than open-loop VCO-ADCs [74], however, they present a low impedance input node as any Sigma-Delta modulator based on a feedback loop. Therefore, a closed-loop VCO-ADC requires an input buffer same as a conventional Sigma-Delta ADC (see Fig.4.1). In addition, the DAC of a closed-loop VCO-ADC must match the resolution of the quantizer, which can be very large in a microphone (9 bits in our previous example). Although there are several techniques to overcome this problem [75], [76], feedback DAC linearity is still a limitation. As a contrast, open loop VCO-ADCs do not require a feedback DAC and

quantizer resolution is only limited by the VCO frequency. The dynamic range of closed-loop VCO-ADCs is determined by the full scale of the feedback DAC, which corresponds with the maximum input amplitude. When the full scale is reach, the ADC is overloaded. However in the open-loop VCO-ADC, distortion grows progressively with the input signal and the AOP is reach above the maximum SNDR point, in a similar way as in Fig. 4.2. Due to all this, this chapter will be focused on the design of high dynamic range open-loop ADCs.

4.2 Comparison of current and voltage driven ring oscillators

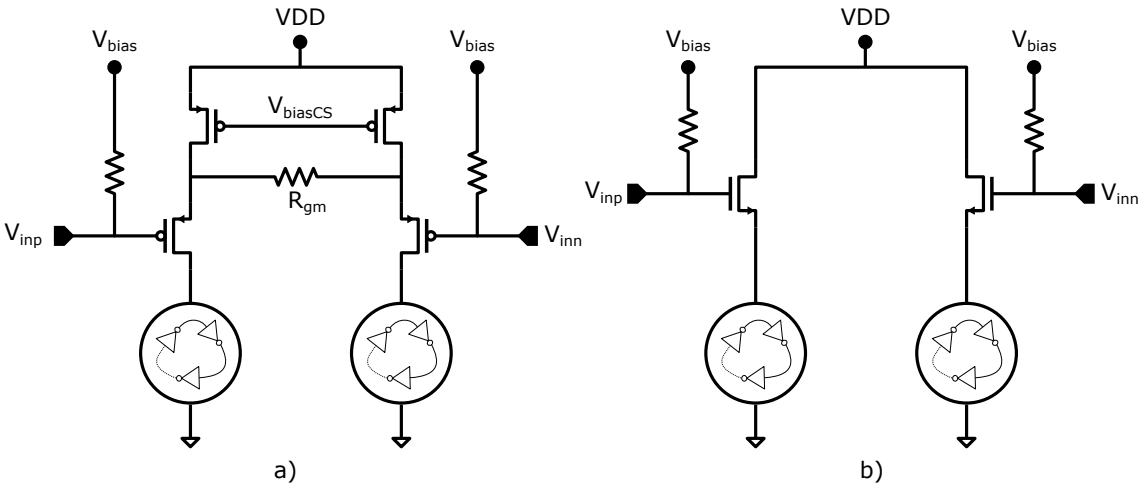

FIGURE 4.3: a) VCO with source degenerated transconductor based front end. b) VCO with source follower based front end.

Once the open-loop architecture has been selected to implement the digital microphone, the next step is to decide the control mode of the oscillator to implement the high input impedance front-end needed to couple the MEMS sensor. As mentioned in the previous chapter, there are two modes to control a ring oscillator, the current mode (CCO) and the voltage mode (VCO). Depending on the selected mode we need a different circuit to drive the oscillator, presenting a high input impedance to the MEMS, as discussed in the previous section. The two alternatives are illustrated in Fig.4.3, using a pseudo-differential architecture.

The strategy to control a CCO is to use a transconductor (GM). This is shown in Fig.4.3 a), where a source degenerated differential pair is used as a GM. Alternatively, the simplest way to control a VCO is to use a source follower (SF) as shown in Fig.4.3 b). Also, a voltage buffer similar to the one used in conventional Sigma-Delta modulators can be employed. The problem with this solution is that, although the current supplied to the VCO can be smaller than in the Sigma-Delta case, not all the current used in the buffer is reused in the VCO. As a contrast,

the circuit shown in Fig.4.3 b) uses the same current to bias both the SF and the VCO. This feature is also present in the GM version of Fig.4.3 a). This makes the open-loop RO a very efficient implementation when it comes to the analog power consumption.

Other similarity between the circuits shown in Fig.4.3 is the aforementioned high input impedance in the MEMS. In fact, if we analyze these circuits from input to output, they are controlled by a voltaje, as both see voltage input signals. However, each of these circuits has some important different characteristics. Understanding them is the key to a successful design, as none of the circuits appears inherently better than the other. The convenience to use one or the other will depend on the application.

The first difference between the CCO and VCO implementation is the way to set the oscillator rest frequency (f_0). In the case of the GM, the rest frequency is set by the differential pair bias current, I_{biasGM}, while for the SF this is set by the voltage in the gate of the SF transistor, which sets a VCO bias voltage equal to $V_{bias} - V_{th}$. This gate bias voltage is set in both topologies through a high-ohmic (HO) resistor, as the MEMS is AC coupled. This difference in setting f_0 does not seem of importance at first glance, but in reality is a critical difference between both architectures, posing extra design challenges in case of the SF bases alternative. This is because of PVT variations. While it is straightforward to compensate PVT variations in the CCO alternative by changing the GM bias current, something easy during chip operation, it is not so simple to adjust the SF gate voltage. This is due to the high time constant imposed by the HO and the combined MEMS and SF's gate capacitance. Also, the SF front-end is more prone to cause f_0 variations under PVT as the VCO bias voltage is determined by the SF transistor threshold voltage, which is very sensitive to temperature and process. Furthermore, if we want to program the bandwidth or resolution of the chip during operation by trading SQNR for power, the same challenges apply to adjust f_0 dynamically.

The same problems are present when dealing with k_{RO} variations under PVT. In the GM based approach, the overall k_{VCO} (remember than from input to output both circuits of Fig.4.3 are VCOs) can be set by adjusting the source resistor in the GM. But in the case of SF this is not possible. We can adjust the SF gate voltage (with the HO shorted to avoid the high time constant, what limits its use only to power up), but this will change also the f_0. There is no way to independently set f_0 and k_{VCO}. A way to solve this is to place a programmable resistor between the SF and the VCO. By changing the resistor value, we can change both the f_0 and k_{VCO}. But the changes on f_0 can be compensated by changing the SF gate voltage. By changing both the resistor value and the gate voltage of the SF we can independently set f_0 and k_{VCO} (to a certain degree). The configuration of SF+Resistor+VCO will be analyzed in more depth later in the chapter.

Another difference between both approaches is noise performance. Differences on noise performance due to the RO control mode has been outlined according with the state-of-the-art [38] in the previous chapter. Aside from these, both driving circuits have different noise sources and different behaviours. Firstly, the GM and the SF has different noise sources. While the GM has two transistors per branch, the SF has only one. Also the two transistors of the other branch of the GM can couple its noise through R_{gm}. Thus the amount of noise sources in the GM is larger than in the SF, so more noise can be expected in the former. Also, in order to lower the noise contributions of the current source transistors in the GM, we need to bias them in strong inversion, i.e. use a high V_{sat}. This is also true for the differential transistors pair, as now the transconductance that refers the noise from this two transistors to the input is determined by $1/R_{gm}$, which is independent of the differential pair bias point. This means that a low noise GM needs high voltage headroom. This is different in the SF, where a best bias for noise purposes places the transistors in weak inversion. Recalling from Chapter 3 that the optimum bias point in CCOs to have low noise is with a high bias voltage, as opposed to VCOs, this means that the current control mode needs higher voltage headroom than the voltage control mode.

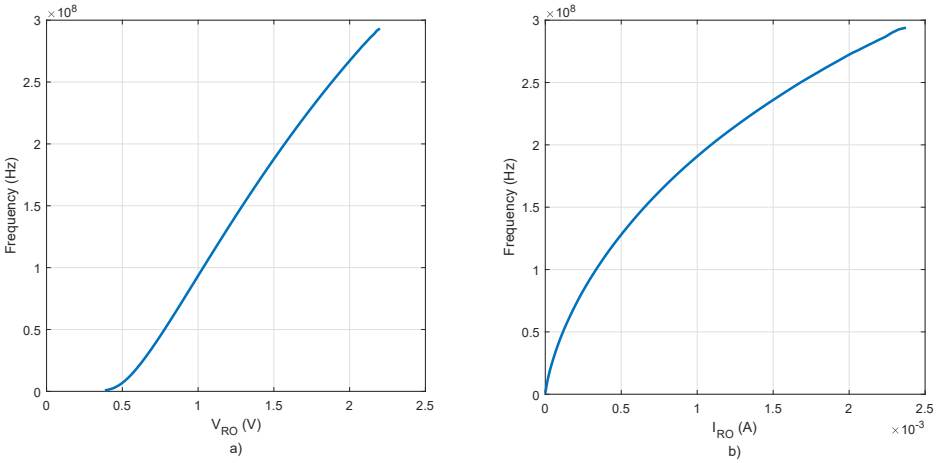

FIGURE 4.4: Tuning curves for an oscillator with sizes $40\mu m/0.8\mu m$ for PMOS and $20\mu m/0.8\mu m$ for NMOS in: a) voltage control b)current control

Finally it is of special interest on this dissertation to analyze the linearity of both approaches. Firstly we should take a look at the drivers in both cases. It is well known that the source degenerated GM has an excellent linearity, that falls abruptly once the current saturates. This is because both current source transistors limit the maximum current that the GM can source. For the SF, the linearity is also quite good despite the distortion due to the transistor body effect. Unlike the GM, the distortion in the SF grows progressively, similarly to the SNDR plot

of Fig.4.2. This means that if our SNDR requirements for the highest input amplitude are lower than the peak SNDR, as happens in Fig.4.2, the SF is a more efficient circuit as with the GM we are losing SNDR.

The other element affecting the distortion of the RO-ADC is the RO itself. Fig.4.4 plots the tuning curves (both voltage and current) of a ring oscillator with PMOS sized $40\mu m/0.8\mu m$ and NMOS sized $20\mu m/0.8\mu m$ in 130nm. Looking at the tuning curves of Fig.4.4 we can intuitively expect that linearity of the VCO is worse at low bias voltages, while the opposite is true for medium an high bias voltages. Fitting the tuning curves from Fig.4.4 to a polynomial, and evaluating this polynomial in different bias points of the tuning curve for a sinusoidal signal with the same excursion of the k_d in each point, the distortion resulting for each tuning curve can be estimated. This method has been used to evaluate the distortion under both current and voltage control modes, with the results shown in Fig.4.5. Figure 4.5 a) shows the HD2 and b) shows the HD3. It can be seen that our intuition proves true. The distortion of the voltage control mode is lower from medium to high bias voltages, while the current control has better linearity at low bias voltages. Notice that this is opposite from the best biasing for noise efficiency [38].

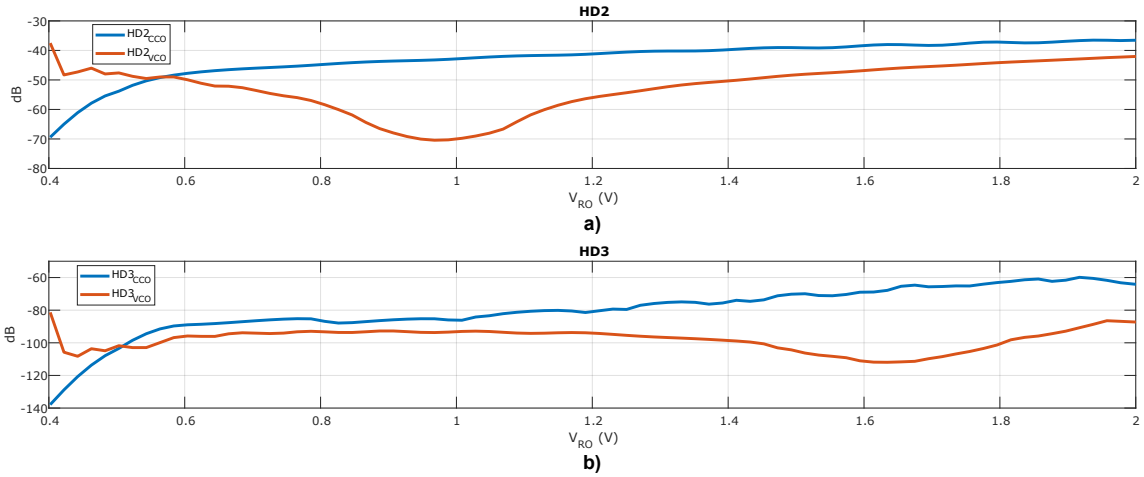

FIGURE 4.5: Linearity of voltage control mode VS current control mode, for a 1kHZ input signal. a) HD2 b) HD3.

Although, the details of the application are key to chose any circuit of Fig.4.3 for the purpose of implementing RO-ADCs for MEMS microphones, the SF is a very interesting option. This is due to several factors. First, the distortion of the SF allows for a more efficient implementation of the SNDR curve of Fig.4.2. Also the linearity of the VCO is better at medium bias voltages, which together with the lower voltage headroom required by the source follower, allows to use a low voltage supply. This reduces the power consumption which is of great interest when designing RO-ADCs for MEMS microphones as they may be used in battery-powered systems. Due to this, we will focus on the SF circuit for the rest

of the chapter. Before that, another potential problem shared by both implementations is worth discussing.

4.2.1 Injection locking

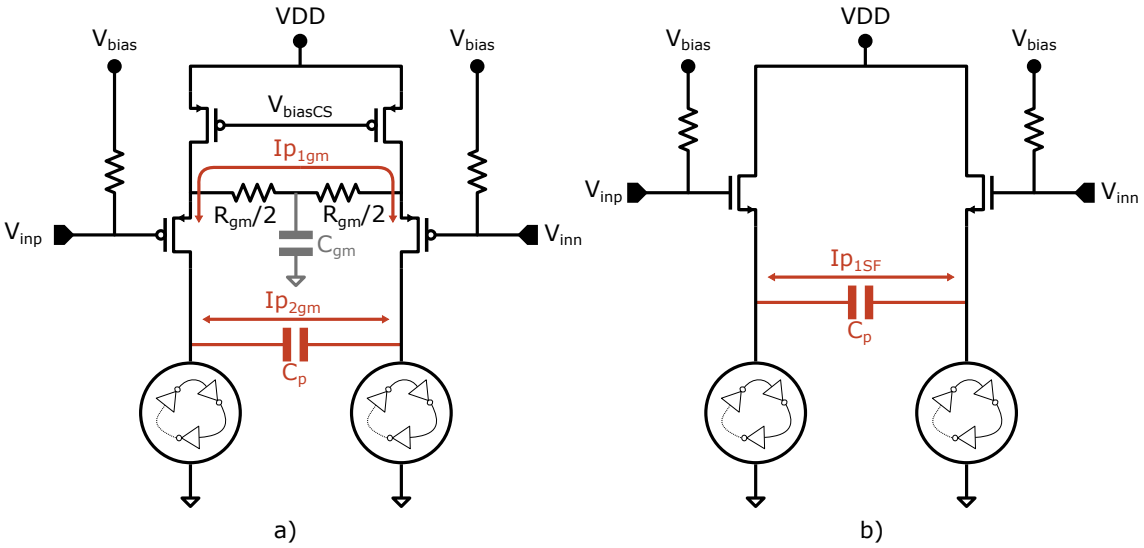

FIGURE 4.6: a) Injection locking in VCO with source degenerated transconductor based front end. b) Injection locking in VCO with source follower based front end.

Injection locking is a phenomenon present in pseudo-differential RO-ADCs. It happens with low input amplitudes and consist in the phase locking on both oscillators of each path of the pseudo-differential architecture. As both oscillators are locked in phase when this phenomenon occurs, the oscillators do not respond to the input signal and thus no output signal is present. Increasing the level of the input signal unlocks the oscillator, making the output signal to be present again. This effect happens because a electrical path with sufficiently low impedance at the oscillation frequency exist between both oscillators.

Figure 4.6 a) shows the two injection locking paths present in the GM controlled oscillator. By circuit inspection, the most evident path is the path through the drain-source capacitance of the differential pair PMOS C_{DS} and the source resistor R_{gm}, marked as Ip_{1gm} in the figure. A second path Ip_{2gm} is present through the parasitic capacitor C_p between the PMOS drain-CCO connection of both sides of the pseudo-differential architecture. The first path can be mitigated by splitting R_{gm} in two and connecting a sufficiently big capacitor between the central point of the split R_{gm} and ground. The second path has to be dealt with by careful layout. Placing sufficient distance in the layout between the PMOS drain-CCO connection of both sides can be enough to avoid this phenomenon. In any case, a metal path connected to ground and the substrate between both sides eliminate this parasitic capacitor.

For the SF case the injection locking path is shown in Fig.4.6 b). Here the only injection locking path present, Ip_{1SF}, is the one between SF-VCO connections of both positive and negative sides. The way to deal with this path is the same that for path Ip_{2gm}, by careful layout. Nevertheless, as the SF has a low output resistance, the VCO control node is more strongly driven, which is expected to make the injection locking mechanism more difficult to be activated.

4.3 Source follower plus ring oscillator architecture

4.3.1 Linearization by resistor

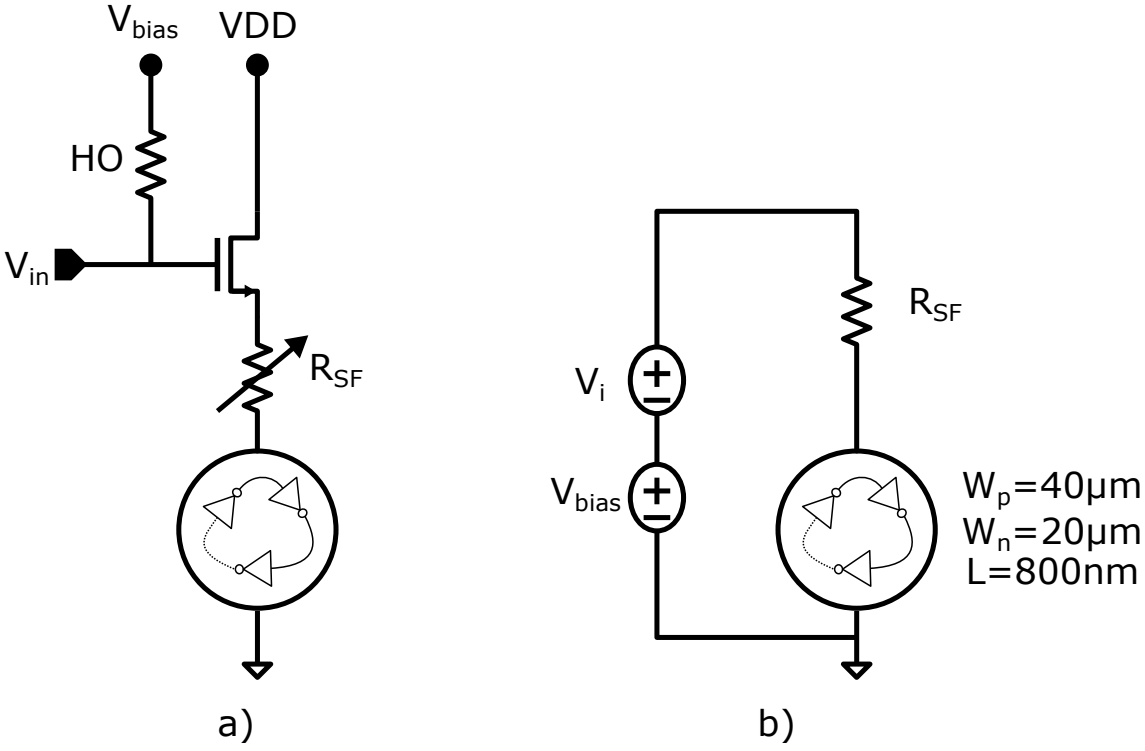

FIGURE 4.7: a) SF+VCO with source follower programmable resistor R_{SF}. b) VCO plus R_{SF} used in periodic state analysis simulations

Previously, when discussing the differences between current and voltage controlled oscillators, it was mentioned that a programmable resistor can be placed between the SF source terminal and the VCO to change f_0, k_{VCO} and also I_{VCO}, so the operation mode of the converter could be changed during operation. The connection of this programmable resistor is shown in Fig4.7 a), where only a single side of the pseudo differential architecture is shown. Here a programmable resistor (R_{SF}) is placed on top of the ring oscillator. This circuit can also be employed in a pseudo-differential architecture like the one shown in Fig. 4.3 a). By

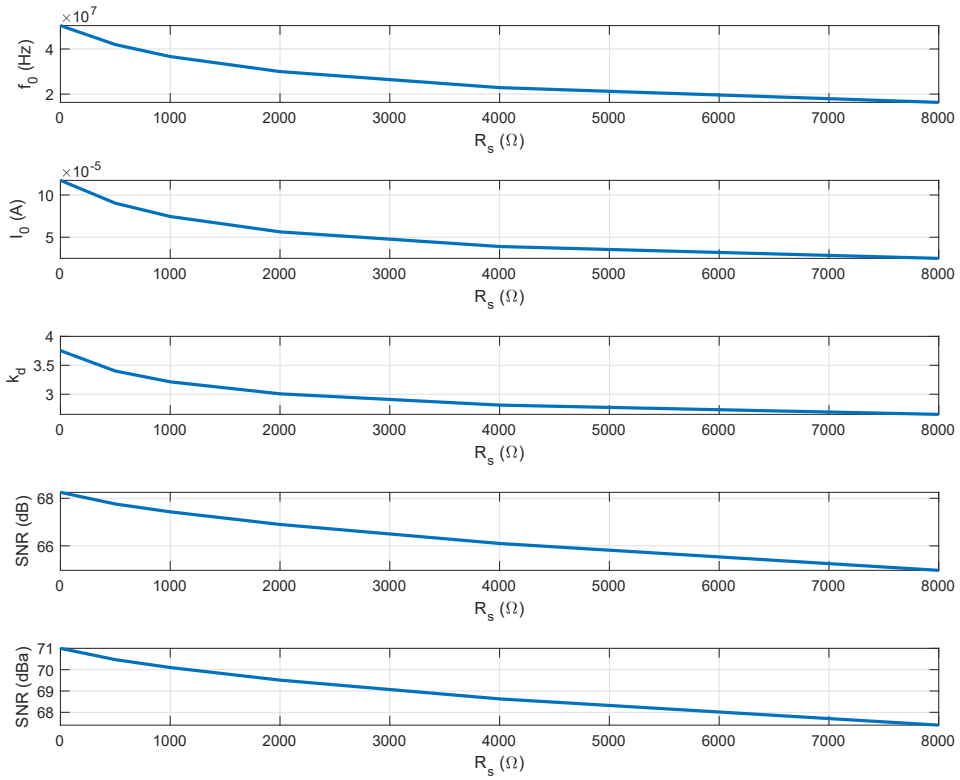

FIGURE 4.8: Variation of f_0, k_d, I_{VCO} and SNR for a -48 dBV input tone at 1 kHz as a function of R_{SF}

changing the value of resistor R_{SF} f_0, k_d and I_{VCO} can be modified. This also changes the SNR due to phase noise, as well as the SQNR due to the variation of f_0 and k_d. The change of f_0, k_d, and I_{VCO} and SNR (including AW-noise) when sweeping the resistor value is plot in Fig 4.8. According to this figure, when the value of R_{SF} is increased, all the aforementioned values decrease. But they do not decrease equally. The more important reduction at the maximum resistor value is found for f_0 and I_{VCO} that fall a 67% and 79% respectively. The fall of the k_d is moderate in comparison with a 30% reduction, while the SNR is almost unaffected with only a 5% less SNR at the highest resistor value.

Aside from this functionality, the addition of the resistor R_{SF} provides a negative feedback for the oscillator, linearizing and stabilizing it across PVT variations. Resistors have been used to cancel the non-linear tuning curve of oscillators before [77]. Unlike in that solution, here the linearization is achieved thanks to negative feedback. Figure 4.9 shows the dynamic ranges obtained using PSS simulations [48] for the same VCO in two configurations: The VCO alone biased at 780mV and the VCO with a resistor R_{SF} of value $3k\Omega$ on top (as shown in Fig.4.7

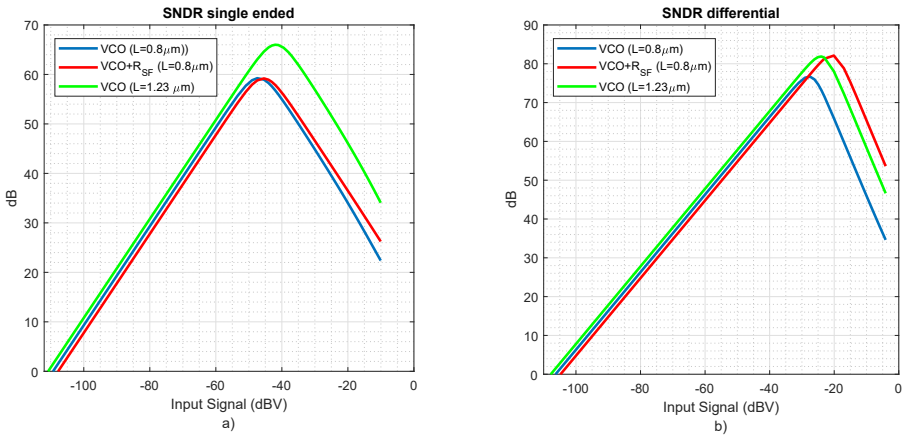

FIGURE 4.9: a) Single ended DR for VCO (blue), VCO+R_{SF} (red) and VCO with long MOS transistors (green). b) Differential DR for VCO (blue), VCO+R_{SF} (red) and VCO with long MOS transistors (green).

b)) and a bias voltage of 1.12V. Transistors in both VCOs are sized $40\mu m/0.8\mu m$ for PMOS and $20\mu m/0.8\mu m$ for NMOS. An additional VCO without the resistor and longer transistors instead that oscillates at the same f_0 than the other two with a 1.12V V_{bias} has been also simulated for comparison. Results are provided for single ended Fig.4.9 a) (showing both second and third harmonic) and differential Fig.4.9 b) (third harmonic limited) configurations. These results show that R_{SF} does not improve the linerarity in the single ended configuration, where only the VCO with longer transistors has a higher $SNDR_{peak}$ and thus better linearity. Instead, the addition of R_{SF} only displaces the SNDR curve to the right, i.e. it is only attenuating the signal.

The situation is different for the differential case. Here, the VCO with long transistor and the one with R_{SF} show similar $SNDR_{peak}$. That means that in both of them the $SNDR_{peak}$ has improved 5.4dB from the conventional case. Nevertheless the power penalty is not the same. The voltage across both VCOs is 1.12v, but the current is different. For the VCO+R_{SF} the current is similar to the conventional VCO and equal to $115\mu A$. The current consumption for the long transistor VCO is $262\mu A$. This means that for the VCO+R_{SF} 40% more power is consumed compared to the simple VCO, while the long transistor VCO consumes up to a 220% more power. So we can conclude that it is more power efficient to use the resistor R_{SF} to improve the linearity of a VCO that to increase the length of the transistors.

There is also the influence of the PVT variations. As resistor R_{SF} provides negative feedback, we should expect a better stability of the oscillation parameters across corners and temperature. Simulation results for f_0 and k_d of the conventional VCO of Fig.4.9 and the one with R_{SF} over corners and temperature are plotted in Fig. 4.10. As can be seen from the figure, the rest frequency of the oscillator, f_0, is more stable across corners and temperature for the VCO+R_{SF},

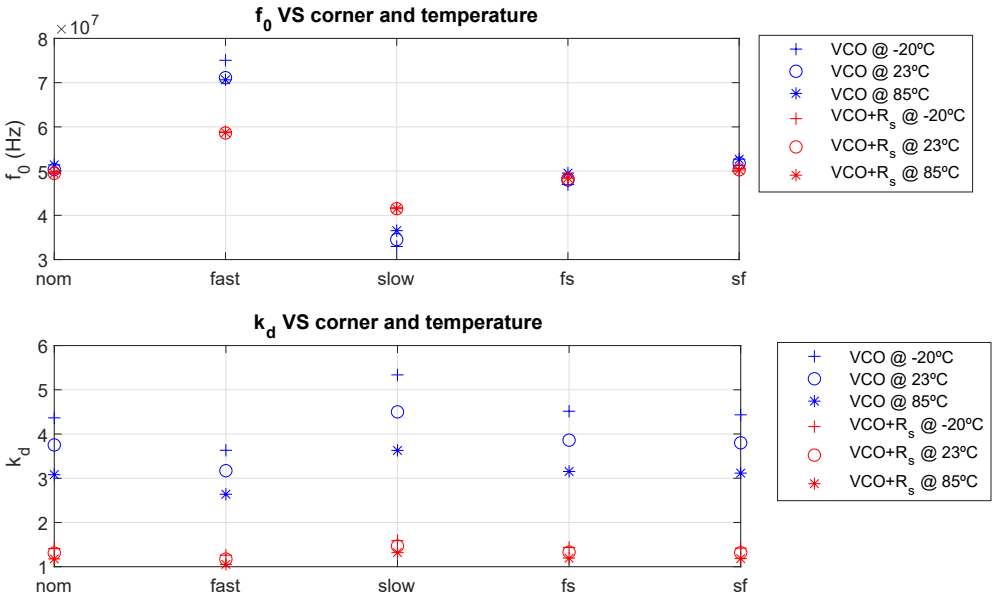

FIGURE 4.10: Temperature and corners dependence of f_0 and k_d for VCO (blue) and VCO+R_{SF} (red).

confirming our expectations. For the case of the k_d it is not so evident from the figure, as each oscillator has a different gain and thus is not easy to compare from visual inspection. Analyzing the data, the maximum k_d for the conventional VCO is 42% higher than the nominal value, while the minimum k_d is 30% smaller than the nominal. For the VCO+R_{SF}, the maximum k_d deviation from the nominal is $\pm$20%. Thus it can be concluded that the resistor R_{SF} stabilizes the VCO thanks to negative feedback. This is an additional use of this resistor, aside from the regulation of the VCO operating point by changing the resistor value.

4.4 Experimental validation: Chip DOC1

To test in silicon all the previously discussed aspects about implementing linear RO-ADCs by circuit optimization, a microphone chip in 130nm has been designed. This chip is a full microphone, that only lacks the MEMS. Nevertheless all the needed circuitry for the microphone is present, including the necessary ancillary circuits. The core of the chip is composed by an analog front end containing a SF based VCO, and the digital back-end that includes the frequency-to-digital converter. In the remaining of this chapter the focus will be placed in the analog front end, although some description about the digital circuitry will be also provided. The interested reader that want to know more about the digital back-end is encouraged to consult reference [62].

4.4.1 System level design

Figure 4.11 shows the building block diagram of the microphone chip, highlighting the ADC as the main component. Apart from the ADC, there are other ancillary circuits: voltage regulators (LDO), Band-gap reference (BG), Serial Parallel Interface (SPI), MEMS Bias generator (CP) and digital Noise Shaper (NS) which are not addressed in this dissertation for being common in MEMS microphones [64], [65]. The microphone chip is intended for a dual back plate MEMS sensor providing two differential analog signals and a common terminal connected to the CP [64]. The ADC architecture uses a pseudo-differential circuit with two identical signal paths to seize the differential MEMS output, mitigate distortion and enhance the Power Supply Rejection Ratio (PSRR). The ADC is composed of two main blocks, the analog core and the digital core. The analog core includes two source followers with their biasing circuits and two VCOs. The digital core implements the coarse-fine frequency-to-digital converter and is composed of a full custom double binary counter and the coarse-fine interpolation logic, which is synthesized from a hardware description language specification. Multibit first-order noise-shaped data $Y[n]$ is converted to a single-bit PDM signal by means of a digital fifth-order Noise Shaper (NS). In this subsection the basic operation of the ADC coarse-fine architecture [40] will be explained and in the next subsection, the circuit design of the analog core blocks. The digital design will be only briefly commented, as it will be described in full in a different dissertation.

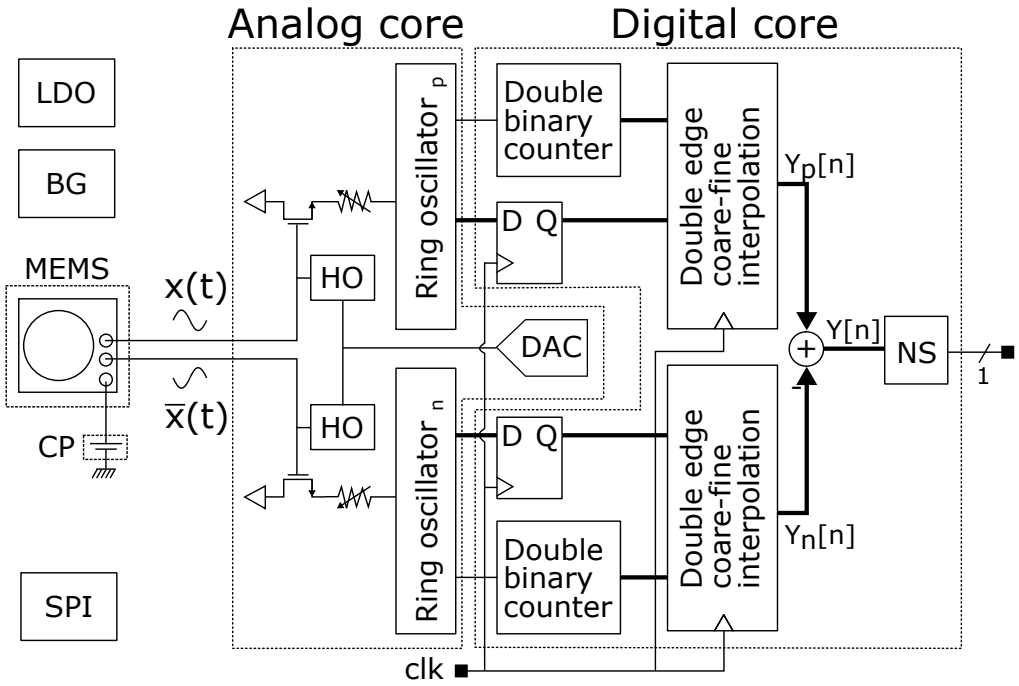

FIGURE 4.11: Block diagram of the proposed architecture.

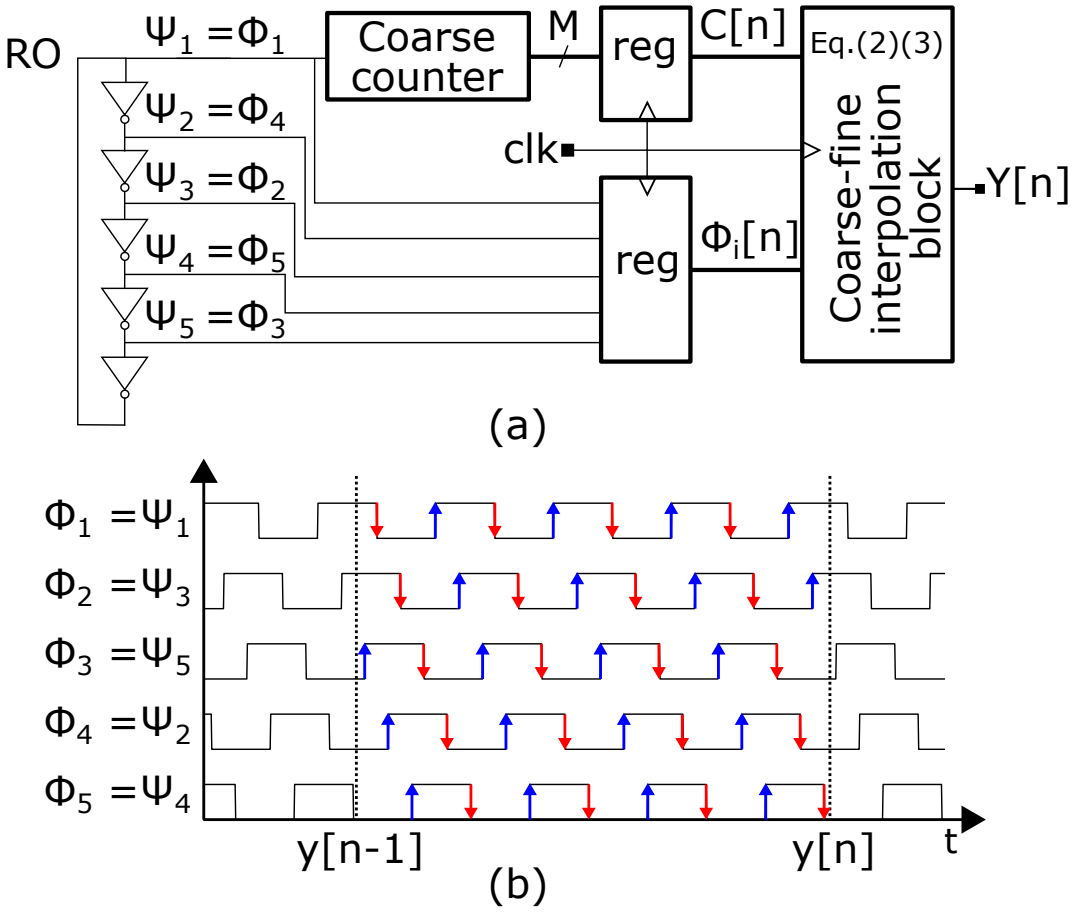

FIGURE 4.12: (a) Example of Double edge coarse-fine architecture and (b) counting the edges of the implementation.

Figure 4.12(a) shows the block diagram of an open-loop VCO-ADC that uses the coarse-fine architecture. This architecture was already introduced in Chapter 3. Here a more detailed explanation follows. The coarse-fine architecture counts the total number of edges produced in a sampling period by a ring-oscillator, oscillating faster than the sampling clock. The number of edges per sampling period generates sequence Y[n], the first-order noise-shaped multibit ADC output [27]. Given that the VCO oscillator produces several cycles per sampling period, we cannot use an array of samplers and XOR gates to account for the number of edges, as in other types of VCO-ADCs [27].

As mentioned in Chapter 3, instead of the XOR array, we could attach a counter to each one of the VCO output phases and add all counters every sampling period. However, this would result in a fairly inefficient circuit, as all counters would count the same number except for +/-1 unit. The example of Fig. 4.12(a), depicts a ring oscillator with $N_{ro} = 5$ inverters with consecutive outputs (Ψ_1 to

Ψ_5). We will restrict N_{ro} to be always an odd number in our explanation. The consecutive inverters produce square signals whose edges are not ordered in time. Figure 4.12(b) shows the wave forms at the VCO outputs Ψ_i reordered to have consecutive edges of the same polarity, by sorting them in two sets with Ψ odd phases followed by the Ψ even phases and renaming the phases as Φ_i, $i = 1...5$. In the example of Fig. 4.12(b), we have marked sampling instants $t = (n-1)T_s$ and $t = nT_s$, where $f_s = 1/T_s$ is the sampling frequency. We will sample the VCO output signals at these sampling instants with a register and designate the sampled sequences as $\Phi_i[n], i = 1..5$. After reordering, data in $\Phi_i[n]$ appears reorganized as blocks of contiguous ones and zeros containing either $(N_{ro}+1)/2$ ones and $(N_{ro}-1)/2$ zeros or the opposite.

If we count the rising and falling edges between sampling instants in the example, (see blue and red arrows in Fig. 4.12(b)), we obtain $Y[n] = 40$ edges. To simplify the counting process, we can choose a reference phase (Φ_1 in Fig. 4.12(a)) and use it to clock a M-bit counter that is latched with the sampling clock, generating the coarse-count sequence $C[n]$. In the example of Fig. 4.12(b), and considering the rising and falling edges of Φ_1, we see that the coarse counter increments by $C[n] - C[n-1] = 8$ units in sampling period n. The key idea of the coarse-fine architecture is that we can combine $C[n]$ with the sampled VCO signals $\Phi_i[n]$ to calculate the total amount of both rising and falling edges $Y[n]$, without requiring additional counters. To do so, we define in (4.2) an auxiliary fine-count sequence, $S[n]$ and build the ADC output $Y[n]$ by combining sequences $C[n]$ and $S[n]$, as described in (4.3). All these computations are performed in Fig. 4.12(a) by the Coarse-Fine interpolation block:

$$S[n] = \Phi_1[n] \cdot \left(\sum_{i=1}^{\frac{N_{ro}+1}{2}} (2 \cdot \Phi_i[n]) + \sum_{i=1}^{N_{ro}} (\overline{\Phi_i}[n]) \right) + \overline{\Phi}_1[n] \cdot \left(\sum_{i=1}^{\frac{N_{ro}+1}{2}} (2 \cdot \overline{\Phi}_i[n]) + \sum_{i=1}^{N_{ro}} (\Phi_i[n]) \right) \quad (4.2)$$

$$Y[n] = N_{ro} \cdot (C[n] - C[n-1]) + (S[n] - S[n-1]) \quad (4.3)$$

Note that we are assuming the first difference in the coarse counter to be taken as a modulus M difference. The power and area consumed by computing (4.2) and (4.3) is significantly lower than that of a multiple counter solution.

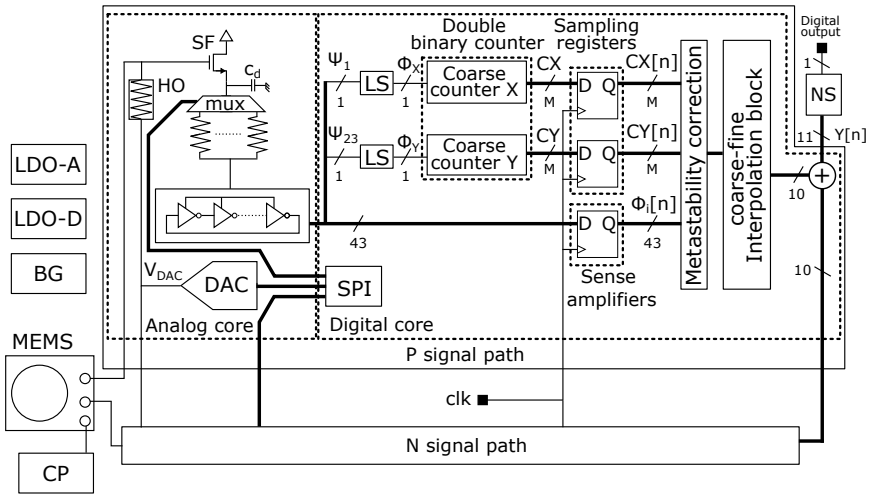

FIGURE 4.13: Block diagram of the chip.

4.5 Circuit design

Figure 4.13 shows the simplified schematic of the proposed ADC circuit, detailing the positive signal path of the pseudo-differential architecture. Same as in Fig. 4.11, we have split the circuit in analog and digital cores. We will explain the design and operation of each block next.

4.5.1 Analog core circuit design

The analog core structure is shown in Fig.4.13. It is composed of two NMOS source followers and two voltage-controlled-ring-oscillators in a pseudo differential configuration. The source follower provides a high input impedance interface for direct connection with the MEMS. The body effect on the SF has been evaluated and considered negligible. The MEMS is AC coupled to each gate of the SF. Each VCO is connected as the load of its respective SF, sharing its bias current. The bias voltage of the SFs is set through a high ohmic resistor (HO), on the order of $300G\Omega$. The HO is implemented by a series of reverse biased diode connected PMOS transistors. A PMOS switch is placed in parallel for circuit start-up. Each tap of the VCO is connected to the digital core for frequency-to-digital conversion.

The VCO is implemented using single-ended CMOS inverters. These are chosen over differential inverters due to their better thermal noise performance [38] and smaller area. No special Power Supply Rejection Ratio (PSRR) penalty has been observed due to the single ended inverter choice in the measurements (see Section 4.6). As discussed in section 4.2 an SF is chosen over a source-degenerated transconductor (GM) to implement the high input impedance interface with the MEMS due to several reasons [40]. Firstly, a single transistor SF circuit reduces

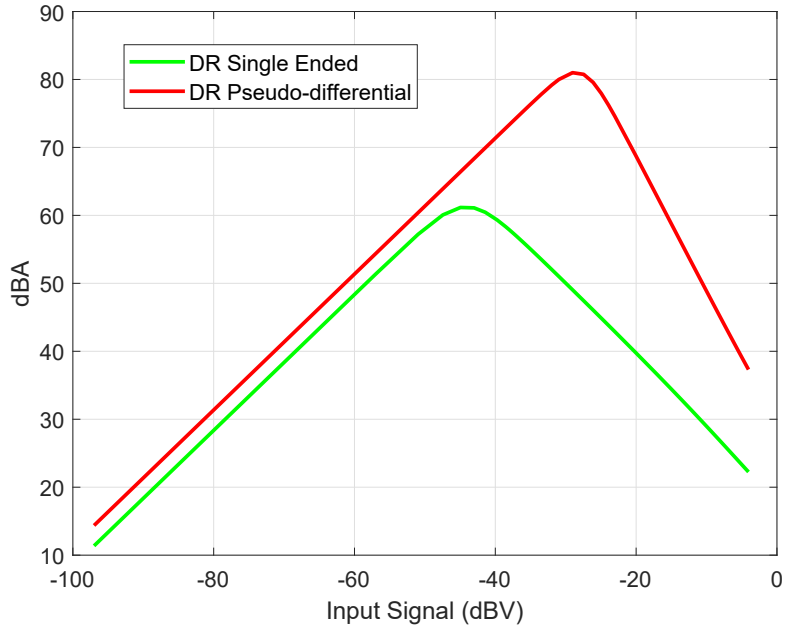

FIGURE 4.14: Simulated dynamic range using PSS analysis

TABLE 4.1: Values for resistor array

	R_0	R_1	R_2	R_3	R_4	R_5	R_6	R_7	R_s
R (Ω)	470.7	892.2	1615.7	2391.2	3114.2	4211.2	6480.5	9469.4	short

the required voltage headroom and thus eases the implementation of the MEMS interface plus VCO structure at lower supply voltages. Secondly, the current supplied by the SF during circuit operation is not limited by the bias current as in the GM case. Therefore, the SF has the benefit over a GM of a less steep decay of the SNDR plot once the peak SNDR is reached. The combination of a SF plus a VCO is thus a power efficient solution to fulfill the SNDR requirements of the coupling circuitry to a MEMS microphone (see Fig.4.2).

As previously mentioned, the use of the SF is not free of challenges. To compensate PVT variations, the bias voltage at the gate of the SF has to be adjusted. In the chip, a single DAC connected to the HOs has been used to set the bias voltage. The use of a single DAC for both branches guarantees the same bias voltage in the two sides of the pseudo-differential architecture. A decoupling capacitor C_d has been added to mitigate the charge injection form the VCO into the MEMS through the parasitic capacity C_{gs} of the SF.

After the SF, a programmable analog multiplexer (mux) and a poly resistor array have been placed in series between the SF and the VCO. The resistor array can change between 8 different values shown in Table 4.1 plus a short (R_S) for

TABLE 4.2: A-weighed Noise Contributions

Component	**Device**	**Noise type**	**Noise NM mode (%)**	**Noise LP mode (%)**
VCO	PMOS	Flicker	13.9	4.6
		Thermal	11.4	23.2
	NMOS	Flicker	36.7	22
		Thermal	6.6	13.9
SF	NMOS	Flicker	24.3	9.8
		Thermal	0.8	1.2
Resitive Array	Resistor	Flicker	0.1	0.8
		Thermal	2.6	22.4
	PMOS switch	Flicker	3.3	1.7
		Thermal	0.2	0.3

testing. The main purpose of the resistor array is to program the SQNR of the ADC allowing a fast regulation of the oscillator rest frequency. As outlined in section 4.2, this cannot be accomplished by changing the bias voltage in the gate of the SF because that path is affected by the time constant of the HO and MEMS capacitor. This change in the VCO's frequency allows to trade power for SQNR while the microphone is in operation. The linearization effect discussed in section 4.3.1 is not the objetive of the resistor array in this chip.

The oscillator has been designed for a $SQNR_{max}$ of 117 dB (123dBA) in pseudo differential configuration with an OSR of 76.8 leaving 7dB of margin between quantization noise and other dominant noise sources such as sensor and ADC thermal and flicker noises. To achieve the aforementioned SQNR, the effective rest frequency of each oscillator [27] must be $f_0 = 1.72GHz$ with a $k_d = k_{VCO}/f_0 = 2.5$, assuming rising and falling edge detection in the frequency-to-digital conversion. The number of taps of the oscillator is mainly determined by flicker noise specifications [48] and power consumption of the digital logic. Using the Periodic Steady State (PSS) noise analysis methodology described in [48], the number of taps has been set to $N_{ro} = 43$. The selected number of VCO taps sets the VCO rest frequency to $f_0 = 20MHz$, and the $k_{VCO} = 50MHz/V$.

Table 4.2 shows the A-weighed noise contributions in percentage for each device in NM and LP mode. The total Input Referred Phase Noise (IRPN) [48] for the NM is $4.5pV^2$ for each channel. For the LP mode the total IRPN is $10.7pV^2$.

The acoustic overload point of the chip (AOP) has been defined at $128dB_{SPL}$ which corresponds approximately to an input voltage of -2dBV coupled through a 4pF input capacitance, assuming an standard dual back-plate MEMS. The VCO inverters and the SF transistor sizes have been optimized iteratively using PSS noise simulations [48]. In order to reduce noise contribution, the SF is biased in weak inversion, which increases the size of the SF and thus its input capacitance. The MEMS and the SF gate capacitance form a capacitive divider that attenuates

TABLE 4.3: PVT variation compensation

Corner	T(ºC)	f_0 (MHz)	$\Delta f_0(\%)$	V_{bias} (V)
Nominal	-40	18.2	9.9	1.28
	27	20.2	0	1.25
	85	19.5	3.4	1.18
Fast	27	19.2	4.9	1.05
Slow	27	19	5.9	1.42
Slow Fast	27	19.3	4.4	1.26
Fast Slow	27	18.2	9.9	1.2

the signal. In order to mitigate the effect of the input capacitance, a minimum length of $400nm$ is used in the SF. The SF width is then sized to optimize the SNR considering both the capacitive divider and the noise. The maximum input amplitude ($128dB_{SPL}$) seen at the gate of each SF is $444.1mV$. The simulated dynamic range (DR) of the complete analog core is shown in Fig. 4.14. The green line shows the single ended results, while the red line shows the pseudo-differential results. The THD for the pseudo-differential case is below 1.4% at the AOP.

The DAC to set the SF bias voltage is implemented with a resistor string topology. The range of possible voltages go from 1V to 1.49 V with 5 bits of resolution. The DAC output is not buffered because it is connected to a high impedance node. The resistor string bottom is connected to a 1 V reference obtained from the BG and buffered by a miller OTA. The output of the DAC drives the low pass filter formed by the HO and the parallel capacitance of the MEMS and the gate capacitance of the NMOS SF transistor. The fact that the cut-off frequency of this low-pass filter is extremely low ($< 1Hz$), and that the DAC Voltage is common to both sides of the pseudo-differential path, minimizes the noise contribution of the OTA and the DAC resistors.

To evaluate the on-chip resources required to keep the VCOs operating in the correct margins, a corner simulation has been performed. Table 4.3 shows the VCO rest frequency f_0 for different temperatures after the bias voltage of the SF, V_{bias}, has been corrected with the DAC code. It can be seen that the DAC provides all necessary correction values of V_{bias} to compensate the temperature in the VCO frequency up to a 10%. Also, Table 4.3 shows a similar compensation for different process corners at 27ºC using the DAC. In the nominal process and at 27ºC, a biasing Gate voltage in the source follower of 1.25V results in a voltage in the Source terminal of 800mV. In the VCO terminals, we have in these conditions 797.5mV when a short is selected in the resistor array.

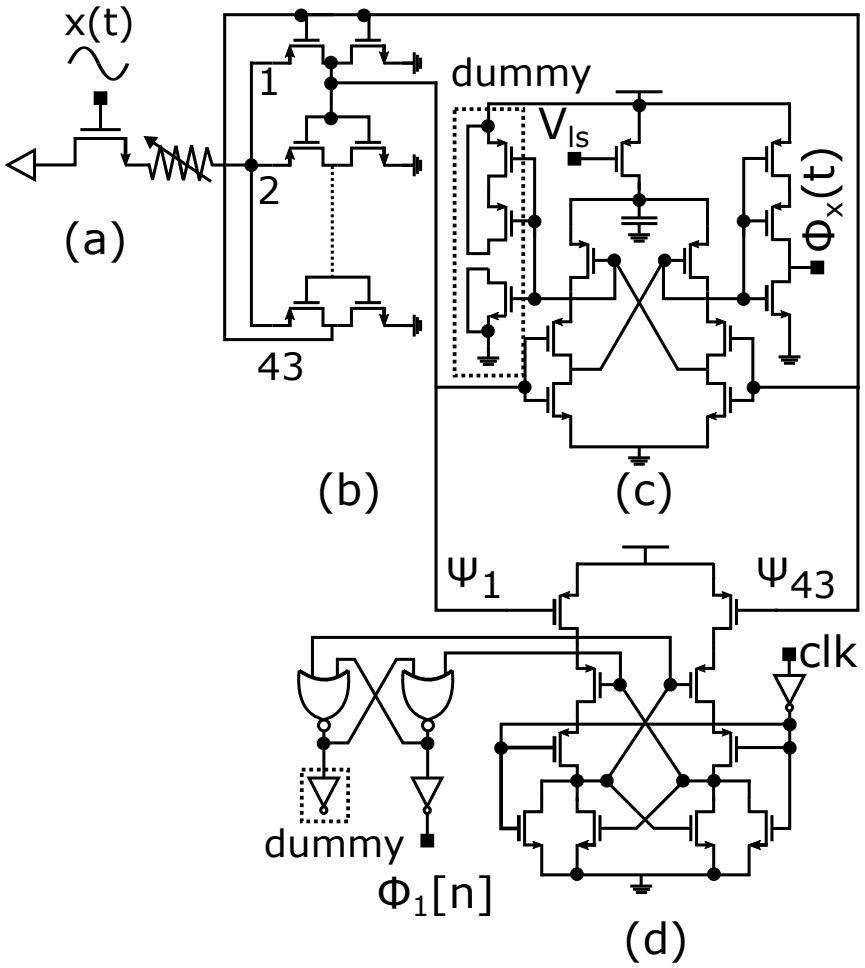

FIGURE 4.15: Circuit diagram of (a) source follower, (b) ring oscillator, (c) level shifter and (d) sense amplifier

4.5.2 Analog-digital interface

In Fig.4.13, we show the digital core implementation that consists in two Level Shifters (LS), a Double Binary Counter (DBC), Sampling Registers (SR), sense amplifiers (SA), the metastability correction block and the coarse-fine interpolation logic. The function of the LS is to convert the ring oscillator output signals to valid logic levels, eliminating the amplitude modulation in the VCO. The DBC counters are two asynchronous counters clocked with the rising edge of phases Ψ_1 and Ψ_2, which are physically consecutive phases in the ring. However, considering the phase reordering (see Fig. 4.12.a) these would be phases Φ_1 and Φ_{23}. We will name $\Phi_x(t)$ the output of the LS connected to Ψ_1 and $\Phi_y(t)$ the output of the LS connected to Ψ_2, as they are employed to clock coarse counters X (BCX) and Y (BCY) respectively. The SR sample counters BCX and BCY at the clock frequency producing sequences $CX[n]$ and $CY[n]$. The SAs sample all ring oscillator

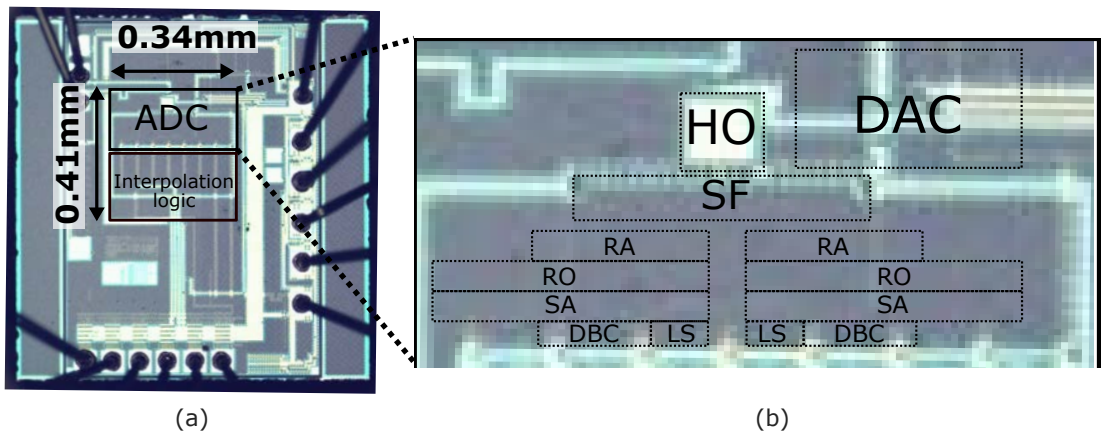

FIGURE 4.16: (a) Micrograph of the microphone chip. (b) Detail of the ADC

phases at the clock frequency, generating $\Phi_i[n]$. Figure 4.15 shows a simplified diagram of the interconnection between the SF (a), the RO inverter cells (b), the LSs (c) and the SAs (d) which seize the input (Ψ_{43}) and output (Ψ_1) of a single ended inverter in the RO as differential inputs. In Fig. 4.15 the circuits for signals $\Phi_1[n]$ (SA) and $\Phi_x(t)$ (LS) are shown. The rest of the phases only require the SA, except Φ_{23} which is similar to the circuit in Fig. 4.15. Using a PMOS input for the SA guarantees that, given the output voltage levels of the VCO, at least one of the two SA input transistors is in strong inversion, reducing the SA metastability. As stated before, the implementation of the coarse-fine architecture is out of the scope of this dissertation and will not be discussed here.

After the F2D implemented with the coarse-fine architecture, the output signal $Y[n]$ is encoded by the NS for compatibility reasons with industry-standard codec interfaces [40]. The in-band quantization noise added by the NS is well below the thermal and flicker components of the ADC and therefore all measurements are limited by the ADC itself and not by this block. The noise shaper is embedded as part of the synthesized digital block and will be considered another ancillary block, therefore its design is not covered in the dissertation.

4.6 Measurement results

The microphone chip has been fabricated in a 130nm CMOS process. The die photo can be seen in Fig.4.16. The active area of the ADC is enlarged at the right side of the photo with an occupied area of $0.14mm^2$. The supply voltages for the analog and digital cores are 1.5V and 0.95V respectively. The chip has two operating modes: Normal Mode (NM) and Low Power mode (LP). The ADC can be set in modes NM or LP by changing the resistor value in the resistor array (see Fig. 4.13) and the clock frequency. Mode NM works with a clock frequency

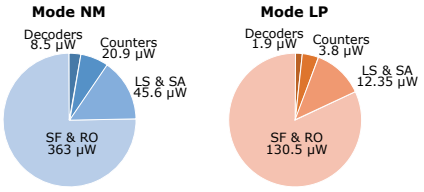

FIGURE 4.17: Power consumption split among different blocks

of 3.072MHz, a signal bandwidth of 20kHz and is selected by setting R_0 in the resistor array. Mode LP works with a clock frequency of 768kHz, a signal bandwidth of 8kHz and is selected by setting R_7 in the resistor array. This modifies the rest frequency of both oscillators accordingly to the sampling rate. The NS input gain and NTF zeros are also digitally modified to accommodate different full scale ranges and bandwidths among modes.

The ADC consumes 438µW/148.6µW, in modes NM and LP respectively. The total power consumption of the microphone chip including all auxiliary circuits and the VCO is less than 520µW. Figure 4.17 shows the power consumption split among different blocks for both modes LP and NM. As can be seen, most of the power is devoted to the VCOs and required to meet thermal and quantization noise specifications.

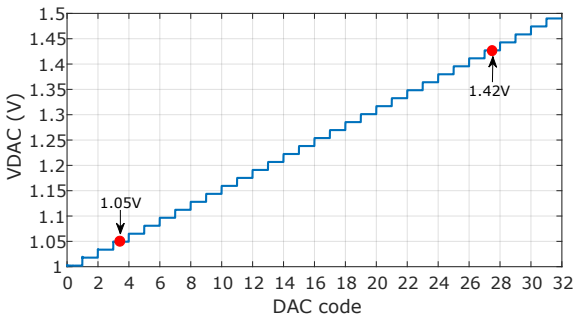

FIGURE 4.18: Bias DAC transfer characteristic

To measure the chip performance, we have to define the value of V_{DAC} in Fig. 4.13 that sets the nominal rest frequency of the oscillators, (approximately 20MHz, see Table 4.3). By means of the SPI control port, it is possible to bring the reference phase Ψ_1 to a pin. This way, the DAC code can be adjusted to the proper value. DAC calibration needs to be done only at start up to compensate process variations. Frequency drifts due to temperature are smaller than those due to process variations. In addition, moderate frequency offsets translate into a common mode digital offset that is removed in the digital post processing. Therefore, no online calibration of the VCO frequency is required. Figure 4.18 shows the code v.s. output voltage curve of the biasing DAC. The corner simulations of Table 4.3 have been used to define the DAC transfer characteristic. The voltage range needed to accomplish the worst-case process variation is between $1.05V$ (Fast

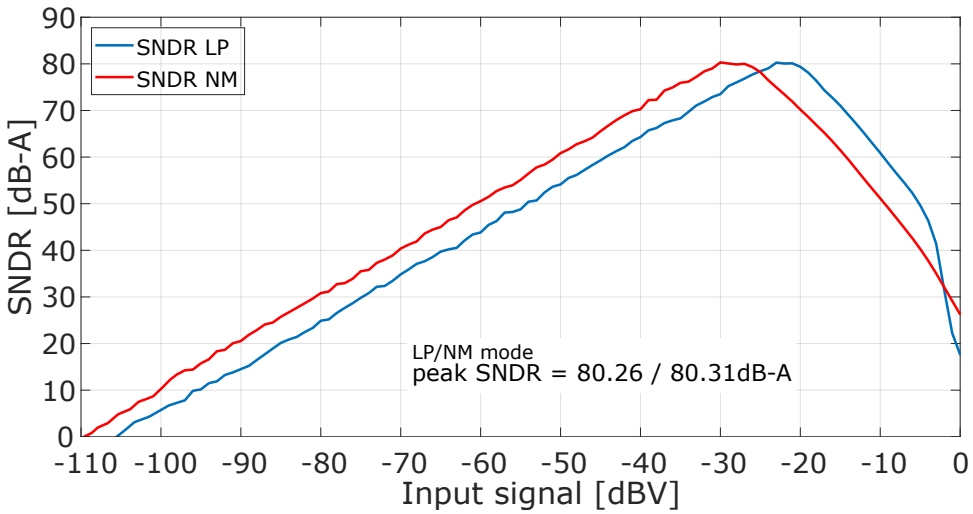

FIGURE 4.19: Dynamic range in LP and NM modes

corner) and 1.42V (Slow corner), see the red dots in Fig. 4.18. As a contrast, the required calibration range for temperature deviations would only require 10mV of span between -40ºC and 85ºC (see Table 4.3).

Figure 4.19 shows the measured A-weighted dynamic range plot for modes NM (red) and LP (blue). The peak SNDR is 80.31dB-A for NM, and 80.26dB-A for LP modes. The plots show the average values of several different samples.

Figure 4.20(a) shows the FFT of the NS single bit output (digital output in Fig. 4.13) in LP mode with an input signal of 1kHz and $-36dBV$. Figure 4.20(b) shows the corresponding FFT for mode NM and the same input signal. This amplitude corresponds approximately with the expected level of a dual backplate MEMS driven by a $94dB_{SPL}$ reference audio signal. The signal source is a Stanford Research Systems DS360 generator, coupled through a dummy MEMS test fixture.

The Total Harmonic Distortion (THD) of the ADC has been also measured and is depicted in Fig. 4.21 for modes NM (red line) and LP (blue line). The THD reaches 5% for an input of 0dBV in mode NM, which would correspond approximately to -130dBSPL ($36dB$ above the reference sound pressure level of $94dB_{SPL}$, see Fig. 4.19).

To test the effect of temperature variations in the SNDR at the reference point of $-36dBV$, a thermal test has been performed. Figure 4.22 shows the SNDR in modes LP and NM for a temperature sweep between -20ºC and 50ºC and without frequency correction (see Table 4.3). Even in this uncalibrated measurement, the maximum SNDR deviation from the reference value at 27ºC is below 2.4dB in mode NM and 1dB in mode LP.

Figure 4.23(a) and Fig. 4.23(b) show the SNDR degradation due to clock jitter in mode LP and NM respectively with a $-36dBV$ input signal (see Fig.4.19). As can be seen, measurements show that a rms clock period jitter up to 4% of the nominal sampling period produces a SNDR degradation smaller than 1.5dB-A.

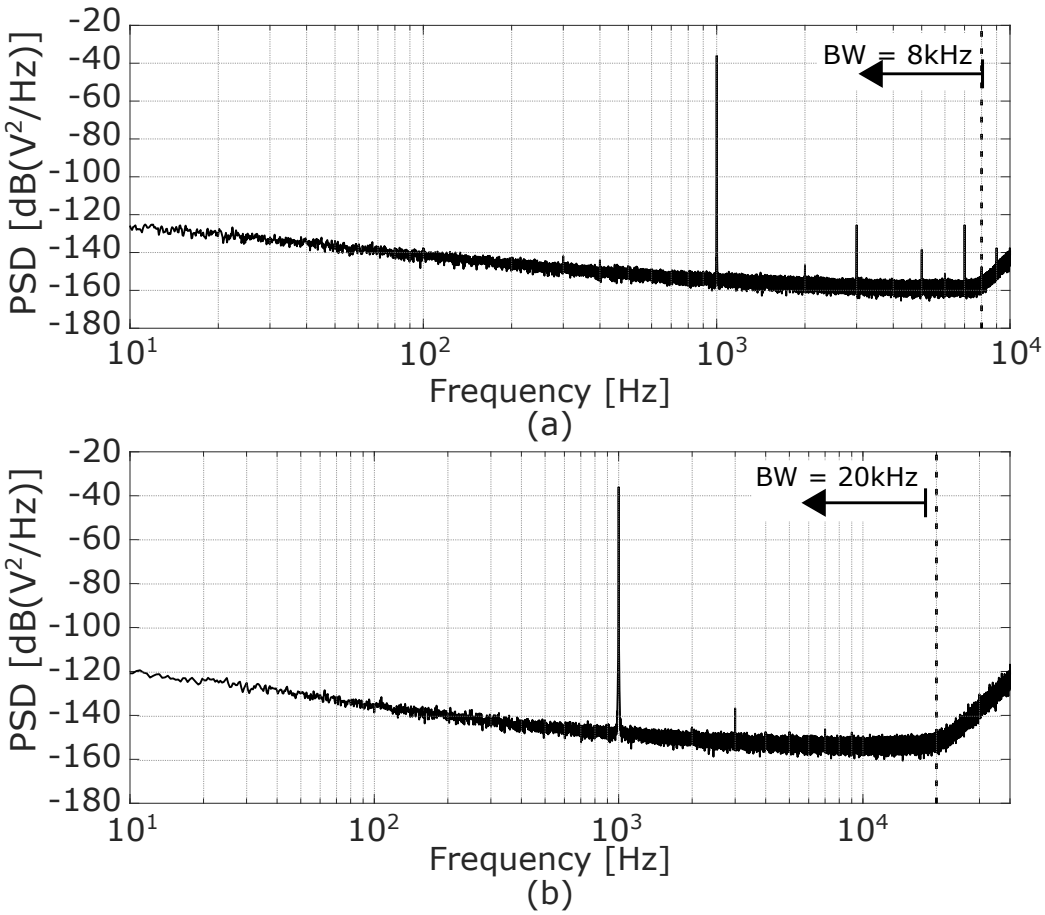

FIGURE 4.20: FFT for 1kHz, -36dBV input. (a) LP mode, (b) NM mode

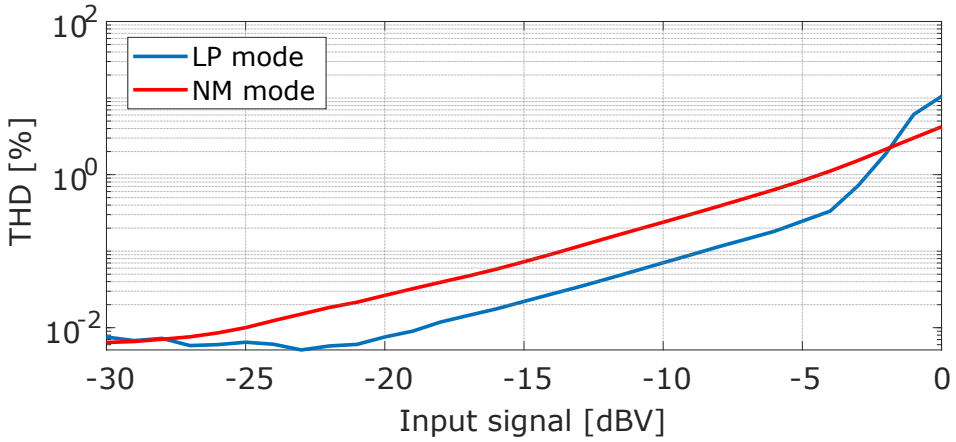

FIGURE 4.21: THD in LP and NM modes

As shown in [78], the high clock jitter tolerance of this architecture is due to the matching between positive and negative RO rest frequencies, turning clock jitter

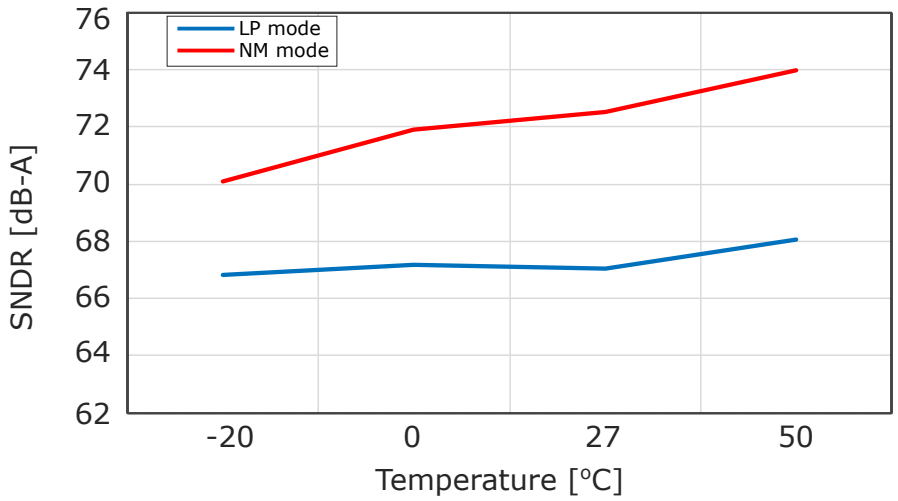

FIGURE 4.22: SNDR at different temperatures in LP and NM modes

errors into a common mode perturbation for moderate clock jitter levels. This result is in par with switched-capacitor converters and does not require compensation by any special circuitry as a difference to continuous-time sigma-delta modulators.

To analyze the effect of the mux and resistor array placed between the SFs and the VCOs (see Fig. 4.13), several measurements have been performed. Figure 4.24 shows the noise floor of the ADC when the value of the resistor array is changed from R_0 to R_7 for signal bandwidths and clock frequencies corresponding to modes LP (Fig.4.24(a)) and NM (Fig.4.24(b)). The noise floor is evaluated applying a 1kHZ, $-36dBV$ tone and removing the tone from a FFT measurement. This plot shows the variation of the noise floor due to the different VCO oscillation frequencies.

Figure 4.25 shows the influence of the resistor value in the overall SNDR for the same 1kHz, $-36dBV$ input (black line) in mode NM. It can be seen that from maximum (R_7) to minimum (R_0) resistor values, the difference in SNDR is approximately $10dB$. Also, Fig. 4.25 shows the power consumption of the analog core (blue dash) with the different resistors, which ranges form $250\mu A$ to $110\mu A$, therefore the converter can effectively exchange SNDR by power consumption. The explanation for this is shown in Fig. 4.26 which plots the VCO rest frequency v.s. the resistor value (black line). As a reference, the analog power consumption is also plotted (blue dash) in Fig. 4.26. For all resistors, the digital power consumption (blue dots in Fig. 4.25 and Fig. 4.26) is approximately the same, as it mainly depends on the sampling clock frequency.

The ADC has been measured for different input frequencies in the audio band. Figure 4.27 shows the FFT measured for frequencies between 100Hz and 20kHz with a $-36dBV$ tone to evaluate the frequency response. The sensitivity variation

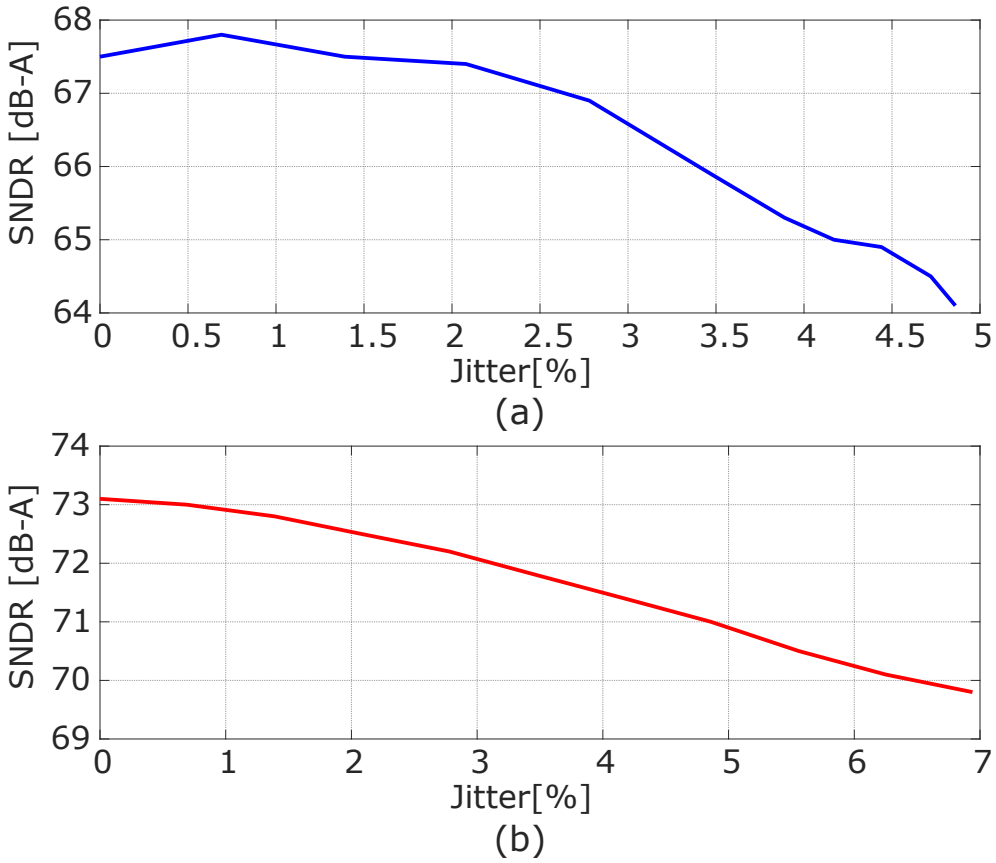

FIGURE 4.23: Measured SNDR v.s. Clock Jitter (a) LP mode and (b) NM mode.

is less than 0.2dB in the whole bandwidth.

The PSRR has been measured for both digital and analog supplies using a 1kHz interfering tone. The worst case measured PSRR is 77dB in NM for the analog supply. The PSRR for the digital supply exceeds 85dB for both modes. These measurements show the robustness of the pseudo differential VCO-ADC against power supply fluctuations even using single ended inverters in the ring oscillators.

In Table 4.4, the ADC is compared with other recent audio ADC chips. To compare the performance of a digital microphone ADC, we consider that the particularities of MEMS microphones must be evaluated in addition to the Schereier FoM. We must distinguish if the ADC is directly compatible with a high output impedance MEMS (as happens in our design) or not, because otherwise a buffer circuit is required whose power consumption would have to be added in the FoM evaluation. Also the dynamic range for microphones is evaluated differently than in conventional ADCs, as it is defined between 0dB of SNDR and the acoustic overload point of the microphone, where SNDR is mainly limited

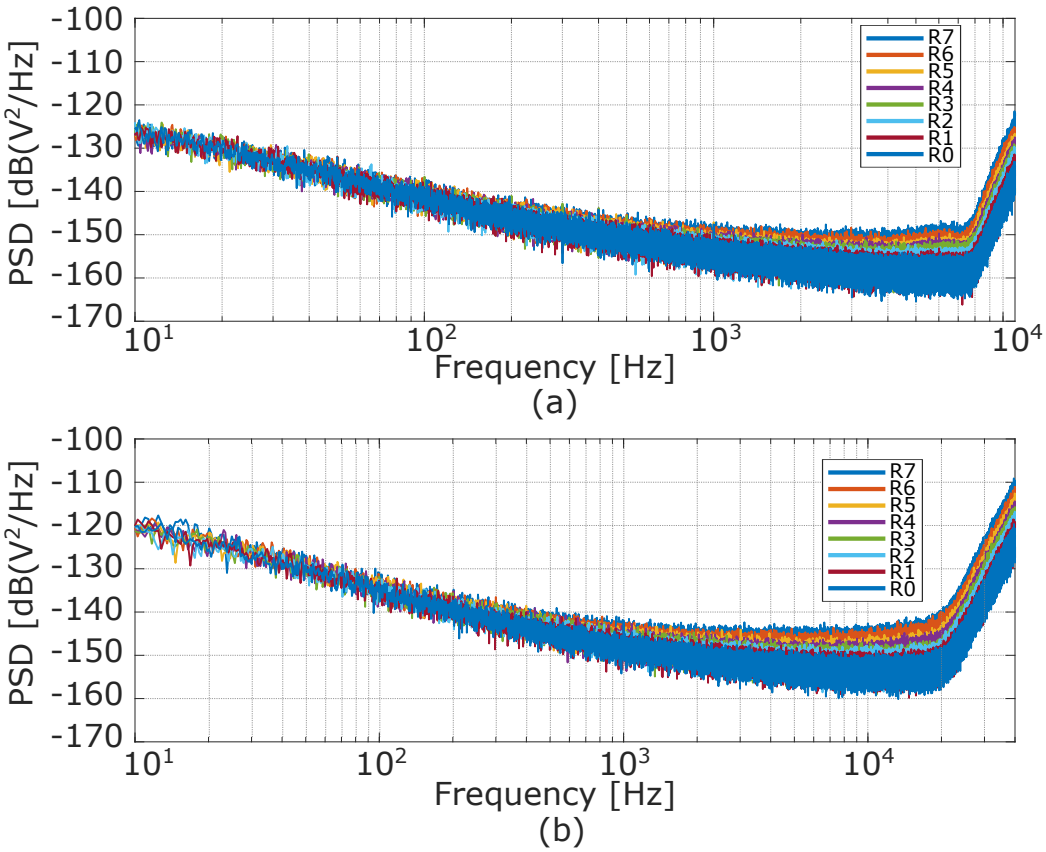

FIGURE 4.24: Noise floor (a) clock frequency 768kHz and (b) clock frequency 3072kHz

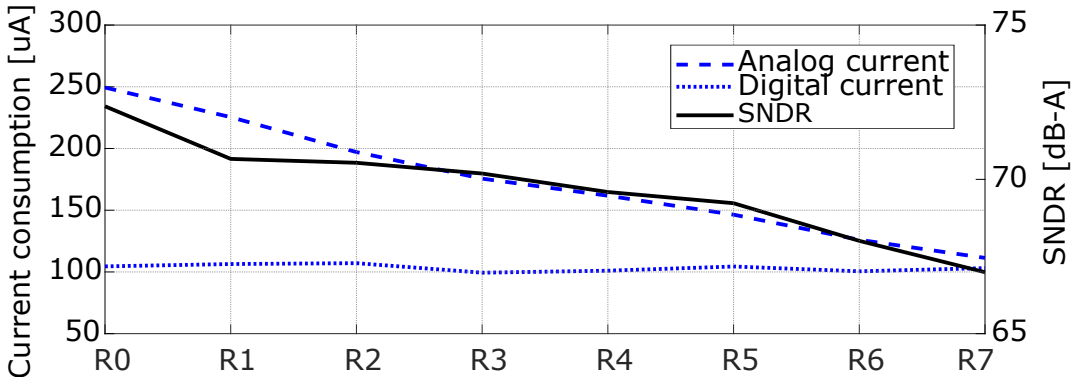

FIGURE 4.25: SNDR v.s. resistor array values at CLK=3072kHz.

by distortion. For these reasons a row has been added in the table indicating the type of input coupling circuit of the ADC whether it is a sampling capacitor (like in switched capacitor sigma-delta modulators), resistive (like in continuous time sigma-delta ADCs) or high impedance (Hi-Z) and therefore compatible

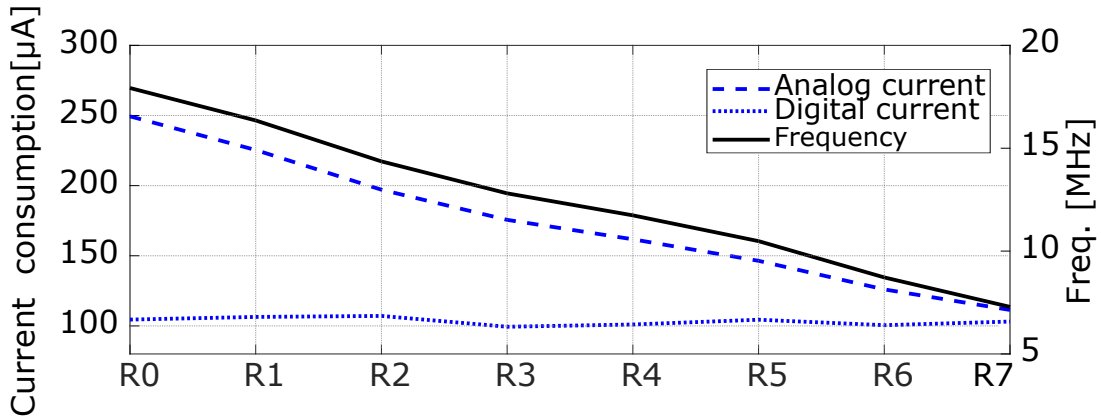

FIGURE 4.26: Rest frequency v.s. resistor array values at CLK=3072kHz.

with a capacitive MEMS. Two other rows have also been added with the Schreier FoM calculated using both the dynamic range and the peak SNDR. Observing the comparison, only two ADCs are directly compatible with a Hi-Z sensor like in the presented chip [40], [74]. In addition, the resolution (considering thermal, flicker and quantization noises) of the design is only matched by the ADC in [79] which would require an additional voltage buffer to offer the same features than the presented ADC.

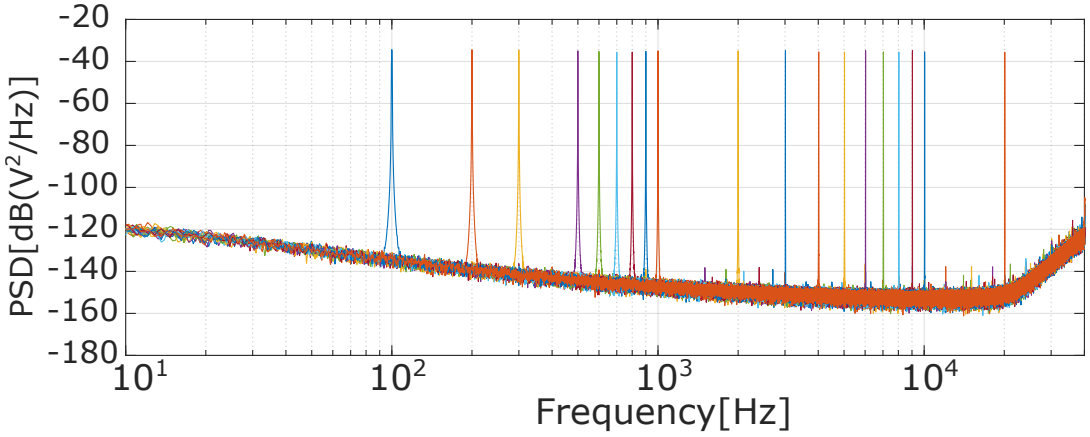

FIGURE 4.27: FFT plot for several input frequencies.

Parameter	**This work**		[74]	[40]	[79]	[71]	[80]	[76]	[81]	[82]
Integration Domain	**Time**		Time	Time	V	V	V	Time	V	Time
Topology	**Open loop**		2nd-ord	Op. loop	CTSD	CTSD	CTSD	1st-order	Incremental	VCO
Techonlogy[nm]	**130**		65	130	160	180	65	65	65	130
Area [mm2]	**0.14**		0.075	0.04	0.27	0.64	0.39	0.11	0.13	0.04
Supply (A/D) [V]	**1.5/0.95**		1.2/0.8	1.2	1.8	1.8	1.2	1	1.2	1.8
Power [uW]	**148.6**	**438.1**	4.25 - 5.8	240	440	265	139	142.6	550	560
Input	Hi-Z		Hi-Z	Hi-Z	Sampling	Resist.	Resist.	Resist.	Sampling	Resist.
Sampling f. [kHz]	**768**	**3072**	200	2400	3500	6100	7.2	2000	10240	20000
Bandwidth [kHz]	**8**	**20**	1	20	20	24	24	20	20	20
PSRR[dB]	77	77	83		89		86	83		
SNDR [dB]	**80.26**	**80.31**	92.3	73.8	106.5	100.9	100.9	94.2	100.8	76.6
DR [dB]	**104**	**108**	92.3	97	109.8	104	104.8	100.3	101.8	98.5
SFDR [dB]			110.3	85			113.7	115.6	121	60
FOM sndr [dB]	157.6	157	174.3	153	183	180.5	183.3	175.7	176.4	152.1
FOM dr [dB]	**181.3**	**184.6**	174.7	176.2	186.4	183.6	187.2	181.8	177.4	174

TABLE 4.4: Performance comparison

Part III

Linerization of open-loop VCO-ADCs by Frequency-to-current converters

Chapter 5

Feedback loop linearization with FDR and gain stages

In Part II of this dissertation a VCO-ADC based microphone was presented. Linearity was improved by optimizing the design and choosing a SF as the high input impedance interface with the MEMS. The ADC was not completely linear, unlike a Sigma-Delta ADC, but this was of no concern, as the typical microphone specifications allow some level of distortion at high amplitudes. This enabled the optimization of the dynamic range of the converter, achieving the required SNR at low amplitudes, and having enough linearity at high amplitudes, by a less steep roll-off. While this provided a good VCO-ADC for MEMS microphones, the use of the optimized SF+VCO might not be enough when moving to lower supply voltages or for applications with more exigent specifications when it comes to distortion at high amplitudes. Thus in this part we will discuss the linearization of ring-oscillators using a component that demodulates the oscillator output and turns it into a low frequency current. Thanks to this component that was already mentioned in Chapter 3, and that have been called in this dissertation frequency-dependent-resistor, or FDR, we can implement negative feedback around the oscillator, linearizing it. As outlined in Chapter 3 this technique has some advantages over conventional closed-loop VCO-ADCs, mainly due to the fact that the sampling is performed outside of the loop. This mean that the FDR feedback oscillator is equivalent to an open-loop VCO and it can use the same frequency-to-digital converters. For instance the coarse-fine architecture of the chip of Chapter 4 could be directly used in an FDR feedback RO.

In the present and following chapters, some circuits using the FDR and a RO oscillator will be discussed, focusing on circuits to implement linear ring oscillators. The linearization thanks to the negative feedback and frequency response and noise behaviour will be analyzed. Also in the present chapter and chapter 6, the theoretical developments will be silicon proven.

5.1 Frequency to current conversion using a time-varying switched capacitor circuit

A switched capacitor circuit that converts a frequency into a current is depicted in Fig. 5.1. It consists of replacing a resistor (Fig. 5.1 (a)) with a capacitor and two switches controlled by two non-overlapping signals, Φ_1 and Φ_2, as shown Fig. 5.1 (b) and (c). The operation principle of the circuit is to transfer a constant charge per clock cycle from a fixed voltage source in and out of a capacitor. The non-overlapping clock phases guarantee a time independent charge transfer. The capacitor is connected alternately between node 1 (V_1), and node 2 (V_2). The switched capacitor circuit is equivalent to a resistor whose value is determined by the switching frequency.

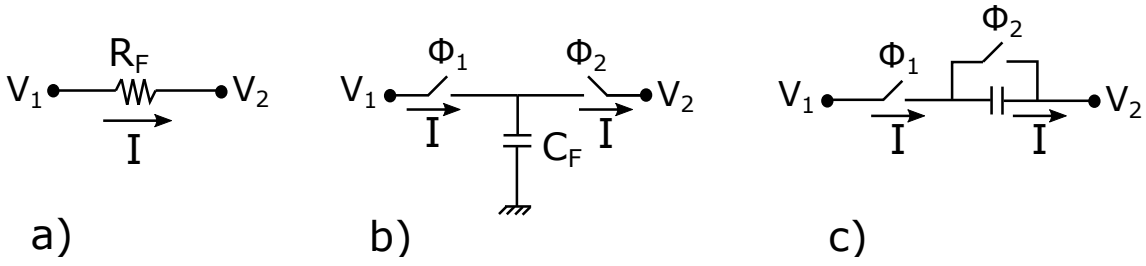

FIGURE 5.1: Switched capacitor based resistor circuit.

When Φ_1 turns ON (Φ_2 turns OFF) the voltage across C_F is V_1 and the charge Q equals $V_1 \cdot C_F$. When Φ_2 turns ON (Φ_1 turns OFF), $Q = V_2 \cdot C_F$. The equivalent average current through C_F during every clock cycle is:

$$I_{avg} = \frac{\Delta Q}{\Delta T} = f_{osc} \cdot C_F \cdot (V_1 - V_2) \tag{5.1}$$

The average current for the equivalent resistor circuit, as Ohm's law states, is:

$$I_{avg} = \frac{V_1 - V_2}{R_F} \tag{5.2}$$

Equating (5.1) and (5.2) equation, we have:

$$R_F = \frac{V_1 - V_2}{f_{osc} \cdot C_F \cdot (V_1 - V_2)} = \frac{1}{f_{sw} \cdot C_F} \tag{5.3}$$

By using a switched capacitor as an equivalent resistor, we can tune the current by changing the conductance value linearly dependent on the switching frequency. That is, the circuit of Fig. 5.1 can be considered a frequency-dependent resistor or FDR. We will use this characteristic to demodulate the signal from the VCO and convert it into a current directly proportional to $f_{osc}(t)$, according to (5.1).

In Fig. 5.2 the proposed circuit to linearize the VCO is depicted, making use of a feedback amplifier [52]. The average current in the circuit, I_{FDR} is given by:

$$I_{\mathrm{FDR}} = \frac{V_{\mathrm{in}}(t) - V_{\mathrm{X}}}{R_{\mathrm{F}}} = f_{\mathrm{osc}}(t) \cdot C_{\mathrm{F}} \cdot V_{\mathrm{X}} \tag{5.4}$$

where $V_{\mathrm{in}}(t)$ is composed by a time dependent component $V_{\mathrm{s}}(t)$ and a time invariant component V_{CM}, and $V_{+} = V_{\mathrm{ref}}$ by virtual ground constant voltage input. Thus, we obtain the dependence between $f_{\mathrm{osc}}(t)$ from VCO and the circuit input signal $V_{\mathrm{in}}(t)$.

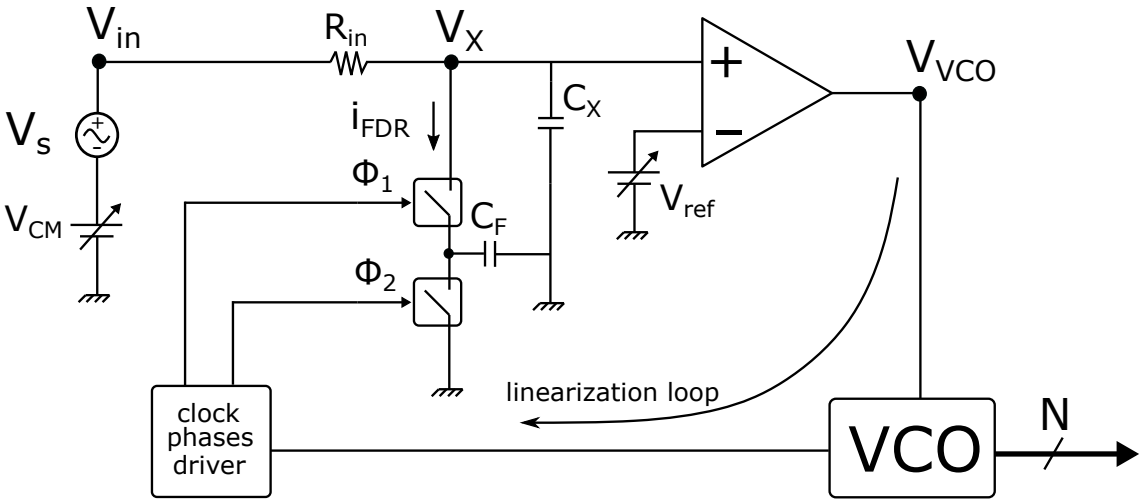

FIGURE 5.2: Proposed circuit to linearize the VCO response.

Combining (1.15) and (5.4), we can separate two components of both equations given by:

$$\frac{V_{\mathrm{CM}} - V_{\mathrm{ref}}}{R_{\mathrm{in}}} = f_0 \cdot C_{\mathrm{F}} \cdot V_{\mathrm{ref}} \qquad \textit{DC component}, \tag{5.5}$$

$$\frac{V_{\mathrm{s}}(t)}{R_{\mathrm{in}}} = k_{\mathrm{VCO}} \cdot V_{\mathrm{VCO}} \cdot C_{\mathrm{F}} \cdot V_{\mathrm{ref}} \qquad \textit{AC component}, \tag{5.6}$$

where V_{VCO} takes values between 0 and supply voltage V_{DD} of the operational amplifier in circuit of Fig. 5.2. Note that (5.5) provides a bias current for the FDR. Alternatively, this bias current can be provided by a current source.

Finally, we have an expression (5.7) which defines the $f_{\mathrm{osc}}(t)$ of the VCO totally independent of the VCO control voltage (V_{VCO}) and the VCO gain (k_{VCO}), and linearly dependent to the circuit input signal ($V_{\mathrm{in}}(t)$). The non-linearity of the VCO is corrected because the gain of the FDR feedback oscillator only depends on linear components R_{in} and C_F. This approximation is true providing that the loop gain is much bigger than one, which will be the case when using an operational amplifier.

The final $f_{\mathrm{osc}}(t)$ for the proposed circuit is:

$$f_{\mathrm{osc}}(t) = \frac{1}{R_{\mathrm{in}} \cdot C_{\mathrm{F}} \cdot V_{\mathrm{ref}}} \cdot (V_{\mathrm{s}}(t) + V_{\mathrm{CM}} - V_{\mathrm{ref}}) \tag{5.7}$$

A remark on the implementation of the FDR in Fig. 5.1 is needed. In Fig.5.1, the FDR is controlled by a non-overlapping signal. An alternative is to control both switches directly with the oscillator output signal (after a LS), avoiding the clock phases drivers. Controlling the FDR in this manner causes a contention current during the switching. The main effect is that the current through the FDR is increased above the value given by (5.4). As the voltage in V_X is kept constant by the loop, the transistors implementing the switches see the same operating point during each switching event, so the amount of extra charge taken from C_X each transition is constant among transitions. Due to this the average amount of extra charge is dependent on the switching frequency. So, as long as the value on V_X does not vary too much, the effect is equivalent to having another resistor in parallel, i.e, is equivalent to having a higher capacitor C_F. Due to this we will avoid the use of non-overlapping driving phases for the rest of this dissertation and simply control the FDR with the oscillator output signals. This way the need of a dedicated circuitry to generate the non-overlapping clocks and the power associated with it is avoided.

5.1.1 Circuit implementation of the FDR

Figure 5.3 a) shows the implementation of the FDR using a simple CMOS inverter and a capacitor C_F. As mentioned above this implementation does not use a non-overlapping clock at the penalty of increasing the power consumption of the FDR. The problem is moot as the size of the capacitor can be reduced to compensate. This can be done by programming the FDR capacitance value to compensate PVT variations in the on resistance of the FDR MOS transistors. For instance an array of capacitors can be use in the FDR. Then the number of capacitors connected to the FDR is digitally controlled as explained later in Section 7.2.1. Notice that in both Fig. 5.2 and Fig. 5.3 the FDR is connected between the positive node of the operational amplifier and ground. This is possible because as shown by (5.3) the FDR resistance, R_F is reduced when the driving frequency is increased. This means that when the output frequency is increased as a consequence of an increase in node V_X, the FDR draws more current from V_X implementing a negative feedback loop. An advantage of connecting the FDR in this manner is that we can spare the reference voltage buffer to supply the FDR without PSRR penalty.

Figure 5.3 b) shows an alternative circuit to that of Fig. 5.3 a) where the input resistor has been substituted by a transconductor (GM). By doing so, we can make the FDR feedback oscillator fully MEMS compatible due to its high input impedance. In a differential implementation, the current source and GM can be

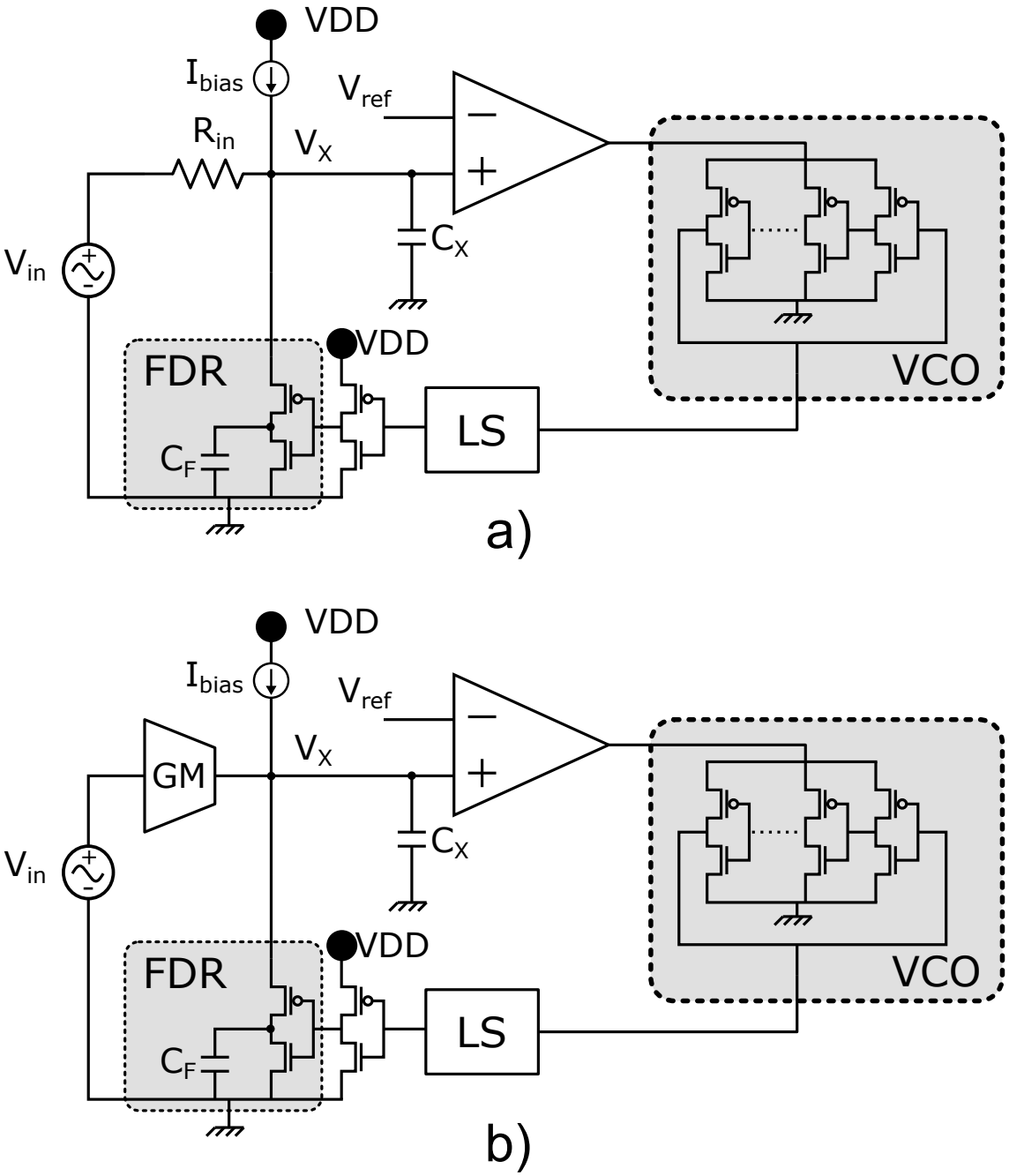

FIGURE 5.3: Transistor implementation of the FDR. a) with input resistor b) with GM input.

merged as in a GM driven open-loop CCO (see Fig. 4.3). This allows the use of the GM bias current to also bias the FDR which improves power consumption.

5.1.2 The switching ripple problem

All the previous discussion is based on the condition of a constant voltage in V_X. This voltage is stabilized by the loop and kept constant in average. The key word here is in average. At the switching frequency of the FDR, the voltage in V_X changes as charge is pulled out of the node to charge capacitor C_F. This causes a ripple at V_X that has a frequency equal to the FDR switching frequency. Increasing the size of capacitor C_X helps reducing the ripple, and guarantees that the input pair of the operational amplifier and the bias current source (or resistor) are kept in the correct bias value.

Another way to reduce ripple takes advantage of the presence of several output phases in the ring oscillator. Splitting the total capacitance C_F in several FDRs with capacitors with proportional sizes and connecting each FDR to an output phase of the oscillator, reduces the size of the ripple and increases its frequency. This greatly helps on mitigating the problem.

5.2 Linearity correction

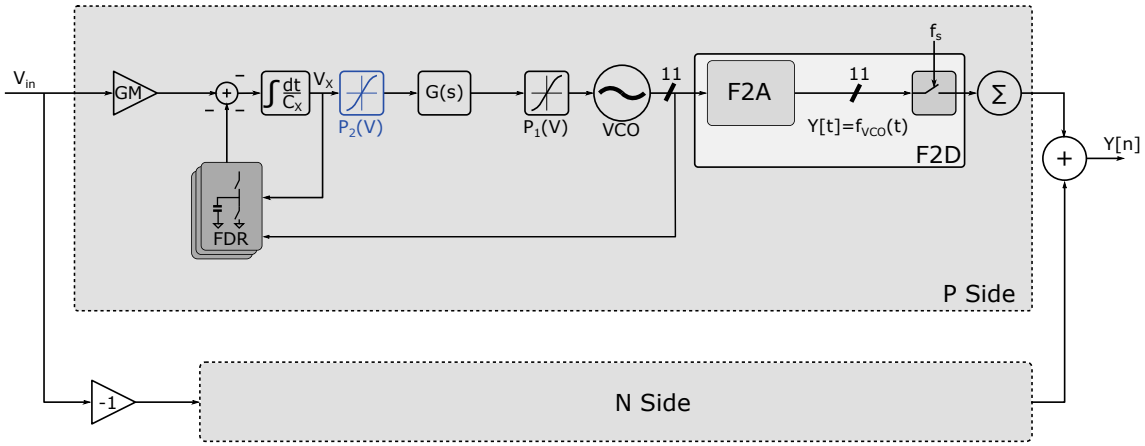

FIGURE 5.4: Block diagram of the FDR feedback oscillator for distortion analysis.

Fig. 5.4 shows a block diagram of the linearization technique shown in Fig.5.2. The diagram includes polynomials $P_1(V)$ and $P_2(V)$ that model the non-linear responses of the oscillator and the operational amplifier respectively. The polynomial modeling the non-linear gain of the oscillator or tuning curve is given by the following expression:

$$k_{VCO}(V) = k_{VCO} \cdot P_1(V) = k_{VCO} \cdot (V + \frac{a_2}{k_{VCO}} \cdot V^2 + ... \frac{a_n}{k_{VCO}} \cdot V^n) \tag{5.8}$$

Defining the transfer function of a single pole operational amplifier ($G(s)$) as:

$$G(s) = \frac{g_{dc}}{\frac{s}{w_p} + 1} \tag{5.9}$$

The polynomial that models the non-linear gain of the amplifier is:

$$G(V) = g_{dc} \cdot P_2(V) = g_{dc} \cdot (V + \frac{b_2}{g_{dc}} \cdot V^2 + ... \frac{b_n}{g_{dc}} \cdot V^n) \tag{5.10}$$

From the analysis of the circuit in Fig. 5.4 we get that:

$$\frac{\Delta f(t)}{V_{IN}(t)} = GM \frac{A \cdot P_1(v) \cdot P_2(v)}{1 + \beta \cdot A \cdot P(v_1) \cdot P_2(v)} \approx \frac{GM}{\beta} \tag{5.11}$$

With $A = g_{dc} \cdot k_{VCO}$. Equation (5.11) is valid as long as:

$$A \cdot P_2(v) \cdot P_2(v) \cdot \beta \gg 1 \tag{5.12}$$

According to 5.11, the gain of the linearized oscillator is $1/\beta$. The question is now how linear this gain is. On the one hand the GM can either be a source degenerated transconductor like that shown in Fig.4.3 a) or a simple resistor, as in Fig.5.2. Assuming the value of V_X to be nearly constant thanks to the feedback loop, both can be considered linear GMs. On the other hand, using equation 5.1 in the circuit of Fig.5.4, we can calculate β as:

$$\beta = \frac{i_{FDR}}{\Delta f(t)} = V_X \cdot C_{FDR} \tag{5.13}$$

Again, as the loop keeps the value of V_X constant, we can see that β does not depend on the input signal, and represents a linear gain. From equations 5.11 and 5.13 we see that the proposed circuit linearizes the nonlinear gain of the VCO in the same way that feedback in an amplifier.

In order to analyze the effectiveness of the linearization, some simulations have been performed. The simulation have been done at system level, using a model of an oscillator and a model of the FDR. The rest of the blocks used have been gains, transfer function blocks, sampling blocks and suming blocks. The non-linearity of the oscillator has been introduced using a polynomial fit of data from circuit level simulations. The simulated system is identical to Fig. 5.4 without polynomial $P_2(V)$. Only distortion from the oscillator has been analyzed.

The model of the FDR used in the simulations is depicted in Fig. 5.5 a). It consists on an integrator and a gain $1/C_F$ that represents the capacitor of the FDR. The switch on resistance is represented by R_{Sw}. The current charging and discharging the capacitor is i_{C_F}. Switch SW_1 alternatively connects node V_1 to either Ct_1 (representing ground) or node V_2. The latter represents the node to which the FDR is connected, in the diagram of Fig. 5.4, that would be V_X. The value of node V_1 is then subtracted from the value of node V_3 and the result is converted into current i_{C_F} by gain $1/R_{Sw}$. Finally, switch SW_2 alternatively

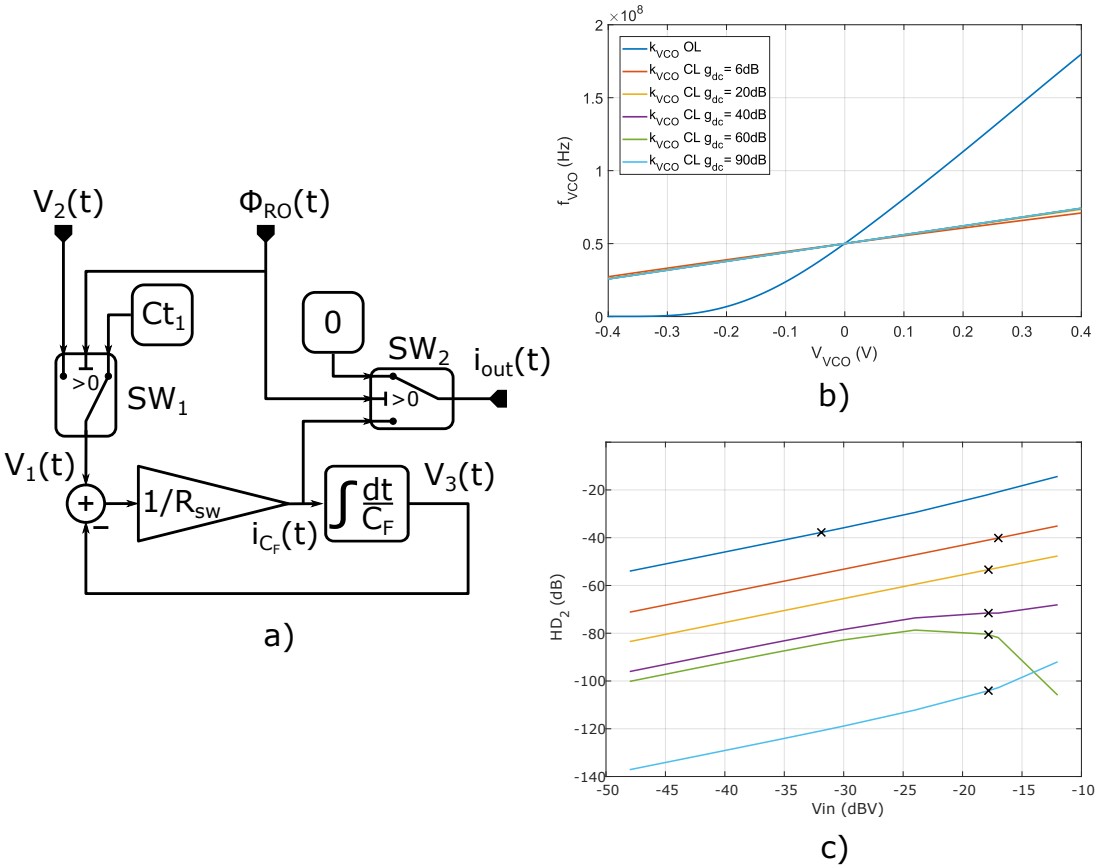

FIGURE 5.5: a) Simulation model of the FDR. b) Simulated tuning curves. c) Simulated HD_2, with marks in equal output power points.

connects i_{out} to either zero or current i_{C_F}. This switch works in a way that the output current is equal to i_{C_F} when the integrator is charging to V_2, and zero when the integrator is discharging to Ct_1. With this model, the currents and voltages of the FDR can be simulated like in a circuit simulation, without second order effects like the finite off resistance of transistors or the aforementioned contention current during switching if we do not use non-overlapping phases to control the FDR.

Figure 5.5 b) shows the k_{VCO} of an open-loop VCO and of an FDR feedback oscillator for different amplifier gains. From this plot is evident that the linearization technique reduces the k_{VCO}, as could be expected due to the similarity with an amplifier with negative feedback. This new oscillator gain is clearly more linear than that of the open-loop oscillator, but it is difficult to asses the effect of the amplifier gain. Fig. 5.5 c) shows distortion coefficient HD_2 of all the oscillators for different input voltages. From this plot it is clear that the open-loop oscillator shows the worst HD_2. For those with feedback, it can be observed that the higher the gain the better the HD_2 value. But a question arises from these plots: is the lower gain the only reason for linearity improvement? Otherwise we could we

get the same results by attenuating the input signal. To answer these questions a series of points with the same output power in the fundamental tone has been marked with black crosses. This is equivalent to equalize the gains of all the oscillators, in a similar way to the comparison we made in Fig. 4.5. Looking at these points, it is evident that by using feedback we are linearizing the oscillator, as HD_2 clearly improves. Nevertheless, looking at the the red line, that corresponds to the lower amplifier gain, we see that the gain is critical to improve the HD_2, as this small gain of 6dB barely improves the linearity compared to the open-loop oscillator. This is to be expected by checking at (5.11) and (5.12), because with low amplifier gains (i.e, low A, as the amplifier gain g_{dc} is included in it), the condition in (5.12) is not fulfilled.

From the equations 5.11 and 5.12, and the results of the simulations in Fig. 5.5 b) y c), we can conclude that the FDR feedback oscillator behaves like a circuit with negative feedback when it comes to compensate the non-linear tuning curve of the oscillator.

5.3 The FDR as a FM to PFM modulator

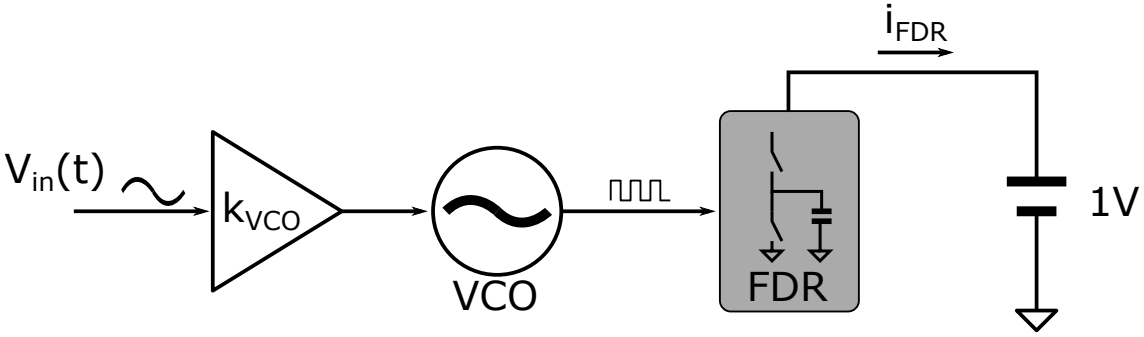

FIGURE 5.6: Circuit for the simulation of the FDR as a FM to PFM modulator.

At the beginning of the chapter it was mentioned that the FDR demodulated the oscillator output signal. The output signal of the oscillator is frequency modulated (FM). As it is well known an FM signal does not have information in the baseband. Only a DC component is present if the carrier signal has a DC level, as it is the case for a ring oscillator that outputs a square wave signal from 0 to V_{VCO}. But no information of the modulating signal is present. If we just feedback the output of the oscillator in FM, we could not compensate the non-linearity of the oscillator as we are not feeding back anything at the frequency of the input signal.

We need to demodulate this FM signal, so we have a tone at the frequency of the input tone (the modulating signal), f_{in}. The FDR performs this demodulation

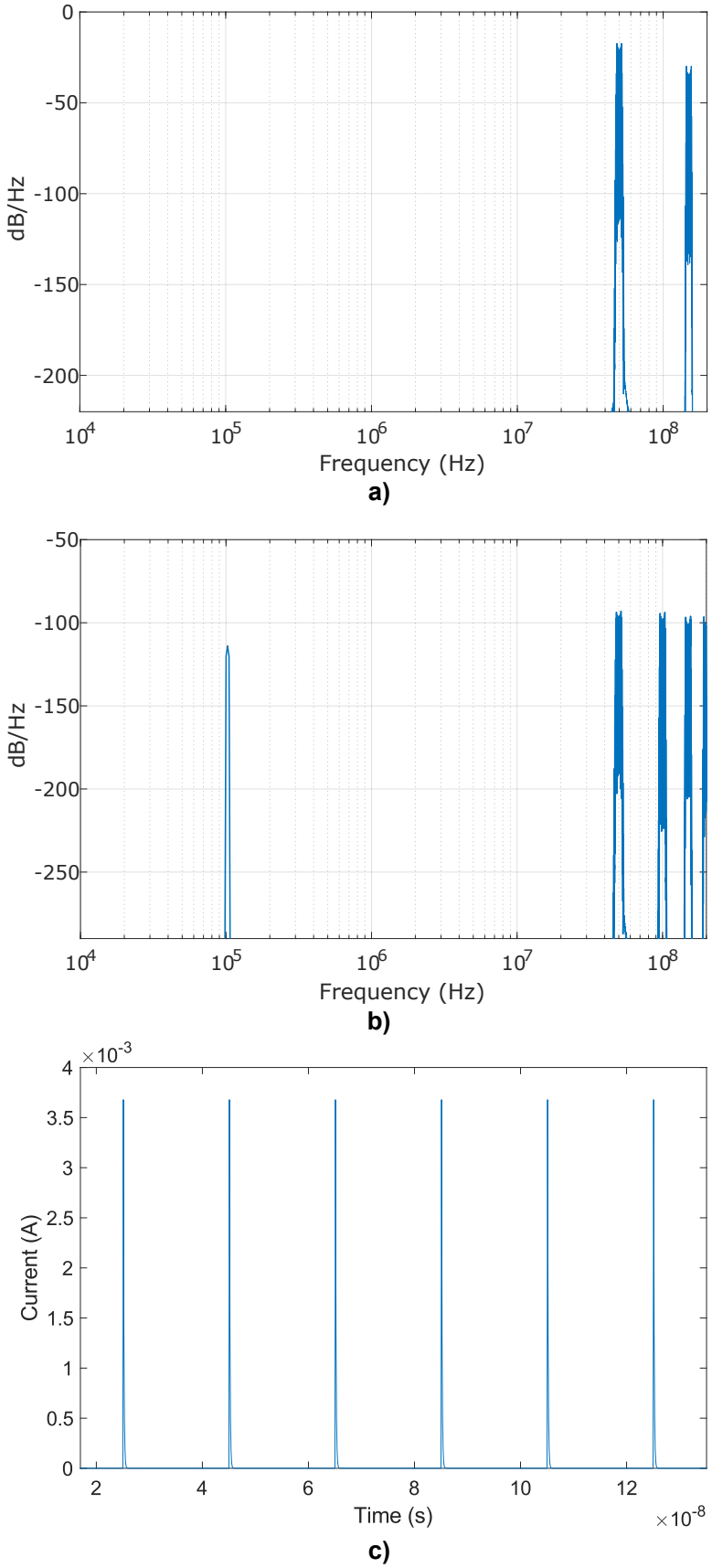

FIGURE 5.7: a) Spectrum of the FM output of the oscillator. b) Spectrum of the PFM output of the FDR. c) Current pulses of the FDR.

by converting the FM signal of the oscillator into a PFM current that is then subtracted from node V_X. This can be shown by simulating the circuit of Fig. 5.6 and looking at the spectrum of i_{FDR}. Figure 5.7 a) shows the spectrum of the FM output of the oscillator. As can be seen, only the modulation side-bands are present and there is no information at f_{in} (That is equal to 10kHz for this simulation). Figure 5.7 b) shows the spectrum of current i_{FDR}. This is a PFM spectrum, and shows both the modulation side-bands and the input tone at $f_{in} = 10kHZ$. Finally, Fig. 5.7 c) shows a plot of i_{FDR}. The current i_{FDR} is a train of current pulses. The area under each pulse given by the integral es equal to the charge stored in C_X each falling edge pulse coming from the oscillator and equal to:

$$Q_{pulse} = C_F \cdot V_X \tag{5.14}$$

This charge is discharged to ground with each rising edge as described in Section 5.1. Thus the output current of the FDR can be modeled as a PFM signal with pulses with height equal to (5.14). The FDR can be seen then as a FM to PFM converter.

5.4 Frequency response

Although the FDR feedback oscillator is a linear periodic time variying system (LPTV) [83], here we are going to make a small signal approximation to a linear system so we can analyze the frequency response. This assumption is supported by the fact that the oscillation frequency is far from the signal bandwidth in a RO-ADC for MEMS microphones.

From the above discussion we know that the FDR can be modeled as a FM to PFM converter. Remembering from Chapter 3 that the RO-ADC can be represented using a PFM model [18] and ignoring the polynomials, we can model the diagram of Fig. 5.4 as shown in Fig.5.8 a). This figure shows the PFM model where the F2D has been represented as in Fig.3.4 and the FDR as a falling edge detector whose output is multiplied by the voltage at node V_X and the value of C_F (i.e. the charge taken by the FDR with each falling edge).

To analyze only the base-band behaviour of the unsampled modulator, we can use the model shown in Fig.5.8 b), where the sampler and block H(s) have been omitted and both edge detectors (the one from the F2D and the one from the FDR) has been represented as a single one. As we are only interested in analyzing the behaviour of the base-band we will ignore the PFM modulation sidebands by placing a brick-wall low-pass filter. Analyzing the effects due to the modulation sidebands of the oscillator linearized by the FDR feedback is out of the scope of this dissertation and will be left for future works. Once we have eliminated the modulation sidebands, and there is only the spectral content in the base-band, we can define the small signal model of Fig.5.8 c) (Note that $V_{ref} = V_{XDC}$). In the model of Fig.5.8 c), R_F is the average FDR resistance as given by 5.3. From this

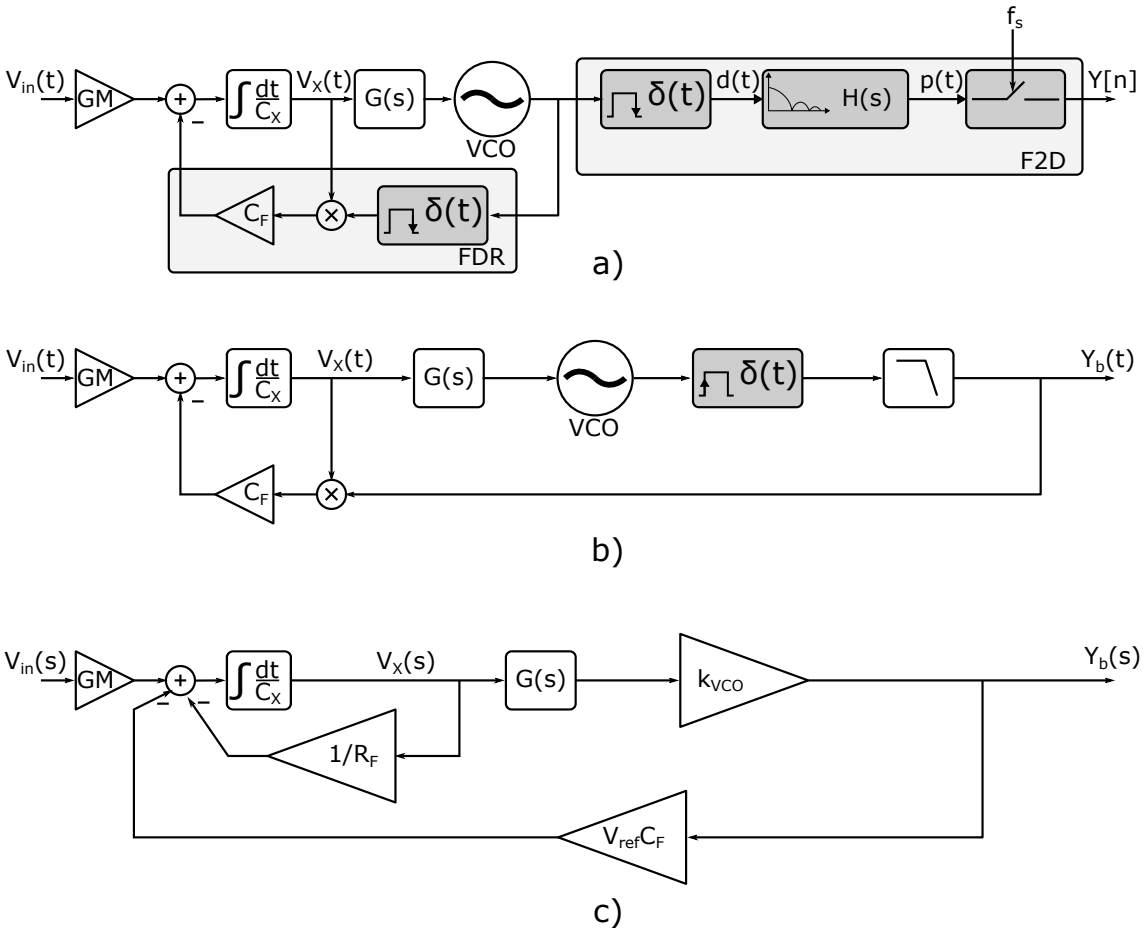

FIGURE 5.8: a) PFM model of the diagram of Fig. 5.4. b) Base-band output model. c) Small signal model of the diagram of Fig.5.4.

model we can obtain the transfer function of the system and analyze its frequency behaviour. The transfer function from input to output is given by:

$$\frac{Y_b}{V_{in}}(s) = \frac{GM \cdot G(s) \cdot k_{VCO}}{sC_X + V_{ref} \cdot C_F \cdot G(s) \cdot k_{VCO} + f_0 \cdot C_F} \tag{5.15}$$

Assuming a single pole amplifier as given by:

$$G(s) = \frac{G_{dc} \cdot \omega_p}{s + \omega_p} \tag{5.16}$$

Equation 5.15 becomes:

$$\frac{Y_b}{V_{in}}(s) = \frac{GM \cdot G_{dc} \cdot k_{VCO} \cdot \omega_p}{s^2 C_X + s(C_X \cdot \omega_p + f_0 \cdot C_F) + V_{ref} \cdot C_F \cdot G_{dc} \cdot k_{VCO} \cdot \omega_p + \omega_p \cdot f_0 \cdot C_F} \tag{5.17}$$

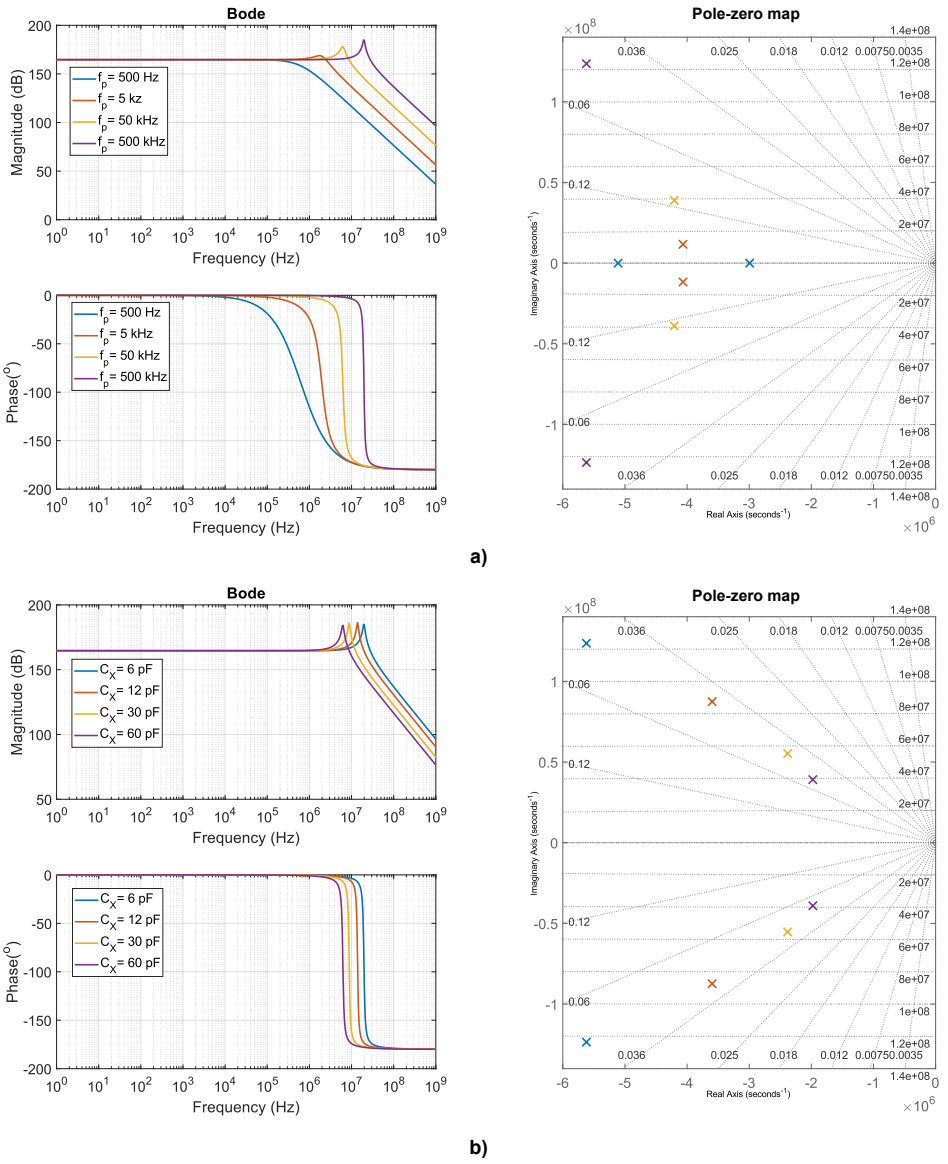

FIGURE 5.9: a) Bode and pole-zero diagrams of (5.17) sweeping parameter a) f_p b) C_X.

This is a second order transfer function where the natural frequency and damping factor are given by:

$$\omega_0 = \sqrt{\frac{(V_{ref} \cdot C_F \cdot G_{dc} \cdot \omega_p \cdot k_{VCO}) + (\omega_p \cdot f_0 \cdot C_F)}{C_X}} \tag{5.18}$$

$$\zeta = \frac{C_X \cdot \omega_p + f_0 \cdot C_F}{2\sqrt{C_X \cdot \omega_p \cdot C_F \cdot (V_{ref} \cdot k_{VCO} \cdot G_{dc} + f_0)}} \tag{5.19}$$

Parameter	Value	Parameter	Value
GM	$0.167mS$	k_{VCO}	$300MHz/V$
G_{dc}	$40dB$	ω_p	$3.14 \cdot 10^6 rads/s$
f_p	$500kHz$	C_F	$972fF$
C_X	$6pF$	V_{ref}	$1V$

TABLE 5.1: Parameters used to obtain the Bode and pole-zero plots of Fig. 5.9

From (5.18) it can be seen that the frequency of the complex-pole pair increases with C_F, ω_p, k_{VCO}, G_{dc}, f_0 and V_{ref}, while it decreases with C_X. Equation 5.19 is more difficult to interpret. To understand the parameter dependence of the frequency response of the system of Fig.5.8 c), a series of parametric sweeps of (5.17) were run. Results follows.

Bode and pole-zero plots of equation 5.17 are shown in Fig. 5.9. Table 5.1 shows the base parameters used to obtain the frequency response. Figure. 5.9 a) shows the Bode and pole-zero plots of (5.17) when the amplifier pole frequency is swept from 500Hz to 500kHz. As the frequency of the amplifier pole is increased the frequency of the complex pole-pair is also increased as can be seen from both the bode and pole-zero plots. Also looking at the pole-zero plot, it can be observed that when the amplifier's pole frequency increases, the damping ratio decreases, making the system more underdamped.

The results of sweeping parameter C_X are shown in Fig. 5.9 b). We can see from both the bode and the pole-zero plot that by increasing the value of C_X the frequency of the complex pole-pair of equation 5.17 is reduced. When it comes to the damping ratio, this looks constant. The result is not surprising, as for (5.19), we can see that the damping ratio approximately increases with the square-root of C_X. This mean, that C_X must be significantly increased to affect the damping ratio. This effect is actually similar to the sweep of ω_p. The difference is that changes in ω_p can be much bigger.

Other parameters that have been sweep are G_{dc}, C_F and k_{VCO}. The three of them have the same effect, i.e. when increasing their values, the frequency of the complex-pole pair is also increased. In regards to the damping ratio, this is decreased as the parameters are increased, except for the case of C_F, which approximately increases with the square-root of C_F as for the case of C_X . Increasing C_F also decreases the gain at low frequency. The amplifier gain, G_{dc}, deserves an special mention. When keeping the amplifier unity gain frequency (f_u) constant, increasing G_{dc} does not affect the frequency of the complex-pole pair. Nevertheless, the damping ratio is still decreased when G_{dc} increases.

Recalling the discussion at the beginning of the chapter about implementing the FDR without non-overlapping clock, we might ask how the extra current drawn by the FDR for each switching event affects the frequency response. This extra current is equivalent to having a resistor (R_{leak}) in parallel with the FDR.

Then the resistance of the FDR given by (5.3) must be corrected:

$$R_X = \frac{1}{f_0 \cdot C_F} // R_{leak} \tag{5.20}$$

Taking the effect of this resistance into account, expression 5.15 and 5.17 become respectively:

$$\frac{Y_b}{V_{in}}(s) = \frac{GM \cdot G(s) \cdot k_{VCO}}{sC_X + V_{ref} \cdot C_F \cdot G(s) \cdot k_{VCO} + \frac{1}{R_X}} \tag{5.21}$$

$$\frac{Y_b}{V_{in}}(s) = \frac{GM \cdot G_{dc} \cdot k_{VCO} \cdot \omega_p}{s^2 C_X + s(C_X \omega_p + \frac{1}{R_X}) + V_{ref} \cdot C_F \cdot G_{dc} \cdot k_{VCO} \cdot \omega_p + \frac{\omega_p}{R_X}} \tag{5.22}$$

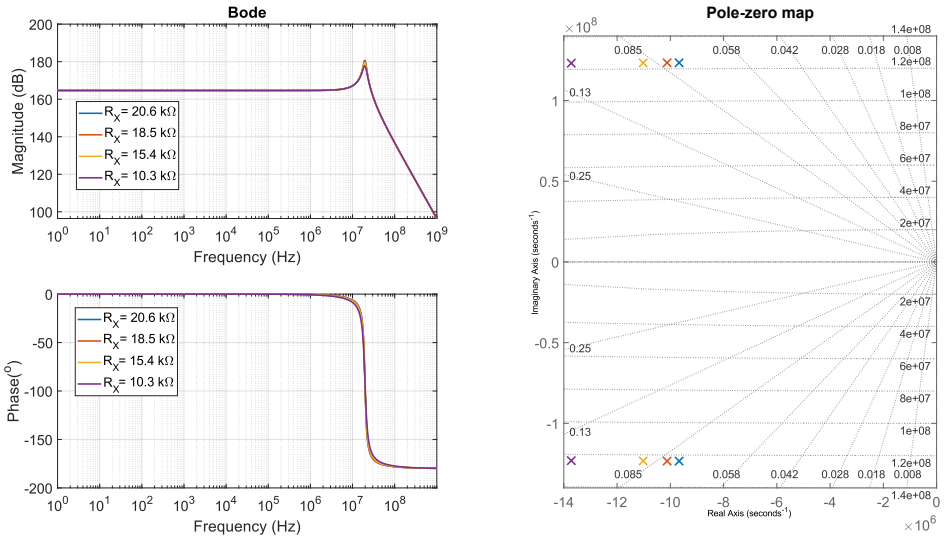

FIGURE 5.10: a) Bode and pole-zero diagrams of (5.17) sweeping parameter R_X.

Calculating (5.22) with the values of Table 5.1 and sweeping R_X between $10k\Omega$ and $1M\Omega$ the bode and pole-zero plots of Fig. 5.10 are obtained. Looking at the pole-zero map, it can be observed that the frequency of the complex pole pair is independent of the value of the parasitic resistance R_X. The effect of the parasitic resistance is limited to the damping ratio, which becomes bigger as R_P increases.

5.4.1 VCO phase noise improvement

Figure 5.11 shows the small signal model of Fig. 5.8 including the noise sources. Four sources of noise are present in this circuit, the oscillator phase noise (PN in Fig. 5.11), the noise from the operational amplifier, i_{nOTA}, the noise from the bias

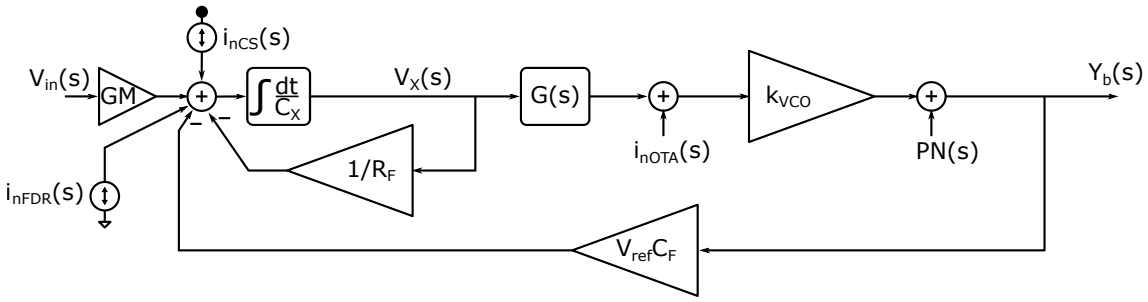

FIGURE 5.11: FDR closed-loop linear model for noise analysis.

current source, i_{nCS}, and the noise from the FDR, i_{nFDR}. Notice that the phase noise of the oscillator, PN, is the demodulated phase noise, i.e. the noise from the oscillator at the baseband after the PFM modulation and filtering as described in section 5.3 (See Fig. 5.8 and the associated discussion). Using the demodulated phase noise we can use the small signal model to evaluate the frequency response of the noise from the oscillator. From the small signal model, the PSD of the noise from the oscillator at the output (after the F2D converter) is given by:

$$S_{NY_b}(f) = |H_{PN}(j2\pi f)|^2 S_{PN}(f) \tag{5.23}$$

With $H_{PN}(s)$ being:

$$H_{PN}(s) = \frac{sC_X + f_0 \cdot C_F}{sC_X + V_{ref} \cdot C_F \cdot G(s) \cdot k_{VCO} + f_0 \cdot C_F} \tag{5.24}$$

For a single-pole amplifier, $G(s)$ is given by (5.16). Substituting this in (5.24) we obtain:

$$H_{PN}(s) = \frac{(sC_X + f_0 \cdot C_F) \cdot (s + \omega_p)}{s^2 C_X + s(C_X \cdot \omega_p + f_0 \cdot C_F) + V_{ref} \cdot C_F \cdot k_{VCO} \cdot G_{dc} \cdot \omega_p + \omega_p \cdot f_0 \cdot C_F} \tag{5.25}$$

That is the transfer function seen by the phase noise when the amplifier is implemented with a single pole. Let's now proceed to analyze how changes in different design parameters affect this transfer function. First, G_{dc} is swept keeping the same unity gain frequency of the amplifier, f_u. The results are shown in Fig. 5.12 a). For this plot, the same values of Table. 5.1 are used, except for f_p, that is now calculated to achieve a f_u of 50MHz for each g_{dc}.

Looking at the bode plot of Fig. 5.12 a), we can see that the frequency of the complex-pole pair does not change. This can be confirmed in the pole-zero plot, were the complex poles are located along the same frequency line. What changes is the damping ratio, that decreases as the amplifier gain is increased. Conversely, the second zero (the one given by: $(s + \omega_p)$ moves from higher frequencies to lower frequencies as the gain is increased. This makes the 40dB/decade slope to

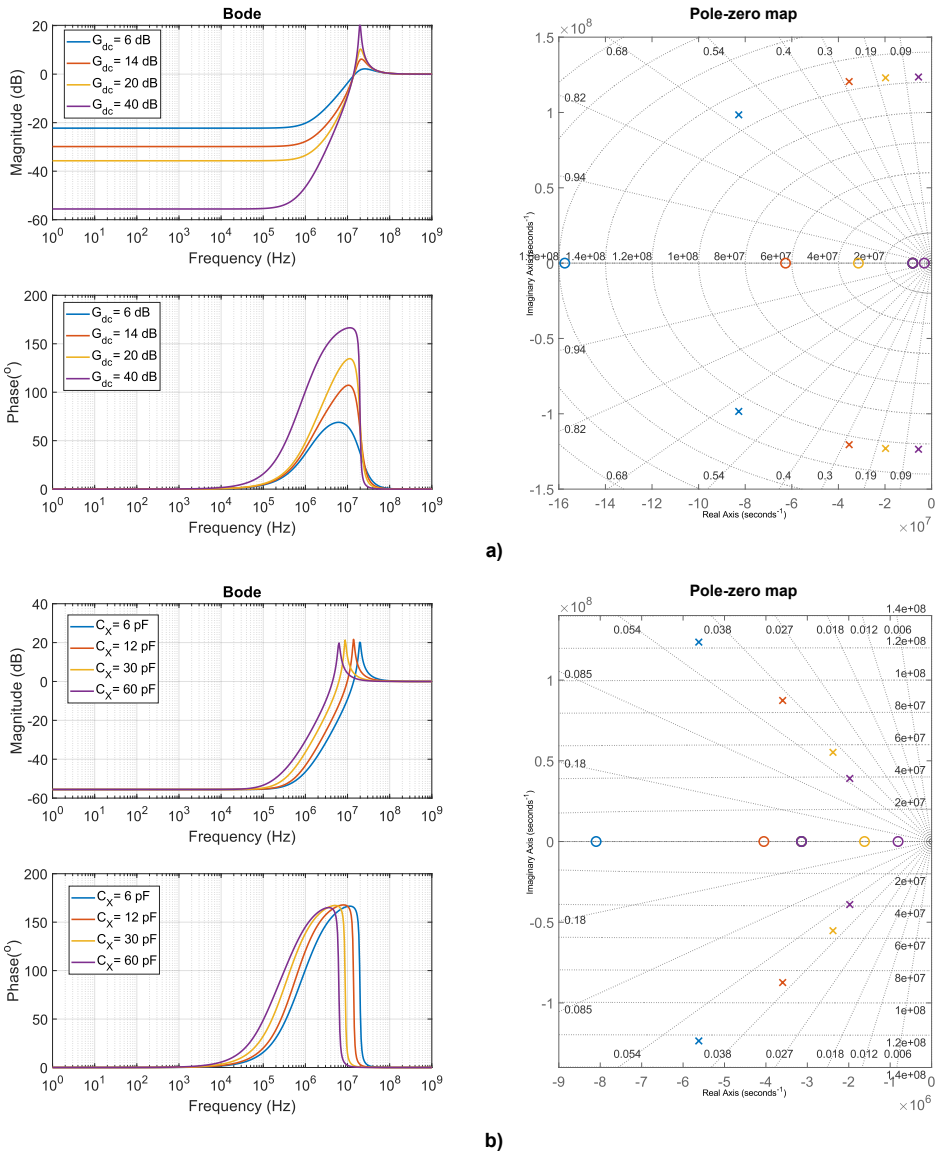

FIGURE 5.12: Bode and pole-zero diagrams of (5.25) sweeping parameter a) G_{dc} at constant f_u b) C_X.

be visible in the bode plot for $G_{dc} = 40$. The effect of this is to increase the noise attenuation at lower frequencies, as the amplifier gain is increased. When the pole of the amplifier is keep at the same frequency, the effect is similar, but in this case the complex-pole pair moves to higher frequencies as the gain is increased, while the second zero is now kept at a fixed frequency. As it is evident from 5.25, this behaviour is also found when increasing either k_{VCO} or V_{ref} In both cases the main effect is that the noise in the base-band is decreased as the gain of the amplifier increases. When C_F is increased, the complex-pole pair moves to a higher frequency and the system becomes more damped. The zero given by

$(sC_X + f_0 \cdot C_F)$ also moves to a higher frequency. The noise attenuation in the baseband is kept constant.

Regarding the change of the pole frequency of the amplifier, f_p, while the other parameters are kept the same, the effect is that both the complex-pair of poles and the second zero moves to higher frequencies as f_p increases and the system becomes more underdamped. As for the case of the swept of C_F, the noise attenuation in the baseband is constant.

Figure 5.12 b) plots the bode and pole-zero plots of (5.25) for several values of C_X. In this case the effect is the opposite to the one found when changing either G_{dc}, k_{VCO} or V_{ref}. A higher value of C_X reduces the frequency of the complex-pole pair and the zero given by $(sC_X + f_0 \cdot C_F)$. The attenuation of the noise in the baseband is not changed.

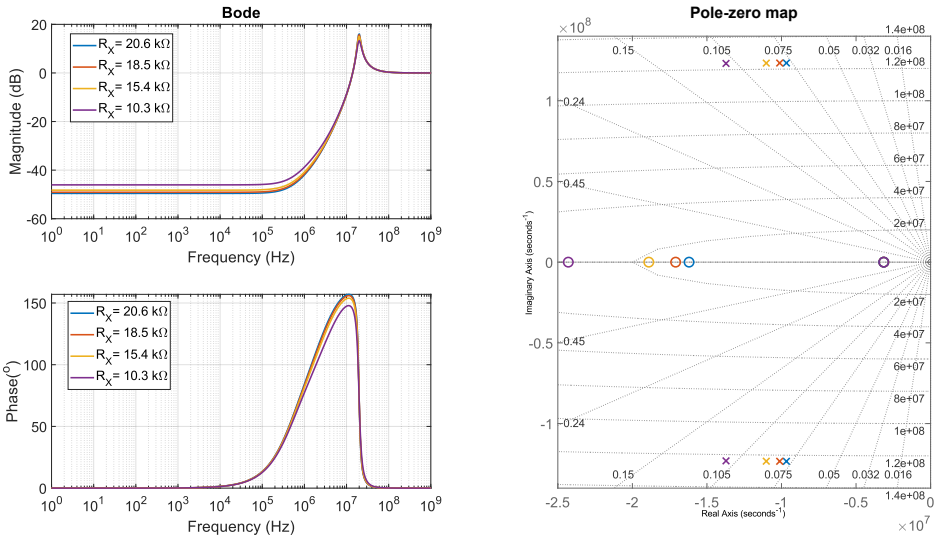

FIGURE 5.13: Bode and pole-zero diagrams of (5.25) sweeping parameter R_X.

To analyze the effects of leakage in the FDR Fig. 5.13 shows the bode and pole-zero plots for different values of R_X using:

$$H_{PN}(s) = \frac{(sC_X + \frac{1}{R_X}) \cdot (s + \omega_p)}{s^2 C_X + s(C_X \cdot \omega_p + \frac{1}{R_X}) + V_{ref} \cdot C_F \cdot k_{VCO} \cdot G_{dc} \cdot \omega_p + \frac{\omega_p}{R_X}} \tag{5.26}$$

As can be seen a smaller R_X (due to more leakage current in the FDR's transistors) moves the first zero to higher frequencies, reducing the noise attenuation. Nevertheless, it is necessary to have a relatively small parasitic resistor to have an appreciable impact. With a more than reasonable value of $1M\Omega$ for the parasitic resistor the noise attenuation is big enough for this not to be a problem.

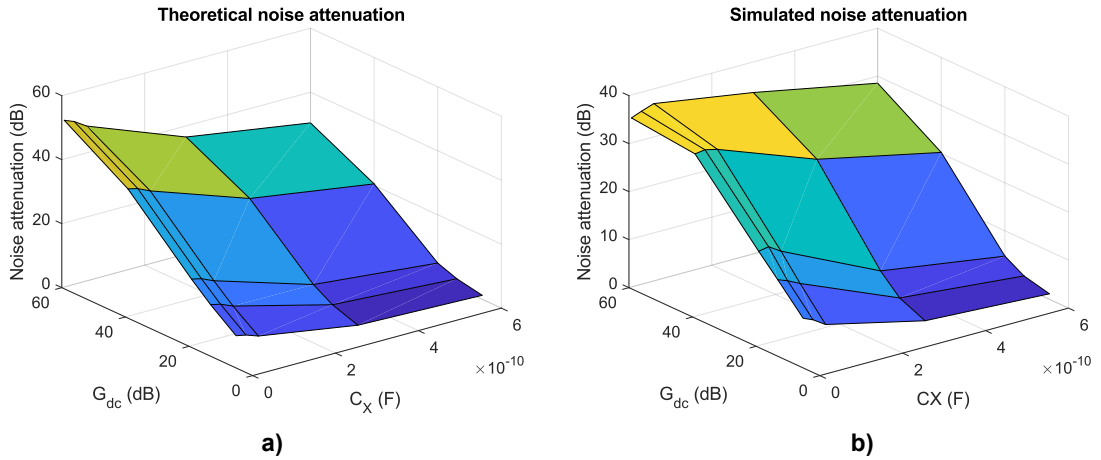

FIGURE 5.14: Noise attenuation for an oscillator with a white noise PSD of -75dB/Hz and parameters from Table 5.1 and several values of G_{dc} and C_X a) Theoretical b) Simulated at system level.

Now we will quantify the phase noise attenuation achieved by the FDR feedback. The in-band noise at the output due to oscillator phase noise for an open-loop RO is given by:

$$IRPN_{OL} = \int_{f_L}^{f_H} S_{PN}(f) \tag{5.27}$$

With f_L being the lower frequency in the bandwidth and f_L being the highest. For the case of the closed-loop implemented with an FDR, the in-band noise at the output is given by:

$$IRPN_{CL} = \int_{f_L}^{f_H} |H_{PN}(j2\pi f)|^2 S_{PN}(f) \tag{5.28}$$

With (5.27) and (5.28) the phase noise improvement in dB thanks to feedback can be defined as:

$$Noiseimprovement(dB) = \frac{\int_{f_L}^{f_H} S_{PN}(f)}{\int_{f_L}^{f_H} |H_{PN}(j2\pi f)|^2 S_{PN}(f)} \tag{5.29}$$

With this definition we can put numbers to the theoretical improvement due to feedback. Figure 5.14 a) shows a 3d graph showing the theoretical noise attenuation when changing G_{dc} and C_X as in Fig. 5.12, for an oscillator with a very high level (-75dB/Hz) of thermal noise. It can be seen that the noise attenuation increases (i.e. we have less noise) when G_{dc} is increased, while the opposite happens when C_X is increased. The noise has been measured for a 200 kHz BW. This is the reason for the increase of noise when C_X is increased. As we can see in

Fig. 5.12 b), when C_X is increased we move the noise transfer function roll-off into the bandwidth. To validate these theoretical results, a simulation at system level with the model of the FDR shown in Fig. 5.5 has been performed where the values of G_{dc} and C_X has been swept like in Fig. 5.14 a). The results are plotted in Fig. 5.14 b). There is a good agreement between the theoretical prediction and the simulation except for high amplifier gain G_{dc} and low capacitor C_X value. The reason of this discrepancy is because the noise is attenuated that much that it is covered by the quantization noise, even for such a noisy oscillator. This can be seen in Fig. 5.15 a) where the open-loop noise (green), FDR closed-loop noise (blue) and the open-loop noise multiplied by $|H_{PN}(j2\pi f)|^2$ (red) are plotted. The FDR closed-loop noise decays with a -20d/dec limited by the quantization noise.

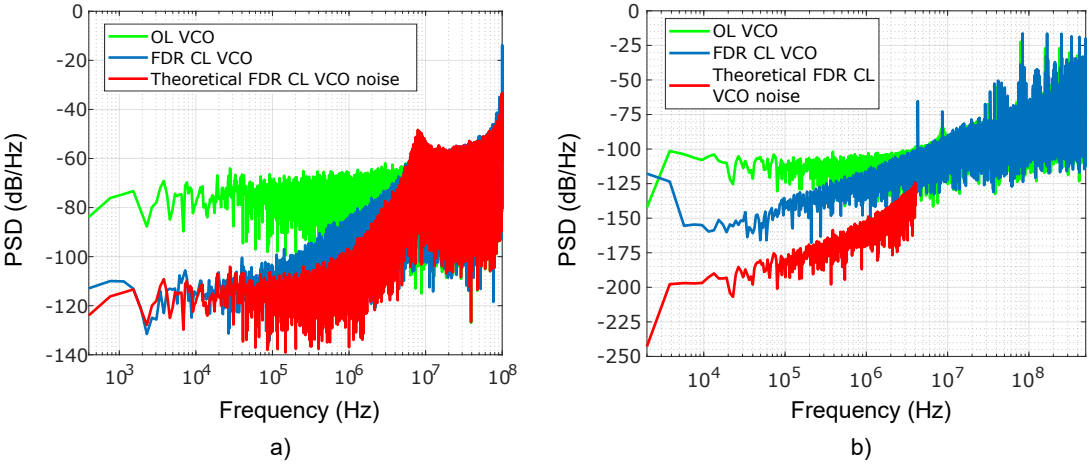

FIGURE 5.15: a) FFTs for point $G_{dc} = 60dB$ and $C_X = 6pF$ of Fig. 5.14 b). Open-loop VCO (green), FDR closed-loop (blue) and theoretical calculation using (5.29) (red). b) FFTs for idle channel circuit level simulation. Open-loop VCO (green), FDR closed-loop (blue) and theoretical calculation using (5.29) (red).

The validity of the aforementioned noise analysis has also been tested with circuit level simulations. Figure 5.15 b) shows the results for a circuit level simulation, for which the oscillator and the FDR have been implemented at transistor level, while the current source and the single-pole amplifier are modeled by ideal blocks (with the transfer function including the pole in the case of the amplifier). The simulation performed is an idle channel measurement, i.e. without signal, only thermal noise. The gain of the amplifier is 90 dB and $f_p = 1.6kHz$. The oscillator has 11 taps and a $k_{VCO} = 275MHz/V$. Eleven FDRs are connected to the oscillator, with capacitors $C_F = 88.36fF$. Capacitor C_X has a value of 6 pF and $f_0 = 40MHz$. Green line shows the PSD for the oscillator in open-loop. The product of this PSD by $|H_{PN}(j2\pi f)|^2$ in the bandwidth is plotted in red. To calculate $H_{PN}(s)$ the effect of the leakage resistance has been taken into account. The results of the simulation with an FDR feedback (i.e. in non-sampled closed-loop)

are plotted in blue. It can be seen that the 20dB/dec slope from the shaping of the quantization noise continues for low frequencies, covering the phase noise.

Another noise that is modified by the feedback is the noise from the operational amplifier, as it is also added inside the loop. If we refer the noise of the amplifier V_{nOTA} to the same point were the phase noise is added (i.e. after the oscillator), then (5.24) to (5.25) can be used to calculate the noise from the oscillator at the output. To do so, we have to convert V_{nOTA} into phase noise. But as we are working with demodulated phase noise, that means according to Fig. 5.11 multiplying V_{nOTA} by k_{VCO}. Then the transfer function from the amplifier noise to the output is given by:

$$H_{opamp}(s) = H_{PN}(s)k_{VCO} \tag{5.30}$$

Thus the amplifier noise improvement is given by:

$$Noiseimprovement(dB) = \frac{\int_{f_L}^{f_H} S_{opamp}(f)}{\int_{f_L}^{f_H} |H_{opamp}(j2\pi f)|^2 S_{opamp}(f)} \tag{5.31}$$

It is clear from (5.30) that the higher the open-loop k_{VCO} the worse the amplifier noise at the output. The other two noise sources present in Fig. 5.11 are the noise from the bias current source (or resistor) and the noise from the FDR. These noise sources see the same transfer function that the signal (divided by the GM, that is not present in the path for the current source and FDR noises) and thus are not modified by the feedback. The noise transfer function of the FDR and CS are given by:

$$H_{FDR}(s) = H_{CS}(s) = \frac{G(s) \cdot k_{VCO}}{sC_X + V_{ref} \cdot C_F \cdot G(s) \cdot k_{VCO} + f_0 \cdot C_F} \tag{5.32}$$

5.5 Experimental validation : Chip DOC2

In this section a 130nm CMOS chip using the architecture depicted in Fig.5.3 is described. The chip has been designed, fabricated and measured. The main goal of this design is to test the analog structure to implement a linear VCO in this chapter. Thus, the digital processing required to implement a VCO-ADC has been omitted.

5.5.1 Chip architecture

The architecture of the analog core of the chip is shown in Fig.5.16. Aside from the analog core the chip contains some ancillary circuits. These are two low-dropout regulators (LDO), a band-gap reference (BG) and output buffers. The two LDOs are used to regulate both the analog and digital supply. As previously mentioned,

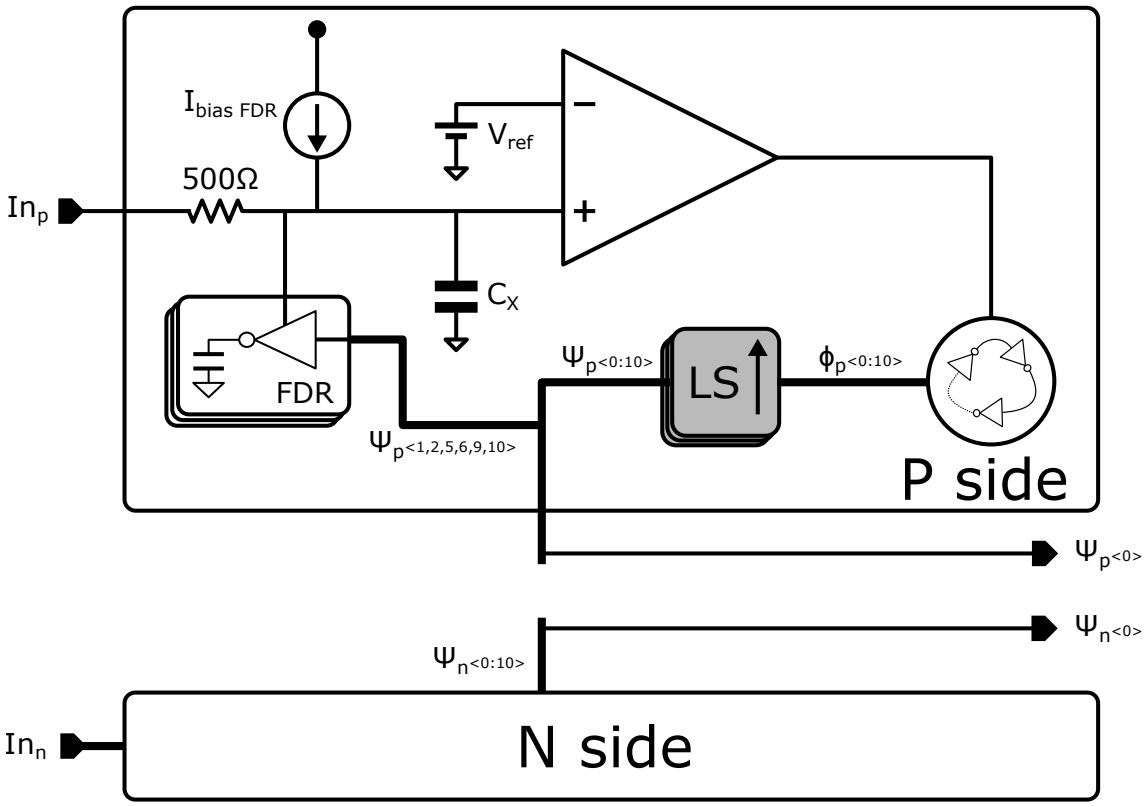

FIGURE 5.16: Circuit level schematic of chip DOC2

the focus of this chip is to test the analog core circuit, so no digital circuitry has been designed to decode the ring oscillator output. One output of each, P side and N side oscillators, has been taken outside the chip through a digital buffer. The digital LDO has been used to regulate the supply of the aforementioned digital buffer and the level-shifters (LS) used to reconstruct full digital values at the output of the oscillator eliminating the effect of the envelope. The chip has programming feature through an SPI port. The circuits used to generate the internal digital control signals are also powered from the digital LDO. The BG is used to generate both reference currents and voltages employed in the different analog components.

Returning to the analog core shown in Fig.5.16 the similarities with the circuit of Fig.5.3 are evident. Two differences can be observed. The first and more clear is the addition of a second signal path in order to implement a pseudo differential architecture. The second difference is the use of several FDRs connected to different oscillator phases. A total of six FDRs have been connected to six different CCO phases. The CCO has a total of 11 phases. This increases the effective frequency of the ripple generated by the FDR in $V+$, thus allowing to reduce the size of capacitor C_X required to effectively attenuate the ripple for a given total FDR capacitance. In the designed chip, the value chosen for C_X is 6pF.

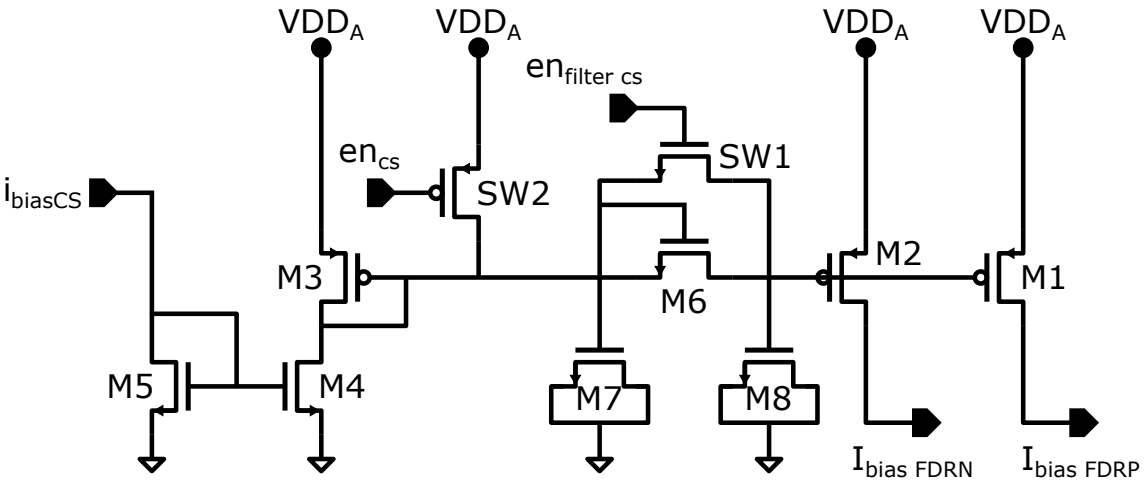

FIGURE 5.17: Schematic of the bias current source of chip DOC2

It is also worth noting that the input resistance used to convert the input voltage to a current has been placed off-chip in the test PCB. Only a small 500Ω resistor has been placed in the chip to protect the gate of the differential pair transistors in the operational amplifier. Finally, V_{ref} is a 1V reference voltage generated by the BG. This voltage is feed to both sides of the pseudo differential architecture, so any coupled noise is common mode noise and thus rejected. Nevertheless, different filter has been placed before both connections to further reduce any noise.

5.5.2 Circuit design

Figure 5.17 shows a detailed schematic of the FDR bias current source that generates $I_{biasFDR}$. The current source has two outputs, $I_{biasFDRP}$ and $I_{biasFDRN}$, for each of the two branches of the pseudo-differential architecture. Each of these currents has a value of $52.5\mu A$, and is generated by transistor M1 and M2. These two transistors copy the current in M3, which is generated by the current mirror formed by M4 and M5. This current mirror receives a $210nA$ reference current from the BG, named I_{biasCS}.

Transistors M6, M7 and M8 implement a π low pass filter to filter out any noise coming from M3, M4, M5 and the BG reference. M6 implements a high-ohmic resistor, while M7 and M8 implement each one a capacitor. Transistor SW1 is a switch used to bypass this filter after power up, allowing to quickly set the gate voltage of transistors M1 and M2. Once this gate voltage has been set, SW1 is opened during normal operation. This switch is controlled by signal $en_{filterCS}$. Another switch, SW2 is used to turn-off the current source. By doing this, the chip can be tested using the input resistor to set the current $I_{biasFDR}$. The control signal for SW2 is en_{CS}.

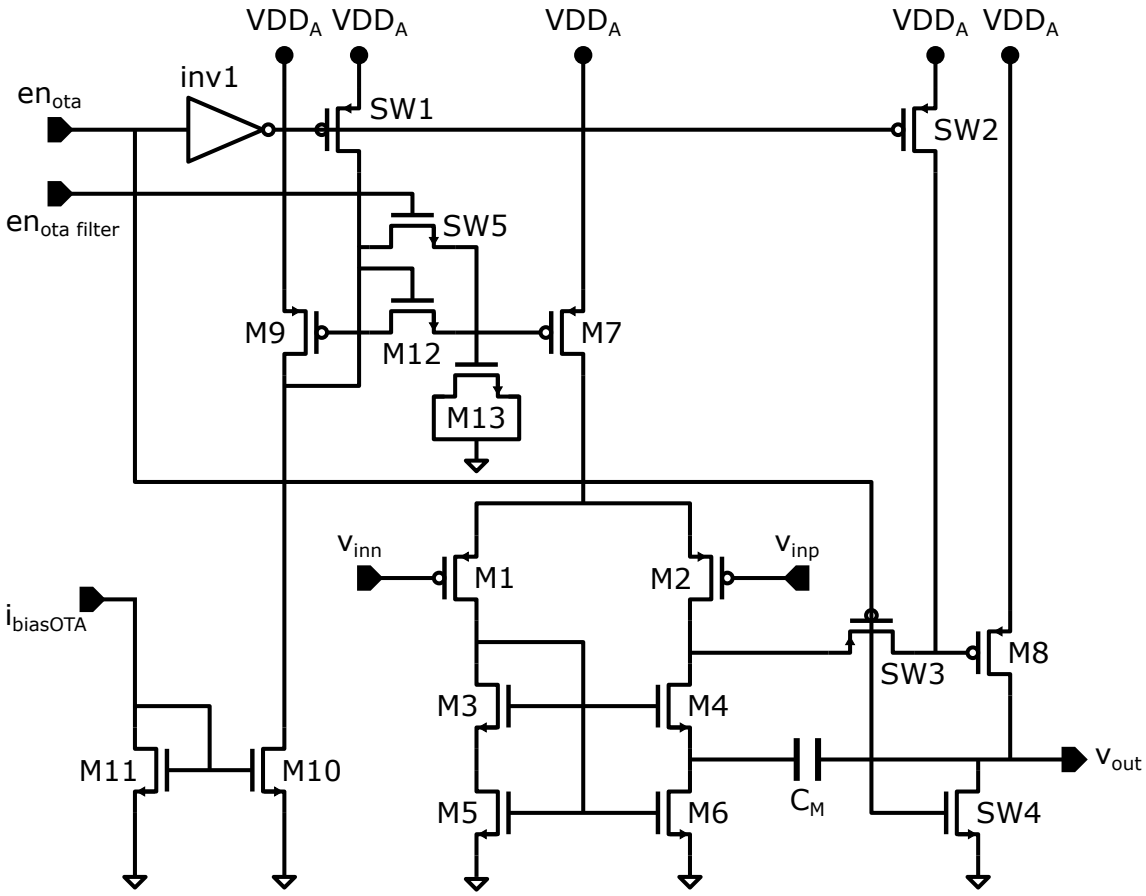

FIGURE 5.18: Schematic of the operational amplifier of chip DOC2

The operational amplifier circuit is shown in Fig.5.18. It is a two stages Miller operational amplifier. The first stage is a differential pair composed by transistors M1 and M2 as input transistors, transistors M3, M4, M5 and M6 as the active load, and transistor M7 as the tail current source. Each of the pairs, M3-M5 and M4-M6, form a long length transistor, separated in two for layout purposes. Splitting them allows the implementation of indirect feedback compensation [84], [85], by connecting the Miller capacitor, C_M, to the point between M4 and M6. This permits us to spare the zero-nulling resistor, and allows for the use of a smaller Miller capacitor. The size of the capacitor C_M is 6.5pF.

The output stage of the amplifier is composed only by transistor M8, as the load of this stage is the average resistance looking into the oscillator, R_{RO} (See expression 3.7 and the associated discussion). This way the bias current of the output stage is reused to bias the CCO, reducing power consumption. Transistors M9, M10 and M11 form the current mirror to generate the bias gate voltage of transistor M7 from the BG current reference, similarly to the previously described current source. This BG current reference, *IbiasOTA*, has a value of 210nA. To filter noise from the circuit formed by M9, M10 and M11 a low pass filter has

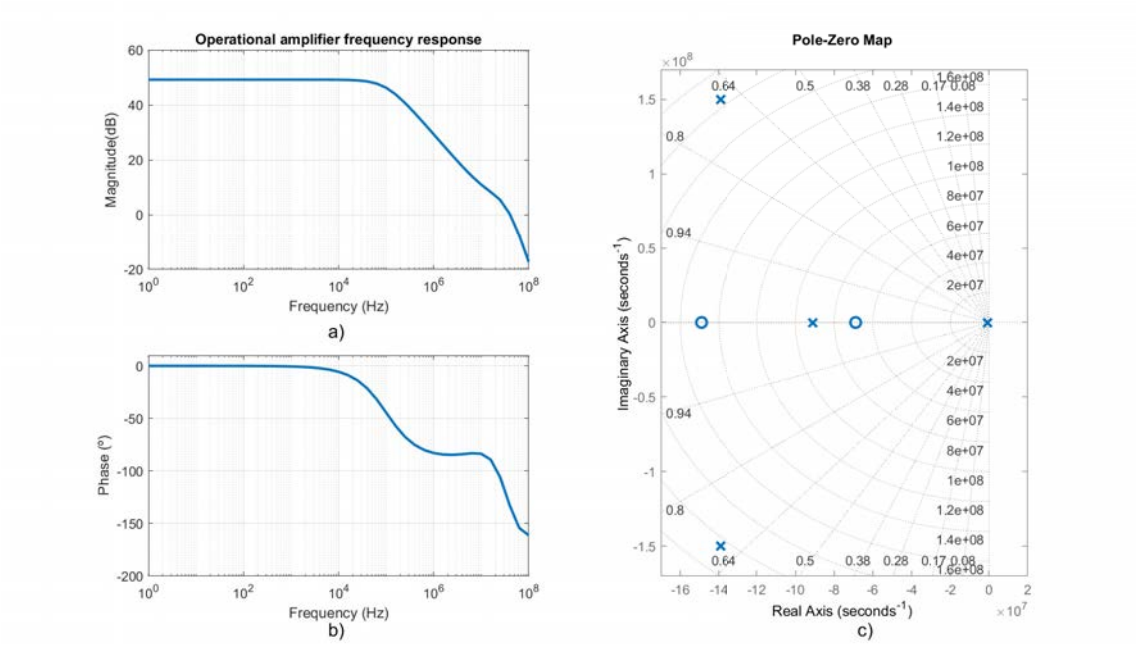

FIGURE 5.19: Frequency response of the operational amplifier of Fig. 5.18 a) Magnitude b) Phase b) Pole-zero plot.

been implemented by transistors M12 and M13. Transistor M12 implements a high-ohmic resistor and M13 a capacitor. Like in the case of the similar filter in the current source of Fig.5.17,a switch, SW5, has been placed to short the filter during power-up. This switch is controlled by signal $en_{OTAfilter}$. The operational amplifier can be turn-off by using switches SW1, SW2, SW3 and SW4, which are controlled by signal en_{OTA}. This signal also stops the oscillator thanks to SW4, that shorts the CCO input to ground. For noise purposes, most current has been allocated in the differential pair of the operational amplifier. This current is 66 μA.

Figure 5.19 shows the frequency response in magnitude (Fig.5.19 a)) and phase (Fig.5.19 b)) of the designed operational amplifier. The gain at low frequencies is 50dB with a unity frequency of 40MHz and a phase margin 47º. The pole-zero diagram is shown in Fig.5.19 c). Sizes of transistors for both the current source of Fig.5.17 and the operational amplifier are shown in Table 5.2.

Figure 5.20 a) shows the schematic of the CCO. It is an inverter based ring oscillator with 11 taps. The delay cells are shown in Fig.5.20 c). Transistors in the delay cell have been sized with relatively small length and width. This is because both linearity and noise requirements in the CCO are alleviated by the feedback loop. The current consumption of the CCO is 13μA with a 0.75V voltage drop. The FDR array is shown in Fig. 5.20 b). It is composed by six FDRs connected to six different phases as shown in Fig. 5.20 b) and Fig. 5.16. The diagram of each individual FDR cell is shown in Fig.5.20 c). Each FDR is implemented with a 162fF capacitor and two switches that alternatively connect this capacitor to

Component	Device	Size (W/L)μm	Device	Size(W/L)μm
Current source	M1,M2	2.6/8 x 50	M3	2.6/8 x 1
	M4	1/7 x 5	M5	1/7 x 1
	M6	2/1 x 1	M8,M8	0.68/1 x 78
	SW1	2/0.6 x 1	SW2	1/0.4 x 1
Operational amplifier	M1,M2	20/0.4 x 30	M3-M6	2.5/7 x 15
	M7	2/1.2 x 240	M8	0.85/1 x 10
	M9	2/1.2 x 4	M10	2.5/3 x 10
	M11	2.5/3 x 2	M12	2/1 x 1
	M13	0.68/1 x 80	SW1-SW3	1/0.4 x 1
	SW4	1/0.4 x 1	SW5	2/0.6 x 1

TABLE 5.2: Device sizes for Fig. 5.17 and Fig. 5.18

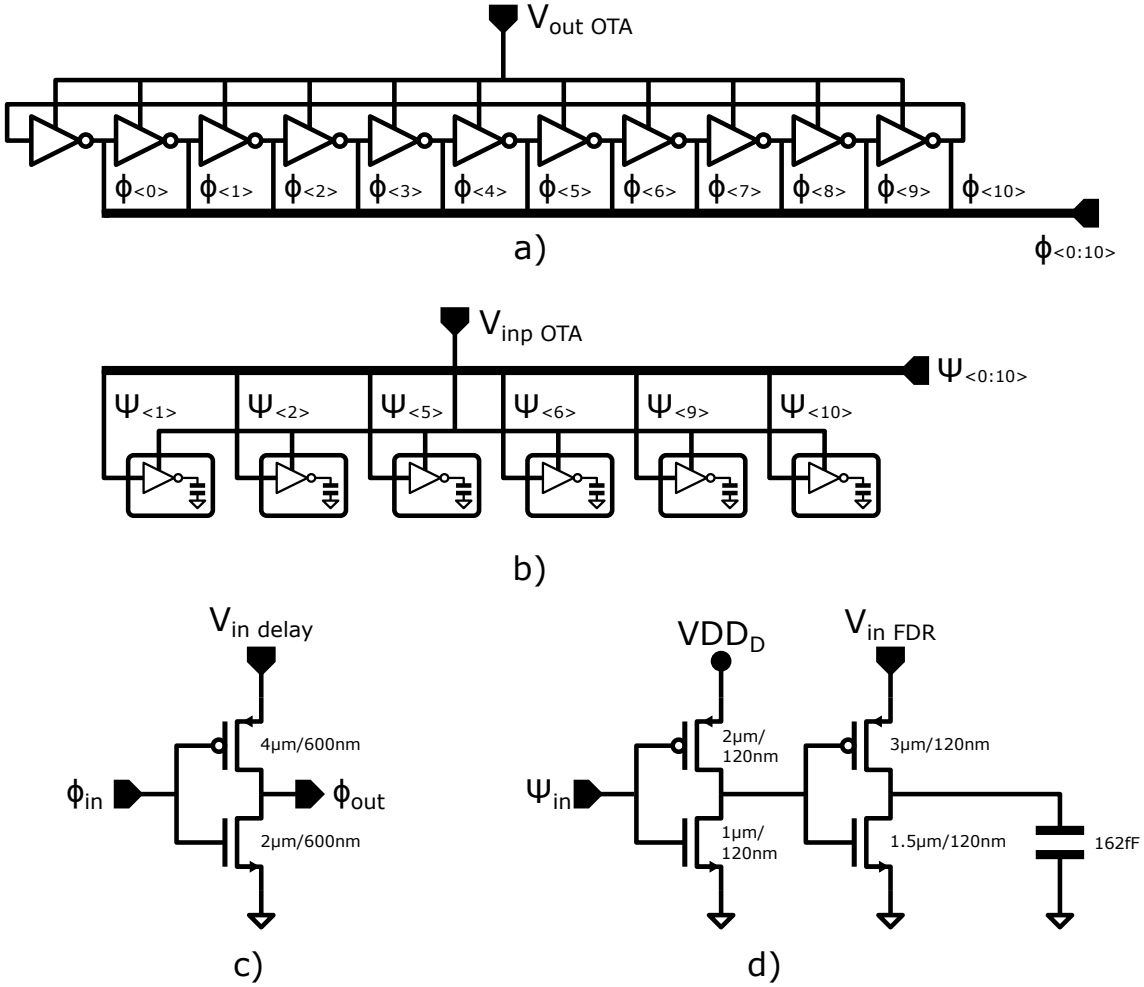

FIGURE 5.20: Schematic a) of the ring oscillator, b) of the FDR array, c) of the delay cells of the ring oscillator, d) of the FDR unit.

V_{inFDR} and ground. In order to drive these switches, an inverter acting as a buffer and connected to the digital supply has been placed.

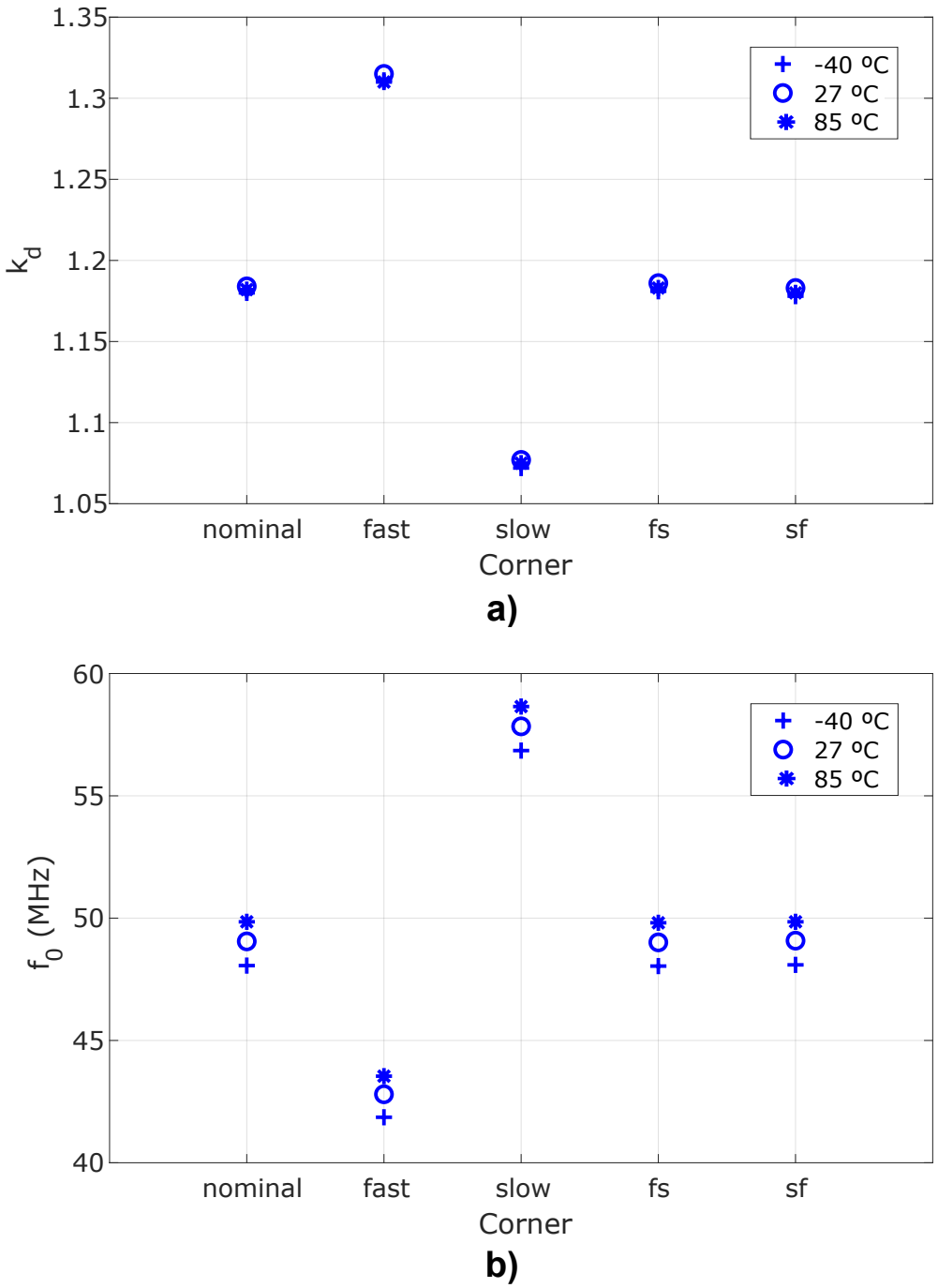

FIGURE 5.21: k_d and f_0 over corners and temperature.

5.5.3 Sensitivity to PVT

Figure 5.21 shows the simulated variation of the k_d and f_0 over corners and temperature. The gain of the oscillator, k_d, shows a very good stability over temperature (Fig. 5.21). The stability over corners is a bit lower. For the rest frequency of the oscillator, f_0, the situation is similar (Fig. 5.21). The rest frequency is less stable than the k_d over corners. In general we can conclude that the FDR feedback stabilized both parameters over PVT variations. The difference of f_0 over corners can be compensate by adjusting the bias current of the FDR properly.

5.5.4 Layout and fabrication

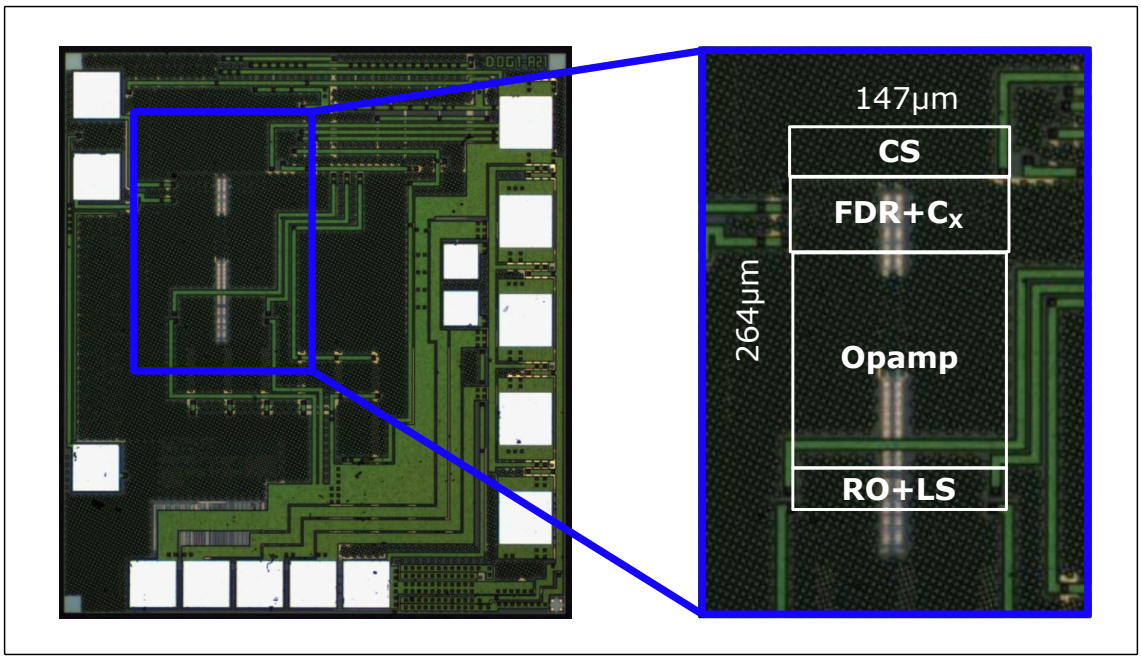

FIGURE 5.22: Micrograph of chip DOC2.

The chip micrograph is shown in Fig. 5.22. The FDR closed-loop oscillator occupies the area marked with a blue rectangle. The lay-out distribution of the different components of the FDR closed-loop oscillator is shown in the detail view on the right. The total area occupied by the designed oscillators is $0.04mm^2$. The largest block is the operational amplifiers, that occupies an area of $0.02mm^2$, i.e half of the area. The block including the FDRs plus the capacitor C_X follows with an area of $0.009mm^2$, mainly due to the size of the two capacitors C_X. The bias current source has an area equal to $0.004mm^2$, while the ring oscillators and the level-shifters occupy a combined area of $0.003mm^2$. The rest of the chip area is occupied by the ancillary circuits and some legacy digital circuitry including the F2D that will not be used in the measurements.

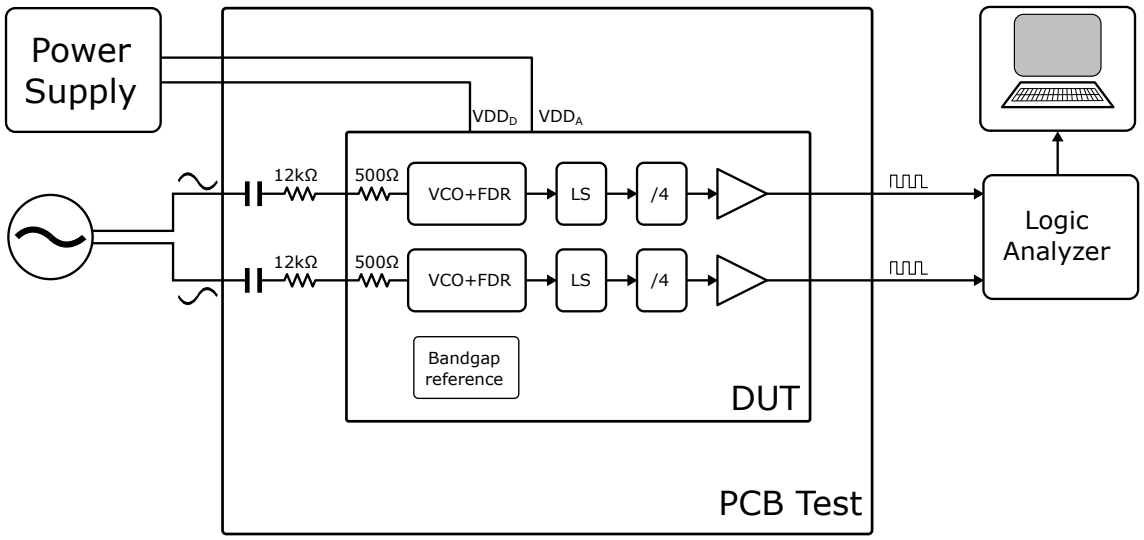

FIGURE 5.23: Test fixture for chip DOC2

The chip has been measured using the text fixture shown in Fig. 5.23. The input signal is generated by a signal generator and AC coupled. The external resistors that convert the input voltage into a current have a value of $6k\Omega$ each. A single oscillator tap per each channel is measured. Before taking these signals out of the chip, a divider by four reduces the frequency to avoid pad ring noise. Both oscillators are sampled at 2 GHz by a logic analyzer. The raw data is then processed in Matlab. As mentioned before, the chip contains an F2D that could be used to perform the measurements and take a PDM signal out of the chip. Nevertheless, this F2D is not designed for the dynamic range of the FDR closed-loop oscillator, and thus using it would limit the maximum measured SNDR.

There is no need for a external bias generator, as the chip has a bandgap reference to generate all the reference currents an voltages. The chip also contains two LDOs, one for the digital circuitry and the other for the analog. They can be activated and deactivated. The test PCB board is introduced in a metal box that serves as a Faraday cage during the measurements.

5.5.5 Measurements

Figure 5.24 shows the measured A-weighted dynamic range of the FDR closed-loop (in blue) and the open-loop oscillator (in green). The open loop oscillator is the same RO used in the FDR closed-loop, but placed in open loop without FDR, operational amplifier, bias current source and the input resistor. The measures are provided in differential, from data of both channels of the pseudo-differential topology and for a 20kHz bandwidth. The dynamic range shows that the FDR closed-loop topology improves the peak SNDR in 14dB over the open loop. The measured k_d of the FDR closed-loop and the open loop are 1.74 and 3.1 respectively. The rest oscillation frequency of both oscillators is the same and equal

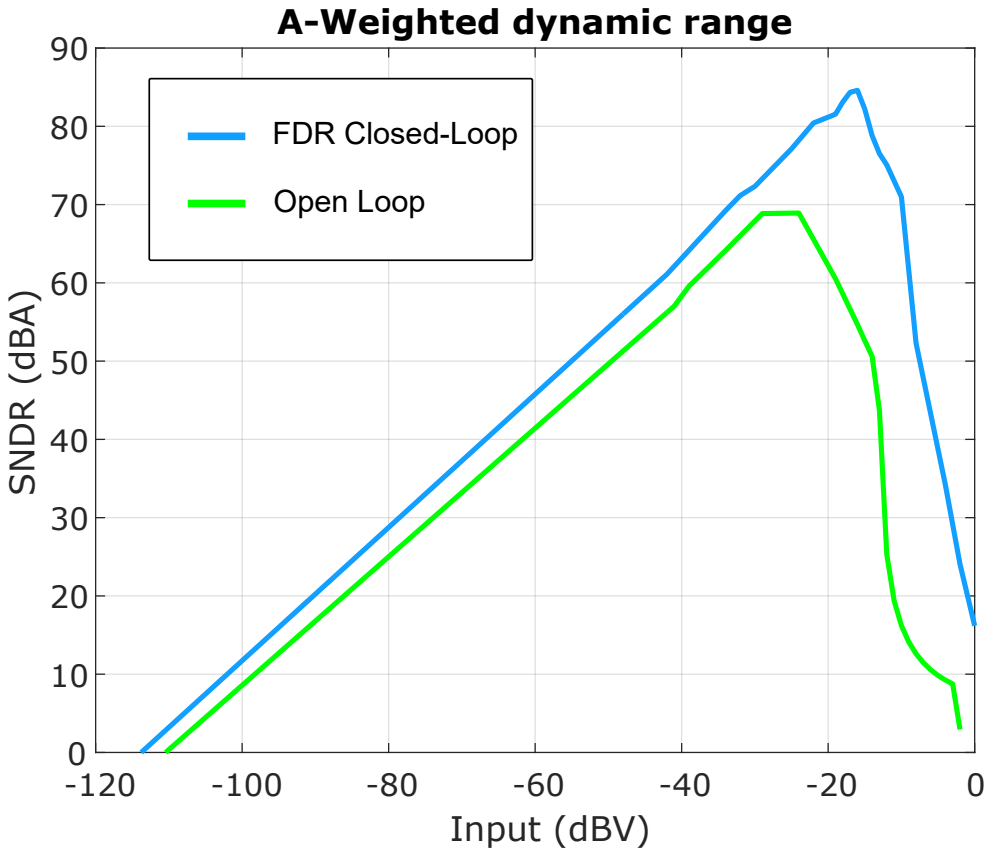

FIGURE 5.24: Dynamic range of FDR closed-loop (blue) and open-loop (green).

to 50MHz. Figure 5.25 shows the FFT of the FDR closed-loop at the $SNDR_{peak}$ (non A-weighted in the top, A-weighted in the bottom). The SFDR of the FDR closed-loop is 93 dB.

The reader might have already noticed that despite having higher k_d the open loop oscillator shows a worse SNR (in the noise dominated region of the DR) than the FDR closed-loop. As it has already been mentioned, the feedback loop attenuates both the RO and opamp noise. Nevertheless, even with attenuation, the opamp is an additional noise source, that dominates the noise according to simulations. And it is important not to forget, that the noises from the FDR and the current source are not attenuated, with the current source being of special concern as it is the second largest contributor to noise according to simulations.

To check if despite the added noise sources, the noise of the FDR closed-loop is lower than the open loop and confirm that the DR is correct, idle channel measures have been taken. These measures have been taken using the test fixture shown in Fig. 5.26 for the FDR closed-loop. For the open loop the short between both channels of the chip has been placed just before the connection to the chip input pins as the input resistor is not present.

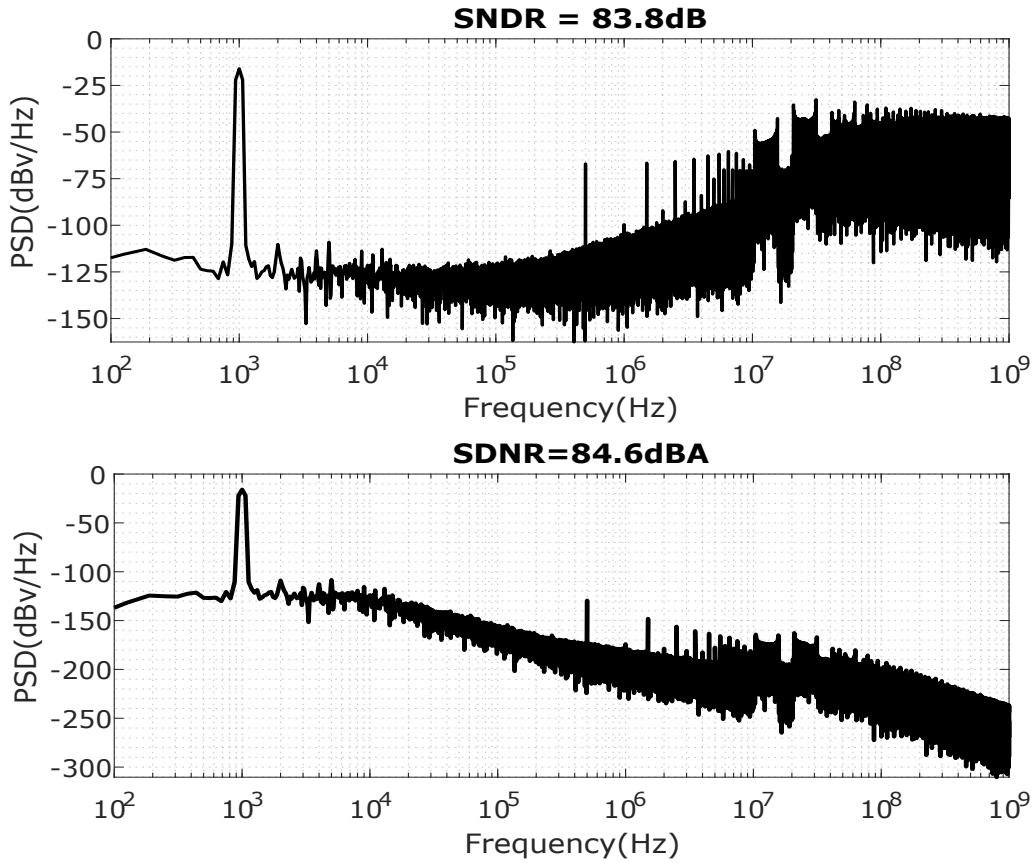

FIGURE 5.25: Non A-Weighted PSD (top) and A-Weighted PSD (bottom) of the FDR closed-loop oscillator.

The FFT of the idle channel measurements are shown in Fig. 5.27 a) and b) for the open-loop and FDR closed-loop respectively. Looking at the spectrum of the open loop (Fig. 5.27 a)) the flicker noise is clearly visible with the noise corner at about 40kHz. Fig. 5.27 b) shows that the noise spectrum of the FDR closed-loop is flat down to 100 Hz frequencies. The integrated noise of the FDR closed-loop is -137 dB while the integrated noise of the open loop is -121 dB. Despite the added noise sources we can find an improvement in the noise of 16 dB in the FDR closed-loop configuration.

Only the analog power consumption of the chip has been measured, as the digital circuitry is not used as explained before. It is important to recall that the FDR closed-loop is to the matter of sampling equal than an open loop RO, so any of the F2D converters used in open-loop RO-ADCs can be used, providing it has enough dynamic range to not overshadow the dynamic range of the RO. Going back to the power measurements, the analog supply voltage used in the measurements is $1.65V$. With this supply the analog current consumption is $360\mu A$

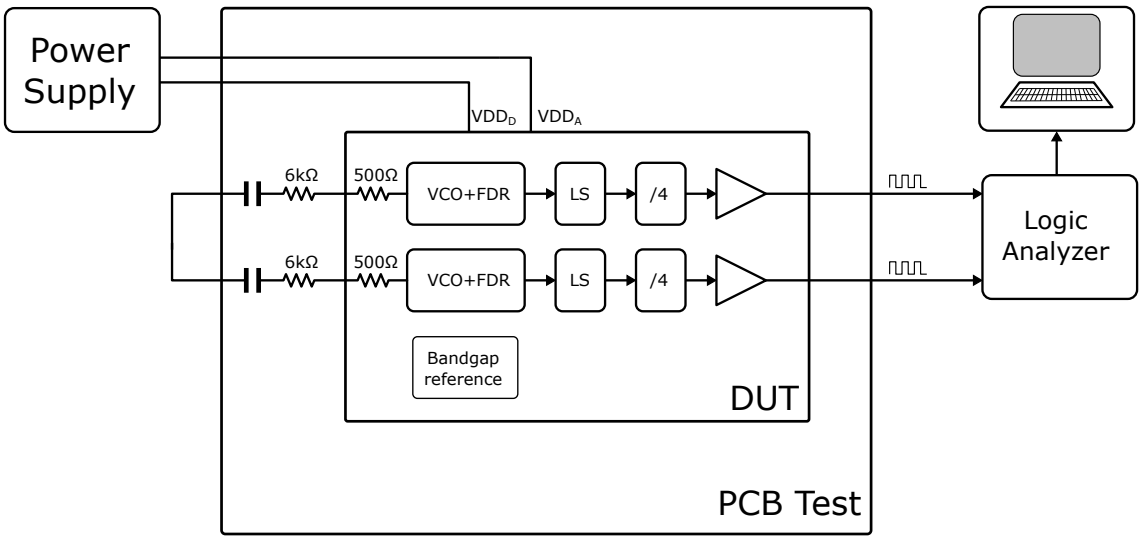

FIGURE 5.26: Idle noise test for chip DOC2

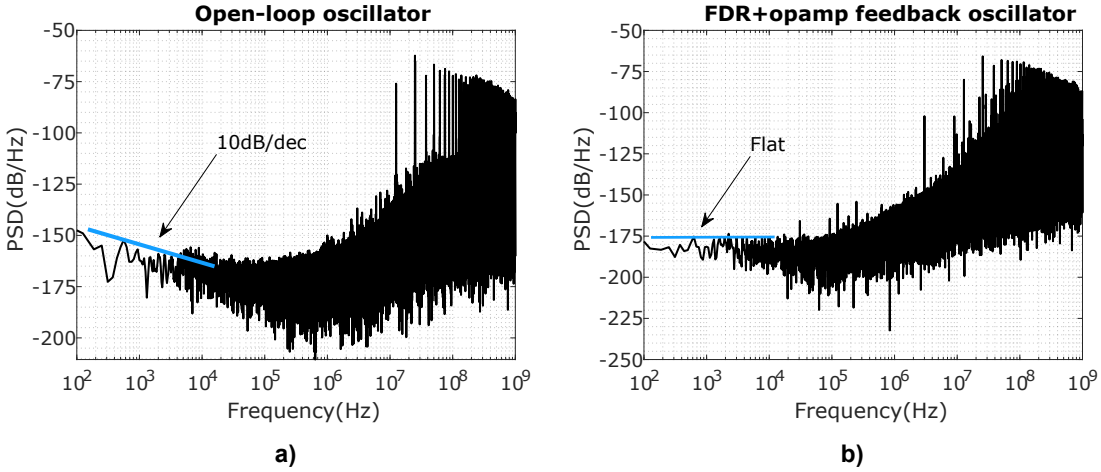

FIGURE 5.27: Idle channel output power spectra for a) open-loop oscillator b) FDR + opamp feedback oscillator.

for both the P and N channel. The power consumption is $600\mu W$. This result should be compared with the DOC1 (Chapter 4) power consumption. With regards to that chip, the power consumption is increased in a 65% while the peak SNDR is increased in 4dB. Now, the oscillator has only 11 taps, instead of the 43 taps of DOC1, which reduces the digital complexity and power. Nevertheless, it is important to bear in mind that while DOC1 is an optimized open-loop VCO-ADC, DOC2 is just a concept proof, and thus has not been optimized to the same level. The Schereier FoM for the chip is 160 dB, accounting only for analog power consumption.

Finally, as described before the chip has the possibility to be measured in single ended (only one channel while the other is off). The measurements done in

single ended are not be presented here in full, as the single ended SNR is degraded from the differential in more than the expected 3dB. This is due to a common mode noise coupled to the oscillators, that is suppressed in the differential measurements but not in the single ended ones.The origin of this noise is not completely understood. It could come from the rest of the chip circuitry (although all the unused circuitry has bee turn off or clock gated when possible), or from the test setup.

That being said it is interesting to provide the SFDR of the single ended FDR closed-loop configuration. The measured SFDR is 78 dB while the analog current is $181\mu A$. The power consumption in single ended is then $300\mu A$.

Chapter 6

Feedback linearization with direct FDR - Ring Oscillator coupling

In the previous chapter a linearization technique for ring oscillators has been discussed. This technique made use of a feedback loop that includes, aside from the oscillator, an operational amplifier and an FDR array. Despite of the fact that this technique shows good results regardless of the characteristics of the oscillator, a lot of power budget has to be allocated in the operational amplifier to fulfill noise requirements. In this chapter an alternative circuit to linearize CCO is presented. The basic idea of this technique is similar to the one presented in the previous chapter, but eliminating the operational amplifier, and seizing the CCO gain, k_{CCO}, to implement the feedback loop. As the achievable gain of the CCO is much lower that the gain of an operational amplifier plus CCO (or VCO), the effectiveness of the linearization is more limited. Nevertheless, this allows not only to eliminate the power consumption of the operational amplifier, but also to share the bias current between the FDR and the CCO, reducing power even more.The overall area of the structure is also reduced. This circuit reduces the signal swing in the oscillator, easing the implementation of the converter at lower supply voltages.

6.1 VCO linearization with FDR + CCO

Figure 6.1 shows the block diagram of the proposed linearized VCO-ADC. The structure is composed of a transconductor (GM), and a linearized CCO. The linearized CCO is made by an inverter-based current-controlled ring oscillator, RO, and a frequency-dependant resistor (FDR). Again, the FDR is just an inverter loaded by a capacitor C_F. A filtering capacitor C_X is required to attenuate the voltage ripple produced by the FDR switching in the VCO. To produce a digital sampled data, the VCO outputs are digitized by a frequency to digital converter (F2D).

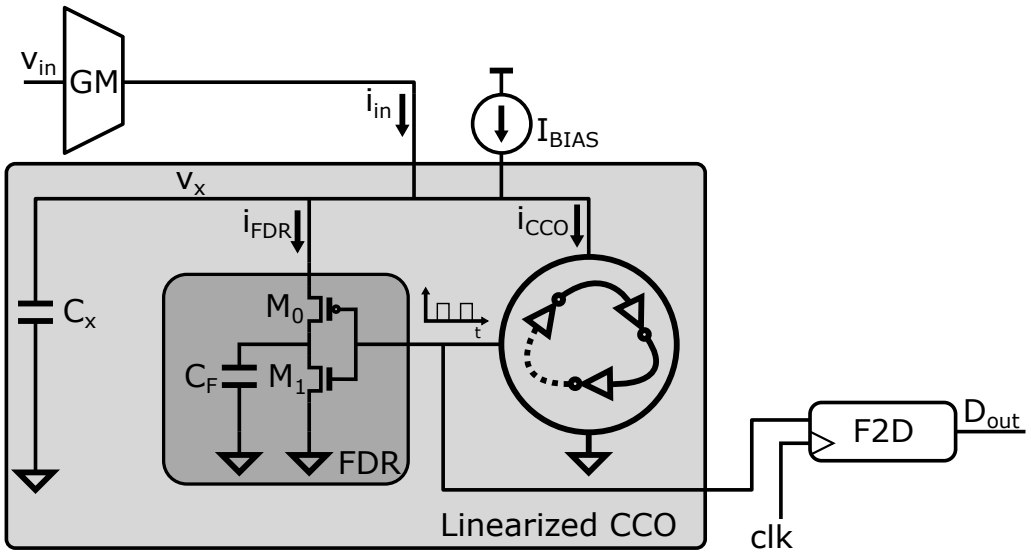

FIGURE 6.1: Block diagram of the proposed linearized VCO.

6.1.1 CCO linearization by a frequency dependent resistor

In Fig. 6.1 we can assume that the switched capacitor equivalent resistor is again given by (5.3). Same as happens with the virtual ground node in Chapter 5, we can assume that if the CCO has a large gain k_{CCO}, the voltage in V_X, is nearly constant. To prove it intuitively, we assume that when the input current i_{in} increases, the CCO frequency f_{out} also increases. The output signal of the CCO then controls the charge and discharge of C_F in the FDR. The average resistance of the FDR inversely depends with the switching frequency (see 5.3) and therefore an increased i_{FDR} will be subtracted from i_{in}. This way, a negative feedback loop is created that stabilizes voltage V_X due to the opposed variations of i_{FDR} and i_{CCO}:

$$i_{CCO} = I_{BIAS} + i_{in} - i_{FDR} \tag{6.1}$$

The overall gain of the proposed structure is given by:

$$\frac{\Delta f}{i_{in}} = \frac{k_{CCO}}{1 + \beta \cdot k_{CCO}}, \beta = V_{X_{DC}} \cdot C_F \tag{6.2}$$

Where $V_{X_{DC}}$ is the DC component of V_X. Observing (6.2), it can be seen that if the product $V_{X_{DC}} \cdot C_F \cdot k_{CCO}$, or loop gain, is much larger than one, the gain of the linearized CCO is independent of k_{CCO}. The best way to fulfill the aforementioned condition is to increase the value of k_{CCO}, but this can be a challenging task. As other options we can raise the bias voltage $V_{X_{DC}}$ or the FDR capacitor C_F. On one hand, increasing $V_{X_{DC}}$ will directly increase the current consumption of the FDR and the CCO at the same time. Furthermore, as the k_{CCO} is maximized for a certain rest frequency when the oscillator is biased in weak inversion, increasing $V_{X_{DC}}$ will reduce the gain of the oscillator, making the loop gain smaller. On

the other hand, increasing the value of capacitor C_F, will only increase the power consumption of the FDR without reducing the k_{CCO}. Nevertheless, a bigger C_F will increase the ripple in node V_X, caused by the switched current drawn by the FDR. The ripple will happen at the oscillator frequency degrading the SNR. To attenuate the ripple we will require a large capacitor C_X. A better alternative is to connect an independent FDR to each tap of the ring oscillator, using proportionally smaller capacitors adding up to a same total capacitance. This way, the ripple in V_X happens at the higher effective frequency of the oscillator [27] reducing SNR degradation.

The rest frequency of the oscillator is given by (6.3):

$$f_0 = \frac{I_{BIAS}}{C_F \cdot V_{X_{DC}}} - \frac{1}{C_F \cdot R_{CCO}} \tag{6.3}$$

where R_{CCO} is the dynamic resistor seen from the input of the oscillator to ground. Finally, (6.4) gives the gain k_{VCO}, including the input transconductor. Given that the voltage swing in V_X is reduced by the effect of the feedback loop, it can be assumed that node V_X approximately behaves as a virtual ground. This makes possible to use a simple resistor as the GM or to fit a source degenerated GM with the benefit of a reduced output swing.

$$k_{VCO} = GM \cdot (\Delta f / i_{in})(Hz/V) \tag{6.4}$$

6.2 Linearity improvement and modeling

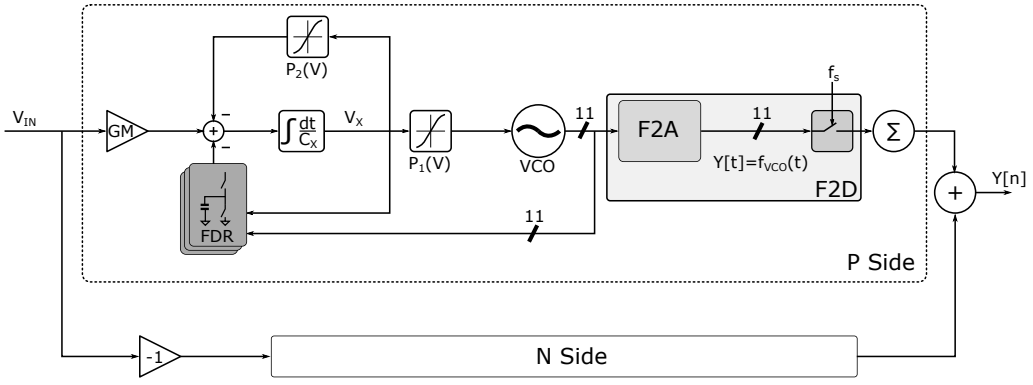

FIGURE 6.2: Diagram of the behavioural model of the FDR feedback structure.

In order to evaluate the distortion correction of the proposed technique, a behavioral model of Fig. 6.1 has been simulated. This model is shown in Fig. 6.2, where the CCO is implemented as an ideal voltage-controlled oscillator and two polynomials, $P_1(V)$ and $P_2(V)$. Polynomial $P_1(V)$ represents the non-linear tuning curve of the actual CCO. Polynomial $P_2(V)$ represents the dynamic resistance

of the CCO, R_{CCO}. Thus $P_2(V)$ converts the input voltage into a current that is then subtracted from node V_X. The integrator represents the integrating function of capacitor C_X and provides voltage V_X. The block FDR is a behavioral model of the FDR (see Fig. 5.5). This block is driven by the oscillator frequency and voltage V_X. The output is i_{FDR} as given by (6.1). Gain GM is the input voltage-to-current conversion factor. The model is implemented in a pseudo-differential configuration [27], therefore, even harmonics are compensated, although single ended results are also shown.

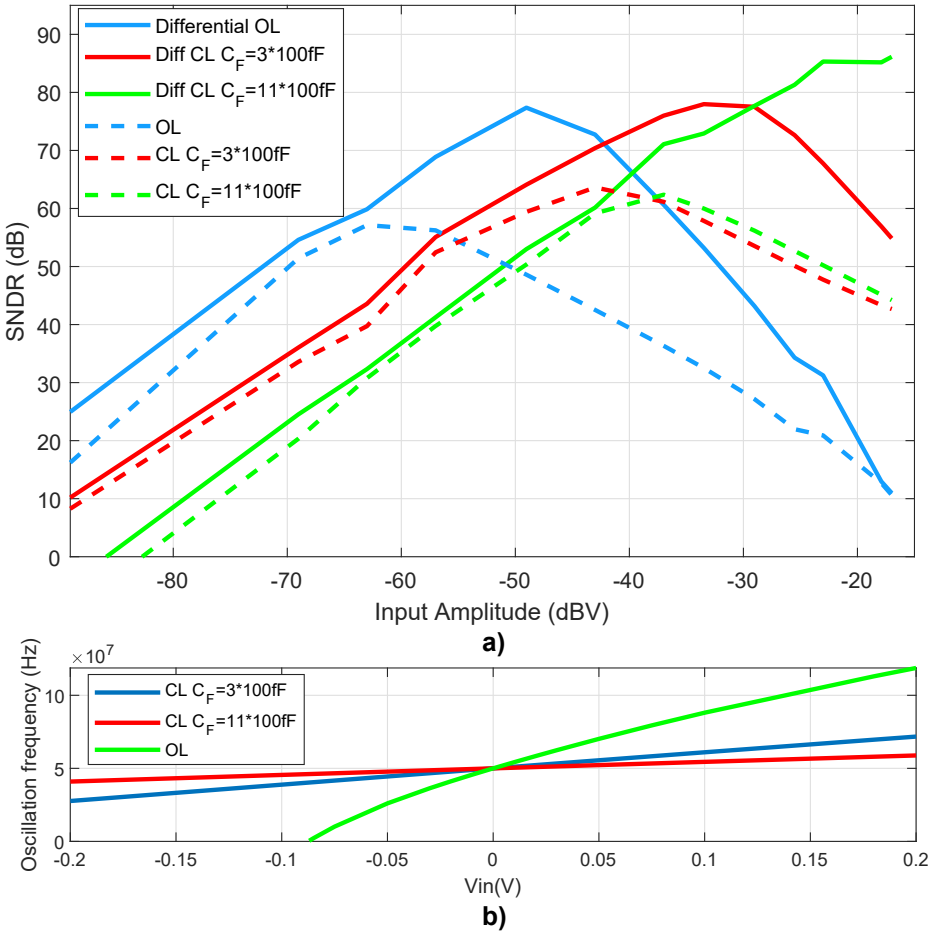

FIGURE 6.3: Results of behavioural simulations a) Dynamic ranges for different configurations of the closed-loop VCO compared with the conventional open-loop VCO. b) Tunning curve of the different configurations.

Figure 6.3(a) shows the dynamic range obtained for several configurations using the aforementioned behavioral model. In this simulation, the VCO has 11 taps. At the rest frequency $f_0 = 50MHz$, the VCO has a gain $k_{VCO} = 575MHz/V$

and a resistance $R_{CCO} = 15k\Omega$. The sampling frequency is 200MHz to simplify the F2D converter. Dotted lines show the results for single ended configurations whereas solid lines show the results for a pseudo-differential architecture. As shown in Fig. 6.3(a) the proposed linearization technique improves the $SNDR_{peak}$. It is worth noting that for a single ended configuration, where 2^{nd} order harmonics dominate, increasing the number of FDRs connected to the oscillator, and thus the total FDR capacitance, does not improve the peak SNDR. This is different from the pseudo-differential topology (dominated by 3^{nd} order harmonics distortion), where increasing the FDR total capacitance by increasing the number of connected FDR from 3 to 11 increases the peak SNDR by 9 dB. The reason for this is as follows. As expressed in (6.2), the size of capacitor C_F impacts the effectiveness of the linearization. For the single ended case the connection of 3 FDRs with a total capacitance of 300 fF reduces the 2^{nd} order harmonic, but not the 3^{rd} harmonic, because the loop gain is not large enough. The peak SNDR for this feedback is not improved over the open-loop because pseudo-differential configuration already cancels 2^{nd} order harmonics. Connecting more FDRs (11 in the example) increases the gain loop and thus the effectiveness of the linearization, compensating also 3^{rd} harmonics, which increases the peak SNDR over the open-loop pseudo-differential architecture. The same result would have been obtained by increasing the gain of the oscillator, which is another way to increase the loop gain.

Figure 6.3(b) shows the tuning curve of the oscillator in open-loop and with feedback for the two aforementioned FDRs configurations. From this plot it can be seen that the proposed topology improves the linearity of the CCO. The results for k_{VCO} for each simulated configuration are 430.16 MHz/V for the open-loop CCO, 111.06 MHz/V for the closed-loop CCO with 3 FDRs and 44.695 MHz/V for the closed-loop with 11 FDRs.

6.3 Frequency response of the FDR feedback oscillator

Figure 6.4 shows the linearized model of the FDR feedback oscillator. As mentioned in Chapter 5 this is a small-signal linear approximation of a LPTV system. From this model, the frequency response of the proposed circuit driven by a GM is given by the following transfer function:

$$\frac{fout}{V_{in}}(s) = \frac{GM \cdot k_{VCO}}{sC_X + C_F \cdot V_{X_{DC}} \cdot k_{VCO} + \frac{1}{R_X}} \tag{6.5}$$

Where R_X is the parallel resistance of the FDR and the ring oscillator as given by:

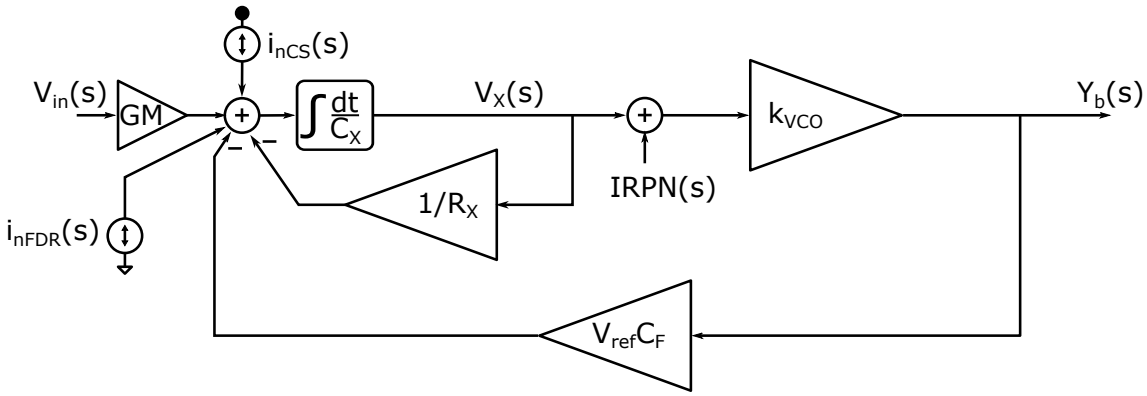

FIGURE 6.4: Linearized small signal model with noise sources of the FDR feedback oscillator.

$$R_X = \frac{1}{C_F \cdot f_0} // R_{CCO} \tag{6.6}$$

For typical values of k_{CCO}, C_F, $V_{X_{DC}}$, R_{CCO} and C_X the cut-off frequency of the system is in the order of hundreds of kHz in the targeted audio application. The frequency response when a resistor R_{in} is used as a GM, is given by the following expression:

$$\frac{fout}{V_{in}}(s) = \frac{1}{R_{in}} \frac{k_{VCO}}{sC_X + C_F \cdot V_{X_{DC}} \cdot k_{VCO} + \frac{R_X + R_{in}}{R_{in} \cdot R_X}} \tag{6.7}$$

6.4 Noise analysis of the FDR feedback oscillator

Figure 6.4 shows also the noise sources present in the circuit. The noise sources are the input referred phase noise of the oscillator, $IRPN$, the noise from the bias current source I_{nCS} and the noise of the FDR i_{nFDR}. The RO output noise PSD is given by the following equation:

$$S_{NY}(f) = |H_{IRPN}(j2\pi f)|^2 S_{IRPN}(f) \tag{6.8}$$

Where $H(s)$ is the transfer function from the input of the RO to the output and is given by:

$$H_{IRPN}(s) = k_{VCO} \frac{sC_X + \frac{1}{R_X}}{sC_X + k_{VCO} V_{X_{DC}} C_F + \frac{1}{R_X}} \tag{6.9}$$

Equation 6.9 must compared with (5.24). This is done in Fig. 6.5, where a R_{CCO} of $67k_\omega$ and the values of Table 5.1 have been used. The noise attenuation is much lower in the case of the direct connection between the FDR and the CCO,

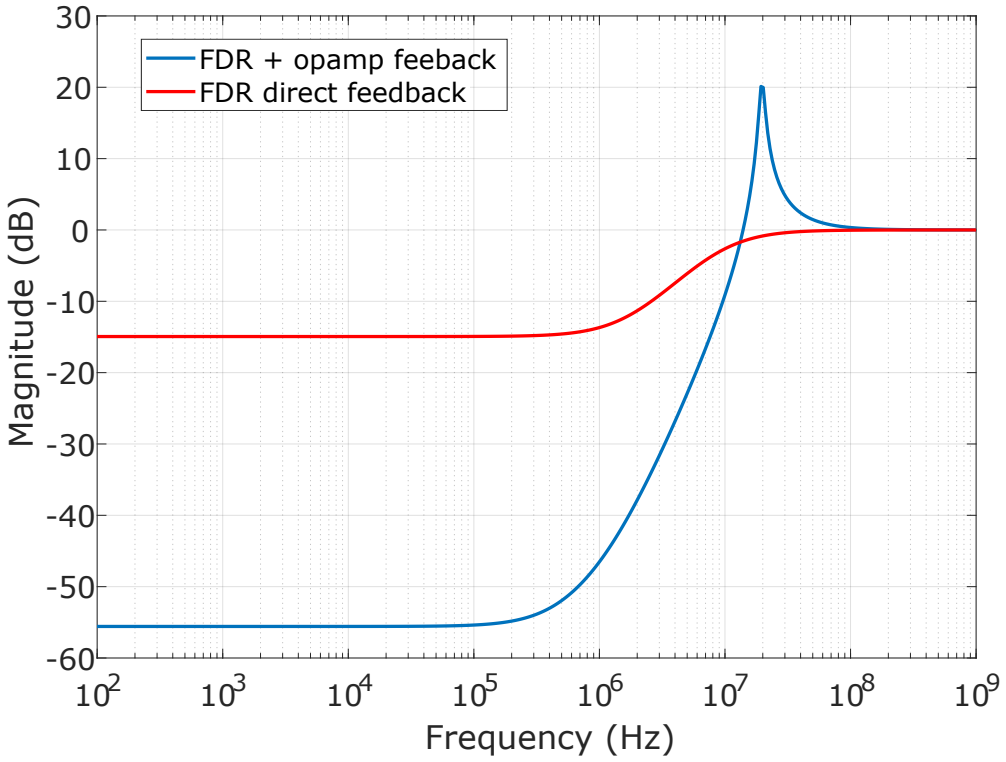

FIGURE 6.5: Comparison of the phase noise transfer functions of the FDR + opamp feedback oscillator and the direct FDR feedback oscillator.

than in the case were the operational amplifier is present. Nevertheless, both the power consumption and noise of the operational amplifier are not present in this circuit. It is specially important to remember that the noise from the operational amplifier is multiplied by k_{VCO} as shown by (5.30). This means that the noise at the output of the oscillator in the direct FDR feedback configuration is not as bad compared with the FDR + opamp feedback as Fig. 6.5 suggest.

The noise from the bias current source and from the FDR see the following transfer function:

$$H_{nFDR}(s) = H_{nCS}(s) = \frac{k_{VCO}}{sC_X + C_F \cdot V_{X_{DC}} \cdot k_{VCO} + \frac{1}{R_X}} \tag{6.10}$$

Which is the same than (6.5) without the GM.

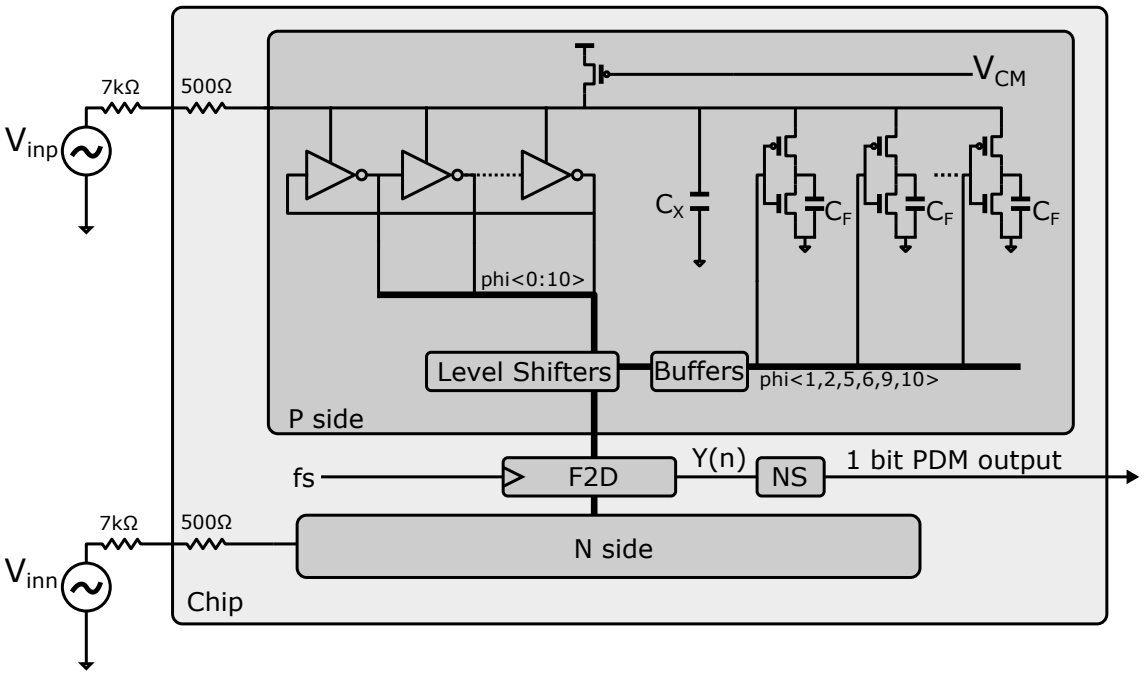

FIGURE 6.6: Schematic of the 130nm CMOS test chip.

6.5 Experimental validation: Chip DOG1

6.5.1 Chip architecture

We have designed and measured a 130nm CMOS chip prototype to test the linearization concept. This chip is intended for an audio application similar to [59], [60], [86] and therefore we evaluate noise measurements applying the A-weighting curve. Unlike the DOC2 chip from the previous chapter, this includes the F2D converter, and it is a full microphone chip. The simplified chip schematic is shown in Fig. 6.6, which uses a pseudo-differential topology with two identical signal paths. Each signal path is composed of a CCO, a FDR array and a biasing current mirror that generates V_{CM} from a bandgap reference. The outputs of the oscillator are connected to level-shifters to reconstruct full logic values. A 6 pF capacitor is used as C_X to filter the FDR's ripple at the CCO input. The voltage to current conversion is performed by an input resistor. This input resistor is partially placed off-chip to trim the transconductance GM and has a nominal value of $7k\Omega$. A 500 ohms resistor is placed on-chip, to limit the current. The CCO is implemented with 11 single-ended inverters oscillating at 50MHz at rest. The value of k_{VCO} is 155 MHz/V. Considering thermal and flicker noises, the inverters are sized $4\mu m/600nm$ for PMOS devices and $2\mu m/600nm$ for NMOS devices. We have chosen six level shifter outputs to drive the corresponding FDR elements in the feedback loop. This connection is made through a buffer implemented with an inverter. This buffer can be enabled or disabled to activate or

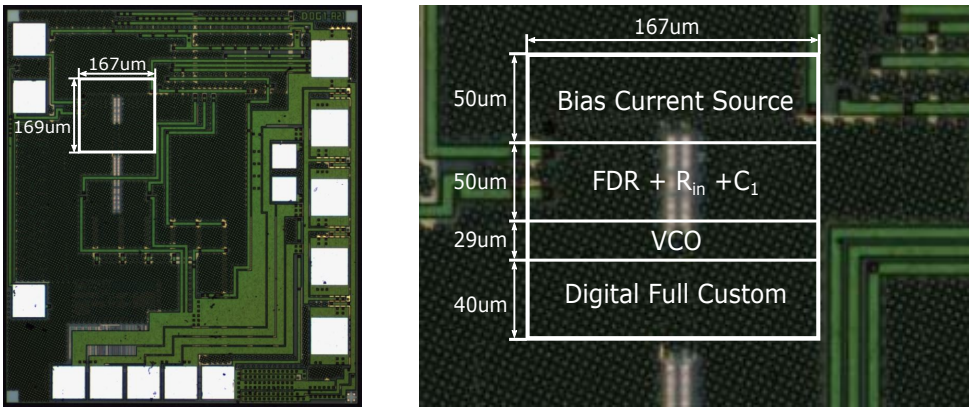

FIGURE 6.7: Micrograph of the 130nm CMOS test chip.

deactivate the feedback loop. This way we can measure both the oscillator with feedback and without feedback and compare the results. The FDR transistors are sized $3\mu m/120nm$ for PMOS and $1.5\mu m/120nm$ for NMOS. Capacitor C_F for each FDR has a value $C_F = 162fF$ summing up a total capacitance of $972fF$ for all taps. The bias voltage in V_X is 1V. The total resistance of the 6 FDRs from node V_X to ground is thus $19k\Omega$ including transistor leakage at the given bias voltage and rest frequency. The supply voltage is 1.5V for the analog domain and 1V for the digital domain.

The reconstructed output of each tap of the oscillator is digitized with a frequency-to-digital converter (F2D) and post-processed by a digital noise shaper (NS) operating at a sampling rate of 3.072MHz. The noise shaper is included for compatibility with standard single-bit PDM MEMS microphone outputs readable by audio test equipment, and is designed to avoid limiting the ADC SNDR[87]. The digital section of the chip uses the same circuitry described in [59]. Therefore, it will not be discussed here again.

6.5.2 Measurements and state of the art comparison

Figure 6.7 shows the micrograph of the 130nm CMOS chip, which contains the ADC and other biasing and testing functions. The area occupied by the ADC is of 0.028 mm^2. The VCO is AC driven by two external decoupling capacitors, although it can also be driven by DC signals with proper DC biasing. The output noise-shaped single-bit stream is captured using an audio analyzer.

Figure 6.8 shows several measurements of the dynamic range of the chip. SNDR values are given in dBA (A-Weighted) and measured in a 20kHz bandwidth. A standard input tone of 1kHz has been used for all measurements. Three different configurations have been measured, (a) closed-loop with an input resistor of 7.5 $k\Omega$ (500 Ω on chip, 7 $k\Omega$ in the PCB board), (b) open-loop with an input resistor of 7.5 $k\Omega$, and (c) open-loop with the on-chip input resistance of 500 Ω.

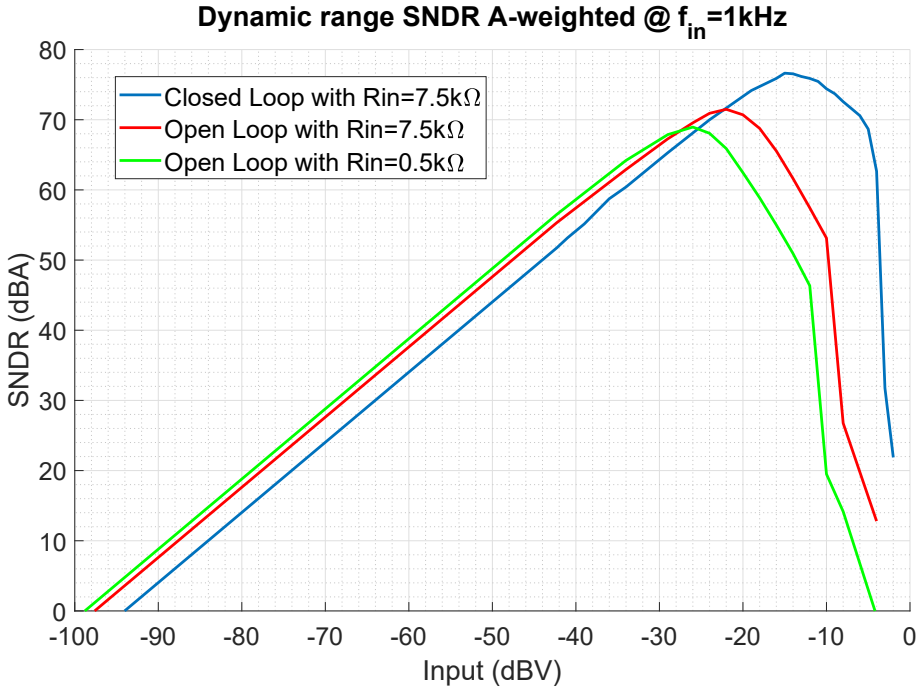

FIGURE 6.8: Comparison of the measured dynamic ranges.

The blue line in Fig. 6.8 shows the DR for the closed-loop configuration (a), which corresponds to full performance operation of the ADC. In this mode, the behavior of the ADC is different form other ADCs because the $SNDR_{peak}$ is achieved at a low amplitude and remains nearly constant in a broad input range. This proves the dynamic range enhancement provided by the proposed technique. From v_{in}=-24dBV to v_{in}=-6dBV, the SNDR remains above 70dBA, with a maximum variation of 6.7dBA achieved at v_{in}=-15dBV, which corresponds to the $SNDR_{peak}$=76.64dBA. To further prove the distortion improvement of the feedback loop, we are going to compare the dynamic range of each configuration assuming as full scale point the amplitude where 60dBA of SNDR is reach due to distortion. For measurement (a), SNDR=60dBA is obtained at -4 dBV, which corresponds to a DR=90dB.

The DR of the open-loop topology with a 7.5 $k\Omega$ input resistor (b) is plotted with a red line in Fig. 6.8. The peak SNDR for this configuration is 71dBA at an input level of v_{in}=-23dBV. The SNDR drops below 60dBA at v_{in}=-13.2dBV which results in a DR=84.1dB. The DR improvement of configuration (a) over (b) is of 5.9dB and the improvement of the peak SNDR is of 5.6dBA. This measurement does not fully show the potential of the linearization, as the series resistor with the VCO provides some distortion cancellation (see Section 4.3.1). For this reason, we have measured the VCO in open loop with only the on-chip 500Ω resistor.

The results of the open-loop topology (c) are shown in green in Fig. 6.8. At $v_{in} = -26dBV$, the peak $SNDR_{peak}$=69dBA is reach. The value of the DR using

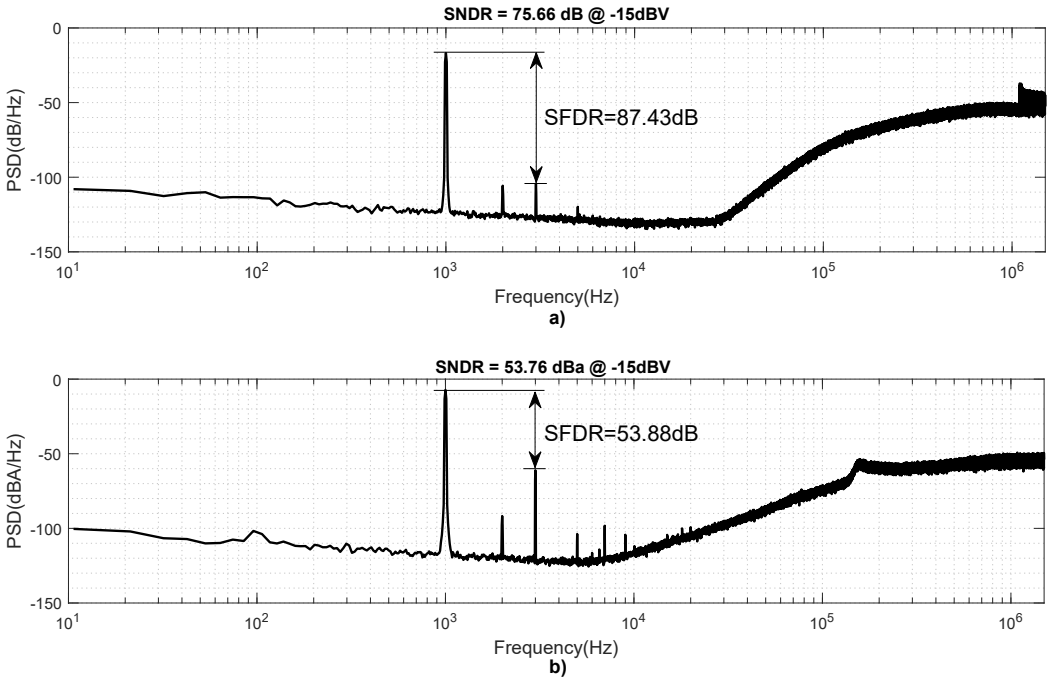

FIGURE 6.9: PSD a) Closed-Loop $V_{in} = -15dBV$ $R_{in} = 7.5k$. b) Open-Loop $V_{in} = -15dBV$ $R_{in} = 0k$.

TABLE 6.1: Comparison with other works

Specification	This work	[88]	[89]	[57]	[16]
Technology	130nm	180nm	65nm	65nm	130nm
BW [MHz]	0.02	0.5	1	20	0.1
Power [mw]	0.48	2.9	0.36	8.2	12.6
Area [mm^2]	0.03	0.03	0.002	0.6	0.08
SNDR [dB]	75.7	71	50.1	68	71.8
FOM [dB] **(SNDR peak)**	152.8	153	143.9	162	140.8

the 60dBA SNDR criteria is DR=79.8 dBV. Thus, the improvement of the closed-loop topology (a) over (c) is of 10.2dB for the DR and 7.64 dBA for the peak SNDR.

The PSD of the single-bit PDM output data is shown in Fig.6.9 for a closed-loop configuration (a) and an open-loop configuration (c) at an input amplitude v_{in}=-15dBv. The noise-shaping profile is more steep than the expected 20dB/decade due to the digital noise-shaper in the output interface. The SFDR for the closed-loop configuration, Fig. 6.9 a), is 87dB, while the SFDR for the open-loop, Fig.6.9 b), is 54dB.

Figure 6.10 shows an idle channel measurement of the oscillator in open-loop a) and with the FDR based feedback b). In b) it can be observed that the noise

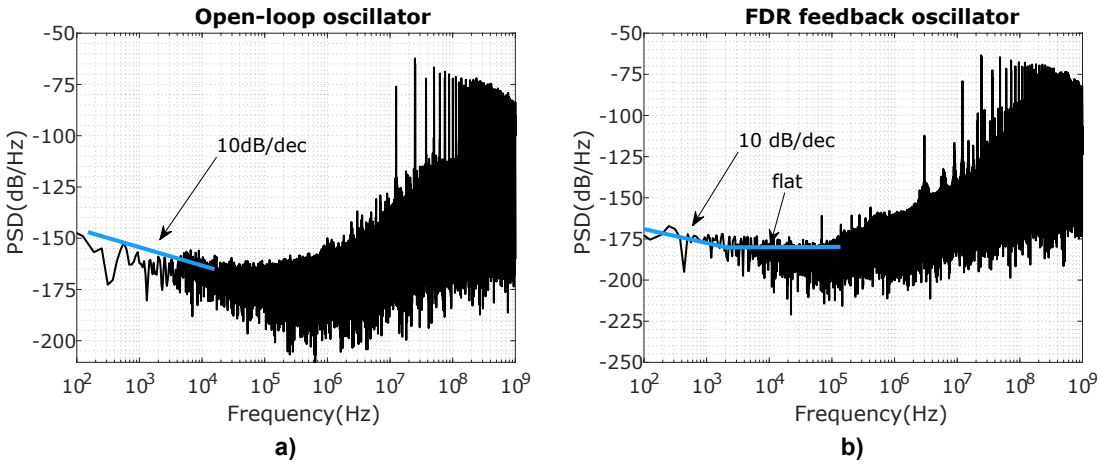

FIGURE 6.10: Idle channel PSD of a) Open-loop. b) FDR feedback architecture.

is attenuated thanks to the feedback, which mitigates the lost of SNR due to the lower gain. Also the flicker corner frequency moves to lower frequencies (approximately 5kHz) compared to the open-loop oscillator.

Total power consumption of the prototype chip is $482\mu W$, with the 53.5% of it spent in the analog front-end and the remaining 46.5% in the digital post-processing. Table 6.1 shows a comparison with other works. Compared to other analog linearization techniques, we can see that our solution shows a better power [88] or peak SNDR [89]. Compared to [57], the complexity of the digital algorithms require a substantial area increase. In [16], a look up table digital linearization techniques result in a less power and area efficient solution. The designed chip can be further improved by higher k_{CCO} oscillators, achievable in smaller CMOS nodes.

6.6 Experimental validation: Mercury 3 chip

We have designed, fabricated and measured a second 55nm CMOS chip prototype to test the linearization concept. Our purpose is to measure the noise and linearity of the oscillator rather that to implement a VCO-ADC data converter and therefore the chip does not include any frequency-to-digital converter, using external hardware for this task. The simplified chip schematic is shown in figure 6.11, which uses a pseudo-differential topology with two identical signal paths. Each signal path is composed of a CCO, an FDR array and a biasing current mirror. The outputs of the oscillator are conected to level-shifters to reconstruct full logical values. A 6 pF capacitors are used as C_X to filter the FDR's ripple at the CCO input. The voltage to current conversion is performed by an input resistor. This input resistor is partially placed off-chip to trim the transconductance GM and has a nominal value of $5.5k\Omega$. A 500 ohms resistor is placed on-chip, to limit

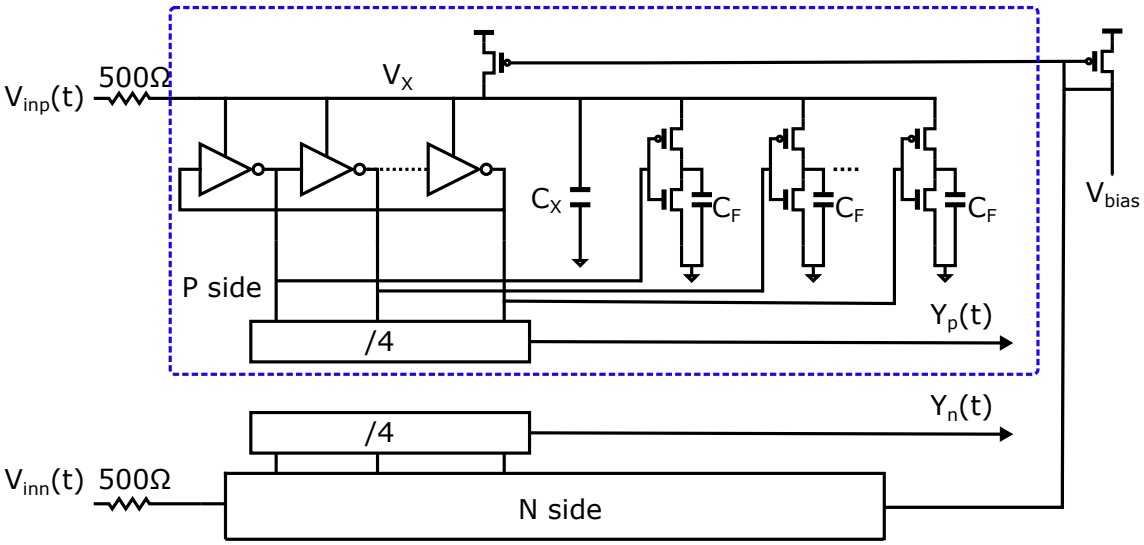

FIGURE 6.11: Schematic of Mercury 3 chip.

the current. The CCO is implemented with 11 single ended inverters oscillating at 50MHz at rest. The value of k_{CCO} is 2.233 MHz/uA. The inverters transistors are sized $20\mu m/280nm$ for PMOS devices and $10\mu m/280nm$ for NMOS devices, based on thermal and flicker noise restrictions. Each tap of the oscillator is connected to a FDR unit. To reduce the capacitive load of the oscillator, transistor sizes in the FDR are down scaled by a factor of 4 to $5\mu m/280nm$ for PMOS and $2.5\mu m/280nm$ for NMOS. Capacitor C_F for each FDR has a value $C_F = 30.82fF$ summing up a total capacitance of $340fF$ for all taps. The bias voltage in V_X is 550mV. The total resistance of the 11 FDRs from node V_X to ground is thus $107k\Omega$ at the given bias voltage and rest frequency. The simulated k_{VCO} of the linearized oscillator is 150 MHz/V giving a normalized gain k_d of 2.7.

6.6.1 Measurements

Figure 6.12 shows the micrograph of the designed and fabricated 55nm CMOS chip. The area occupied by the proposed topology is of 0.013 mm^2. The chip has been tested using the test fixture shown in Fig. 6.13. The VCO is AC driven by two external decoupling capacitors, although it can also be driven by DC signals with proper DC biasing. A single phase out of the 11 VCO outputs is brought out of the chip after dividing the VCO frequency by 4 to avoid excessive noise form the output pads. This single-bit asynchronous oscillation is sampled with a logic analyzer at a frequency of $1Gs/s$ and stored in a memory buffer of $500Ms$. The SQNR due to quantization noise in a bandwidth of 20KHz can then be estimated at 125dB. This way, quantization noise due to the sampling process is negligible compared to the estimated noise due to thermal and flicker sources, which peaks

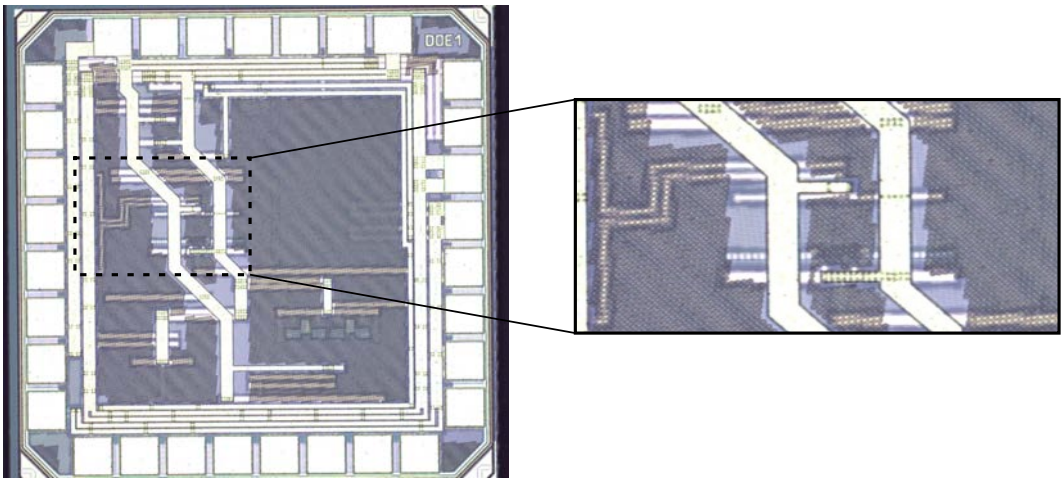

FIGURE 6.12: Micrograph of the Mercury 3 chip.

at 80dB max, and the SNDR estimated for the VCO will be limited by noise and distortion only.

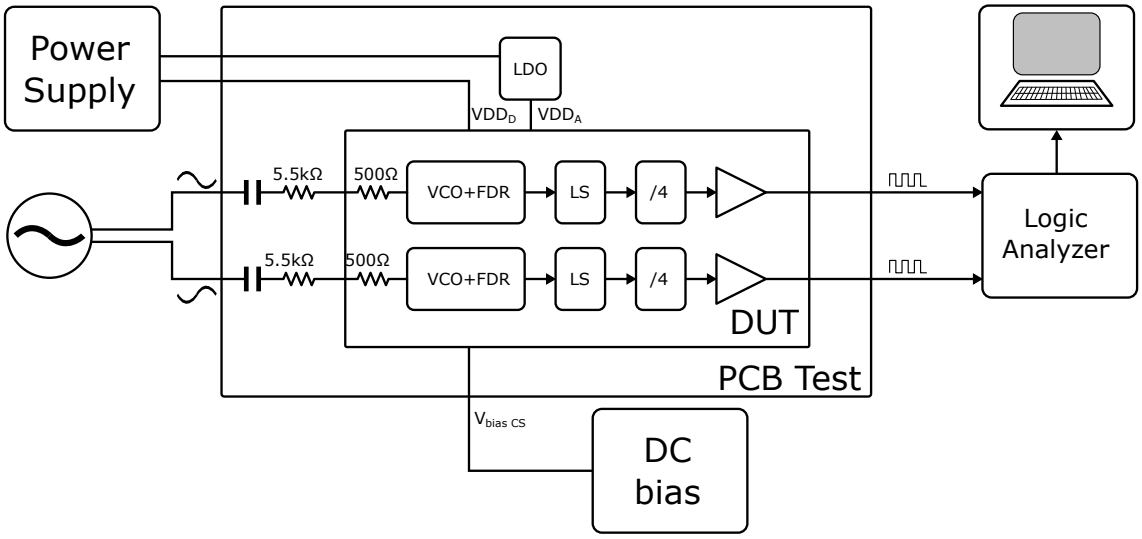

FIGURE 6.13: Mercury 3 chip Test fixture

Figure 6.14 shows a series of simulated and measured dynamic ranges of the proposed chip. SNDR values are given in dBA and measured for a 20kHz bandwidth standard for audio applications. The input tone for the measurements has a 1kHz frequency to properly account for the harmonics within the BW. The blue dash-dotted line shows SNDR of the pseudo-differential system with the oscillator in closed-loop for the different input amplitudes, simulated using a PSS and pnoise analysis. The peak SNDR for this simulation is 80.8 dBA. This result is

compared with the measured DR for the close-loop pseudo-differential configuration shown as a solid blue line. This measurement shows more noise and thus a lower peak SNDR at 78.15 dBA.

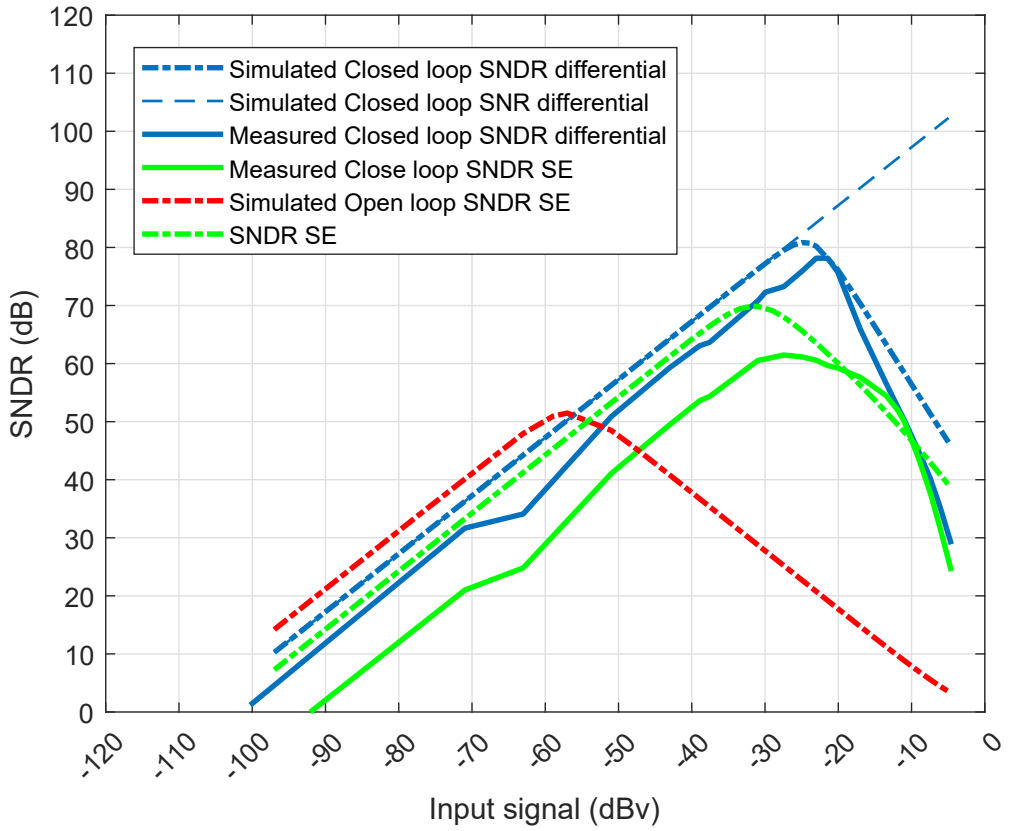

FIGURE 6.14: Comparison of the simulated and measured dynamic ranges.

The single-ended configuration has also been simulated and measured. PSS and pnoise simulation results for the closed-loop single-ended configuration as shown as a green dash-dotted line. Peak SNDR is above 69.8 dBA for this simulation. Measured results for this configuration are shown as a solid green line. This results differ more from simulation than in the pseudo-differential case. Lower SNR and peak SNDR can be observed. The peak SNDR for the measurements is around 61.5 dBA, more than 8 dBA lower than in simulation. The cause of this discrepancy is not fully understood.

Finally, the dash-dotted red line show the PSS and pnoise simulation results for the single-ended oscillator in open-loop, without feedback through the FDR. As the *kd* of the oscillator without feedback is higher, SNR of the open-loop oscillator is better. Nevertheless, the oscillator non-linerity is not compensated, which causes the SNDR to peak at 51.5 dBA. This simulation results can be compared

with the measured DR for the single-ended closed-loop oscillator. Comparison shows that the improvement in the peak SNDR thanks to linearization by the FDR is of 10 dBA.

Figure 6.15 shows the measured a-weighted PSD for the pseudo-differential closed-loop circuit at -23 dBv for a 1khz input signal. It can be seen that no distortion is present. Measured power consumption of the circuit supplied at 1.5 V is 153.0 µW, considering both oscillator phases, level-shifters, frequency dividers and buffer circuitry. The Schereier FoM is 159 dB.

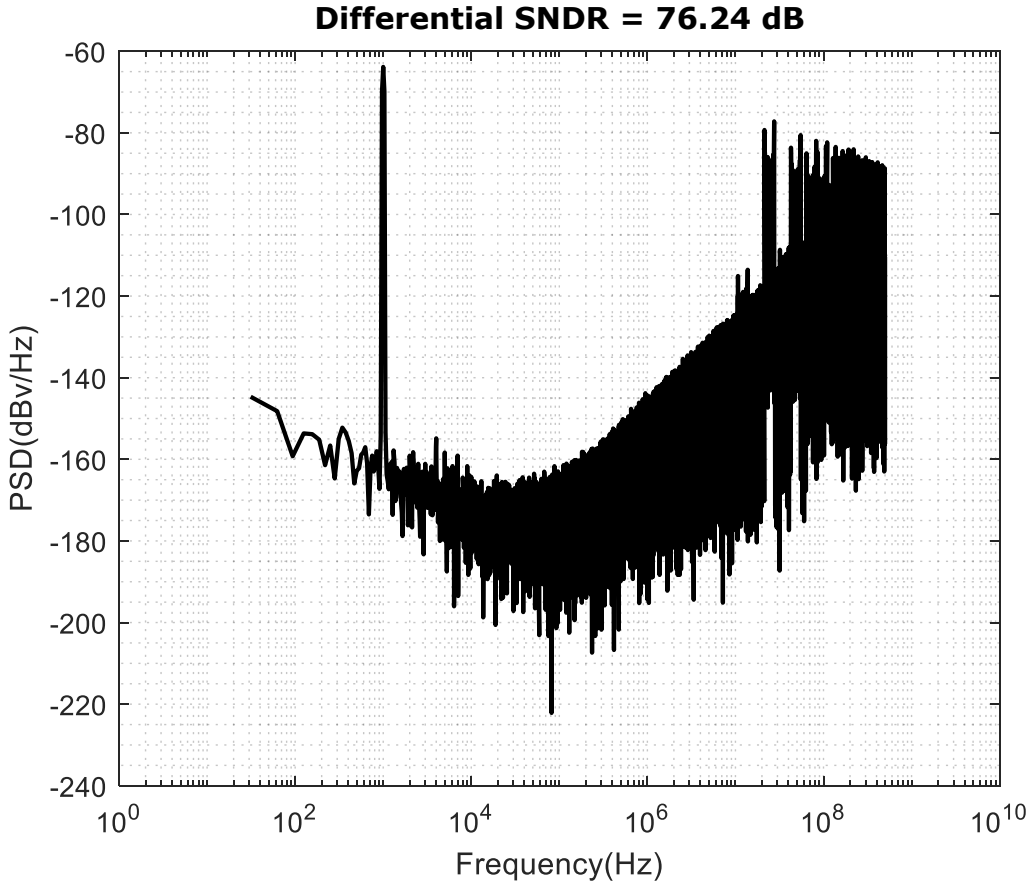

FIGURE 6.15: FFT at peak SNDR of the differential signal, non A-weighted.

Chapter 7

Other applications of FDR circuits

7.1 Direct MEMS

In Chapter 2 the possibility to use a noise-shaping dual slope converter to implement a direct (i.e. without any front end circuit) capacitance-to-digital converter (CDC) was mentioned [21], [22]. Aside from the use of a noise-shaping dual slope converter to implement a CDC the use of VCO based CDCs has been reported [90]. In this Chapter a FDR closed-loop RO based CDC is presented. The idea consist on substituting capacitor C_F in the FDR for a MEMS capacitor. This way a direct measurement of the capacitance can be obtained.

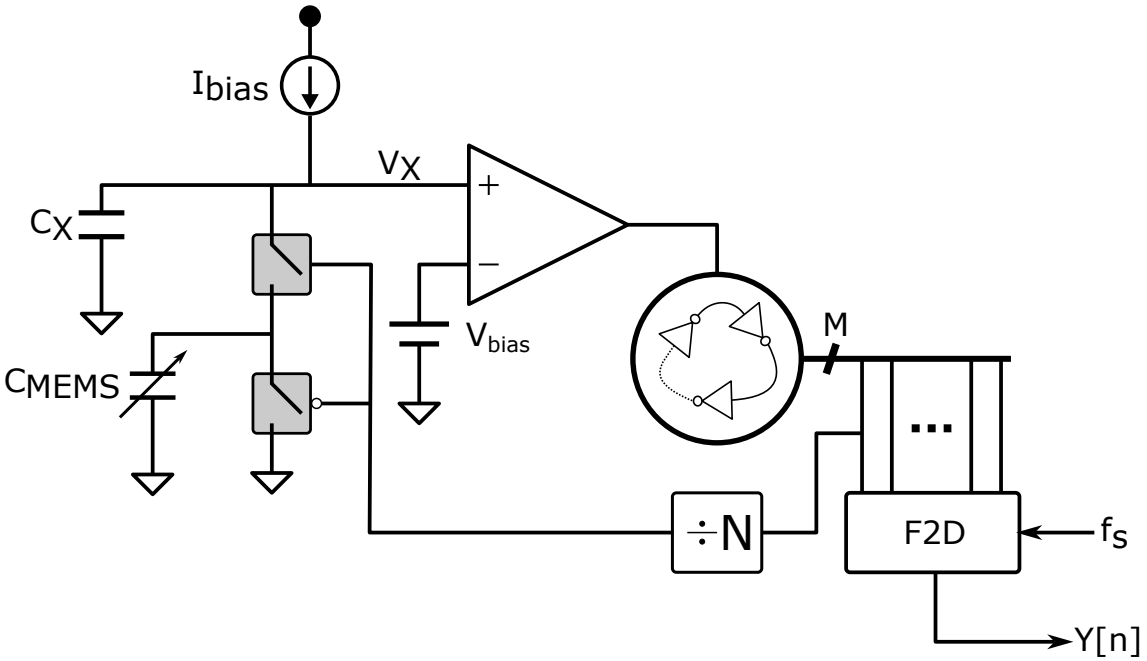

FIGURE 7.1: FDR closed-loop RO based CDC system schematic.

The basic block diagram of the proposed capacitance-to-digital converter is shown in Fig. 7.1. The converter is composed of an M taps voltage controlled oscillator (VCO), an opamp, a current source, a frequency divider and an FDR in

the feedback network. In this circuit the purpose of the FDR is twofold. On the one hand it is used as a means of VCO linearization in a similar way than it has been used before in this dissertation. On the other hand, using MEMS capacitor, C_{MEMS}, as the capacitor in the FDR allows for a direct readout of the MEMS value. Assuming the divider to have a dividing factor equal to one and using either (1.2) or (1.3) , we can analyze the circuit of Fig. 7.1 to get the next expression for the output frequency:

$$f_{\text{osc}} = (d_0 + \Delta d)\frac{I_{bias}}{\epsilon_0 \epsilon_r A \cdot V_{bias}} \tag{7.1}$$

Eq. 7.1 shows that the output frequency varies linearly with the distance between plates of the variable capacitor. This property is very useful because the capacitance in many MEMS capacitve sensors varies with the distance between plates instead of the area. This happens especially in MEMS pressure sensors and MEMS microphones. Fig. 7.1 shows a frequency divider inserted in the feedback loop between the output of the oscillator and the FDR. The divider is added to improve the quantization noise of the circuit without a big increase in power consumption. With the use of the frequency divider, the FDR's switching frequency, f_{M} is related with the VCO's frequency, f_{v}, by the following expression:

$$f_{\text{M}} = \frac{f_v}{N} = (d_0 + \Delta d)\frac{I_{bias}}{\epsilon_0 \epsilon_r A \cdot V_{bias}} \tag{7.2}$$

Where f_{M} is a fraction of f_{v}. The DC and AC components of the VCO's frequency are given by the equation 7.3

$$f_{v_0} + \Delta f_v = d_0 \frac{N \cdot I_{bias}}{\epsilon_0 \epsilon_r A \cdot V_{bias}} + \Delta d \frac{N \cdot I_{bias}}{\epsilon_0 \epsilon_r A \cdot V_{bias}} \tag{7.3}$$

And from equation 7.3, the sensitivity of the VCO to changes in the sensor is given by

$$k_{VCO} = \frac{N \cdot I_{bias}}{\epsilon_0 \epsilon_r A \cdot V_{bias}} \tag{7.4}$$

Equation 7.4 shows that the sensitivity of the VCO is increased by a factor N while keeping the current I_{bias} constant and thus without increasing the power consumption in the FDR. This is an interesting property, because thanks to the feedback, the noise of the oscillator is suppressed. This means that the size of the oscillator delay cells can be made using minimum or near minimum sizes without much noise degradation. Thanks to this making a very fast oscillator with low power is possible without degrading the SNR.

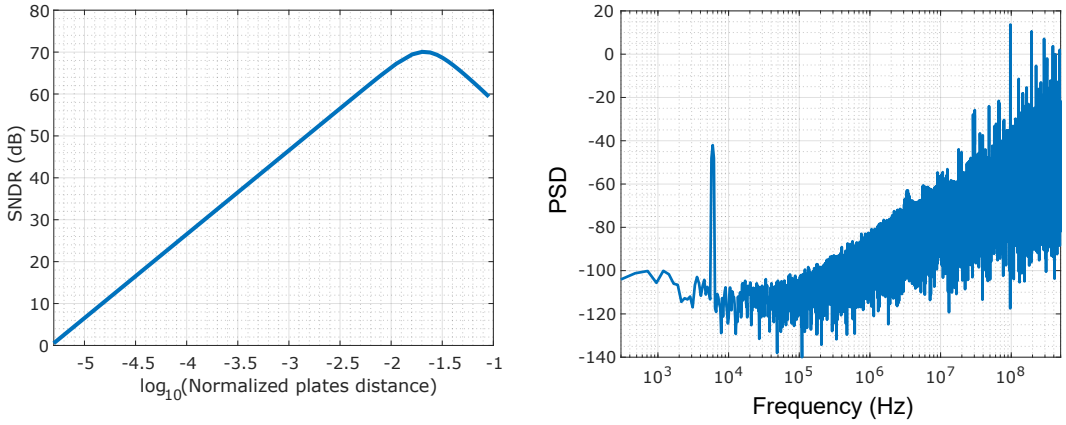

FIGURE 7.2: a) Dynamic range of the FDR closed-loop CDC. b) PSD of the output data of the FDR closed-loop CDC sampled at 2GHz to avoid quantization noise.

Figure 7.2 a) shows the dynamic range obtained with a PPS and PNOISE simulation of the FDR closed-loop CDC. The X-Axis shows the log_{10} of the normalized amplitude distance between the capacitor plates (i.e. divided by the distance at rest) . The rest oscillation frequency for this simulation is 50 MHz with a $k_d = 0.077$. The oscillator and the FDR has been simulated at transistor level, while the amplifier is a single-pole ideal model ($G_{dc} = 60dB$, $f_p = 6kHz$. The bias current source is ideal. The only noise sources considered in the circuit are the VCO and the FDR. Here a limitation of this circuit is evident. The gain of the oscillator is dependent on the sensitivity (in distance between plates) of the MEMS. For the model used in this simulation, this sensitivity is very small. The use of a frequency divider as previously discussed can help to mitigate this problem for quantization noise, but this is not true for circuit noise (specially bias current source noise). So a MEMS capacitor with high sensitivity is necessary to obtain a good SNR.

Figure 7.2 b) shows the PSD obtained from a transient simulation of the same circuit that used for a). Despite the fact that the capacitance varies with the inverse of the distance between plates, no distortion is observed in the PSD. This is because we are changing the value of the capacitor by changing the distance between plates. As previously explained the circuit (Fig. 7.1) responds linearly with the distance between plates.

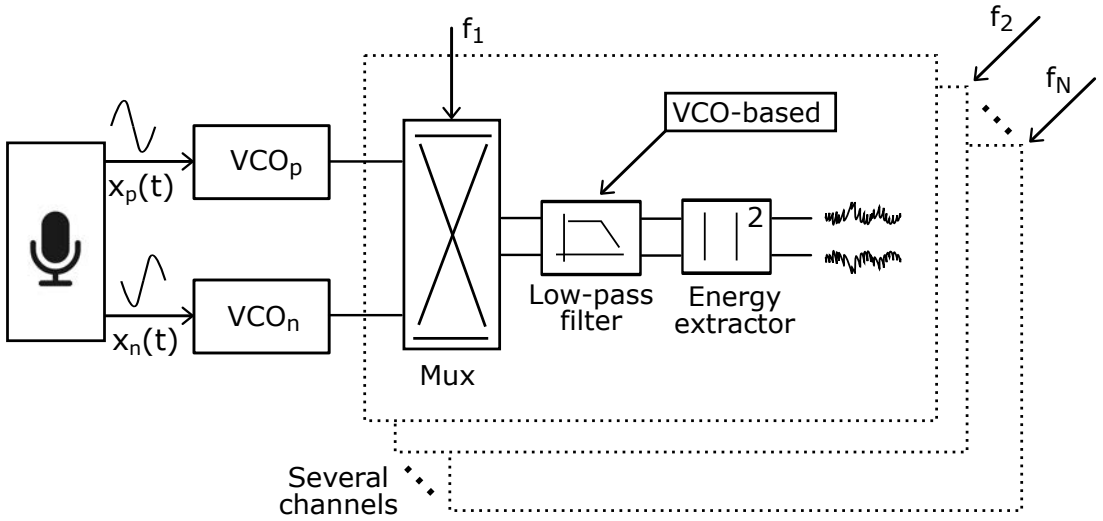

FIGURE 7.3: General diagram of the proposed VCO-based VAD architecture.

7.2 FDR filters

The enormous development of computing capabilities has enabled the efficient implementation of artificial intelligence tasks, such as speech recognition, keyword spotting or image classification [91], [92]. Whereas many of them are implemented over huge computing powered wired servers, going towards edge-computing processing is of high relevance when they are assembled on portable devices. This is the case of Voice-Activity-Detectors (VADs), which are able to detect human voice within noisy environments [93]. The interest of this task relies on directly making use of the human voice as a command for different purposes, such as enabling some operation in the cell-phone or as the first processing stage of another more complex task, like full-audio conversion or keyword spotting [94], [95].

VADs requires continuous monitoring of the input audio stream, so battery life limitations strongly apply. The conventional way to proceed is turning the analog input raw data into digital data and then performing intensive digital computation (windowing, FFT, filtering and power estimations), to extract the features within different bands, classify them and looking for data patterns compatible with human voice [96]. This approach leads to accurate classifications, but consumes much power. Other approach consists of taking the intensive digital computation into the analog domain by means of a set of analog band-pass filters and power estimators. Although the power consumption is now significantly reduced [97], large capacitors are needed to get high time constants, increasing the chip area. Simpler architectures not including smart processing have been also proposed for ultra-low power operation [98].

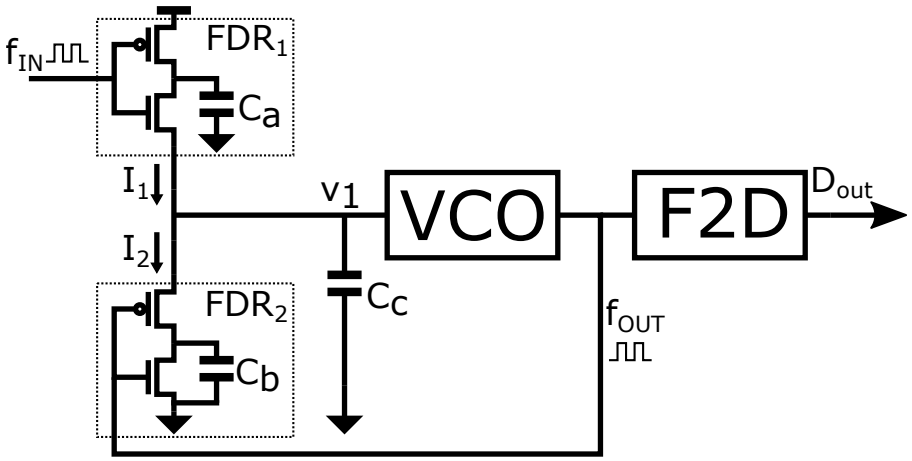

FIGURE 7.4: FDR-based low-pass filter topology.

As mentioned before in this dissertation, time-encoding has become a promising coding theme for new deep-submicron CMOS nodes, mainly due to its scalability property. Additionally they can perform low-frequency filtering without requiring large capacitors. Some examples can be found in [33], [99], [100]. A completely time-based solution for features extraction in VAD applications is proposed in [101]. This proposal uses an scheme similar to the down-conversion and filtering performed in [102] but without requiring analog mixers and operating over phase-encoded digital signals. A general diagram of the proposed solution is shown in Fig. 7.3. The analog microphone signals are pulse-frequency-modulated by a first set of front-end ring-oscillators in a pseudo-differential configuration, whose outputs are multiplexed at different frequencies to be down-converted. These ring-oscillators are common for all the required down-conversion channels and could be used afterwards for full digitization if needed. The output of each multiplexer is then low-pass filtered to be finally connected to an energy estimator. The output of the energy estimator corresponds with the amount of energy of the input audio signal $x(t)$ within the selected bands of interest.

7.2.1 Fundamental theory

Figure 7.4 shows the schematic of a first-order VCO-based low-pass filter. The input signal of the filter, $f_{IN}(t)$, is the pulse-frequency encoded output of a VCO given by the following expression (a sinusoidal input signal is assumed):

$$f_{IN}(t) = f_{rest} + f_{in} \sin(2 \cdot \pi \cdot f \cdot t) \tag{7.5}$$

This signal is connected to a switched capacitor Frequency-Dependent-Resistor (FDR), FDR_1. Using (5.3), the average currents injected into node V_1 by FDR_1 and FDR_2 are given by:

$$\begin{aligned} I_1(t) &= (V_{DD} - V_1) \cdot C_a \cdot f_{IN}(t), \\ I_2(t) &= V_1 \cdot C_b \cdot f_{OUT}(t) \end{aligned} \tag{7.6}$$

The operation of the circuit is as follows. The current $I_1(t)$ charges capacitor C_C, increasing the voltage in node V_1 which in turns increases the output frequency of the VCO, $f_{OUT}(t)$. Then, this frequency is fed back to FDR_2 and turned into a current, $I_2(t)$. Current $I_2(t)$ discharges capacitor C_C, closing a feedback loop that keeps the voltage in V_1 nearly constant, in a similar manner as an inverting amplifier constructed with an opamp and resistors. Thus it can be seen that capacitor C_C acts as an integrator, that slows the change rate of the voltage at node V_1 and thus filters fast changes in the input current $I_1(t)$, generated by fast changes in the input frequency $f_{IN}(t)$. Then, assuming that V_1 is kept constant by the negative feedback loop (VCO normalized gain, k_d, sufficiently high) through FDR_2 the low pass filter transfer function is given by:

$$\frac{f_{out}}{f_{in}}(s) = \frac{\frac{C_a}{C_c} k_{VCO}(V_{DD} - V_1)}{s + \frac{C_b}{C_c} V_1 \cdot k_{VCO}} \tag{7.7}$$

Equation 7.8 defines the normalized gain of the VCO with respect to the rest oscillation frequency f_{rest}, as in [48].

$$k_d = \frac{k_{VCO}}{f_{rest}} \tag{7.8}$$

The filter of Fig. 7.4 has only one tap of the VCO connected to the FDR_2. Connecting more taps to FDR_2 using switches would allow for the programming of the cut-off frequency of the filter. Then the cut-off frequency of the filter would be given by equation 7.9.

$$f_{3dB} = \frac{\sum_{n=1}^{N_{taps}} C_{bn} B_n}{C_c} \frac{V_1 \cdot k_{VCO}}{2\pi} \tag{7.9}$$

Where B_n is the bit controlling the switches that connect the FDR_n to the $n^{th} tap$ when equal to 1 and disconnect when 0. It should be mentioned that, in order to keep the gain of the filter constant, the same procedure applies also to FDR_1.

7.2.2 Simulation

A behavioral model of the proposed filter has been built in MATLAB/Simulink. A circuit example has been also designed and simulated with a 65-nm CMOS node.

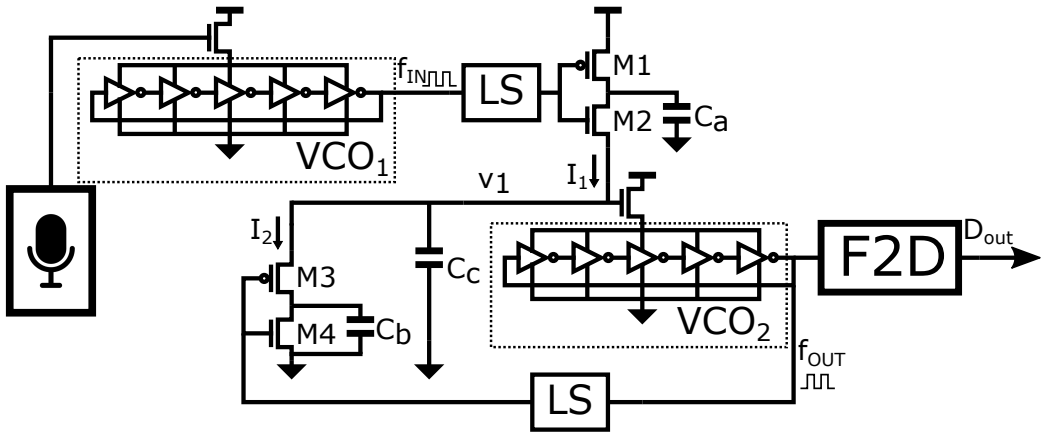

FIGURE 7.5: Transistor level schematic implemented in CMOS 65nm.

The Simulink model has been used to estimate the effect of a finite VCO normalized gain, k_d. A set of simulations has been performed for different normalized gains. In each set, the input frequency has been swept, obtaining a Bode magnitude diagram for each gain. These have been compared with the theoretical Bode from equation 7.7 for a cut-off frequency of 100 Hz. The results are shown in Figure 7.6. It can be seen that for a k_d of at least 50 the attenuation in the pass-band is less than 0.7 dB. Unfortunately, achieving such a high k_d without the use of an amplifying stage between node V_1 and the VCO is not possible. Thus, we have set a k_d of 11.5 for the transistor level circuit simulated in Cadence. With this k_d we can hope to achieve an attenuation in the pass-band of less than 2.9 dB.

The transistor level simulation has been performed in Virtuoso Cadence using a 65-nm CMOS node. A filter has been designed for a cut-off frequency of 100 Hz using the proposed topology. The filter's oscillator has been implemented using a 5-tap ring oscillator with a rest oscillation frequency of 100 kHz and a kvco of 1.16 MHz/V. For the desired cut-off frequency the value of capacitors C_a and C_b have been chosen to be 6 fF while the value of capacitor C_c is 5 pF.

Figure 7.5 shows the schematic of the circuit implemented in Cadence, with two VCOs. The first one pulse-frequency encodes the input signal and generates the signal f_{IN}. This VCO is similar to the filter's VCO described in the previous paragraph. The second one belongs to the filtering stage. Both VCOs are driven by an NMOS-based source follower (SF). In the connection between each one of the VCOs and the FDRs, a level-shifter is placed to reconstruct the signal level to a pumped voltage of 1.2 V. This level-shifter has been implemented using a behavioral model, and its power consumption is not taken into account in upcoming calculations. It is important to note, that in a real implementation these level-shifters can be made in a very simple way, thanks to the fact that the voltage in V_1 has a very small variation (for very high k_d is keep nearly constant). The

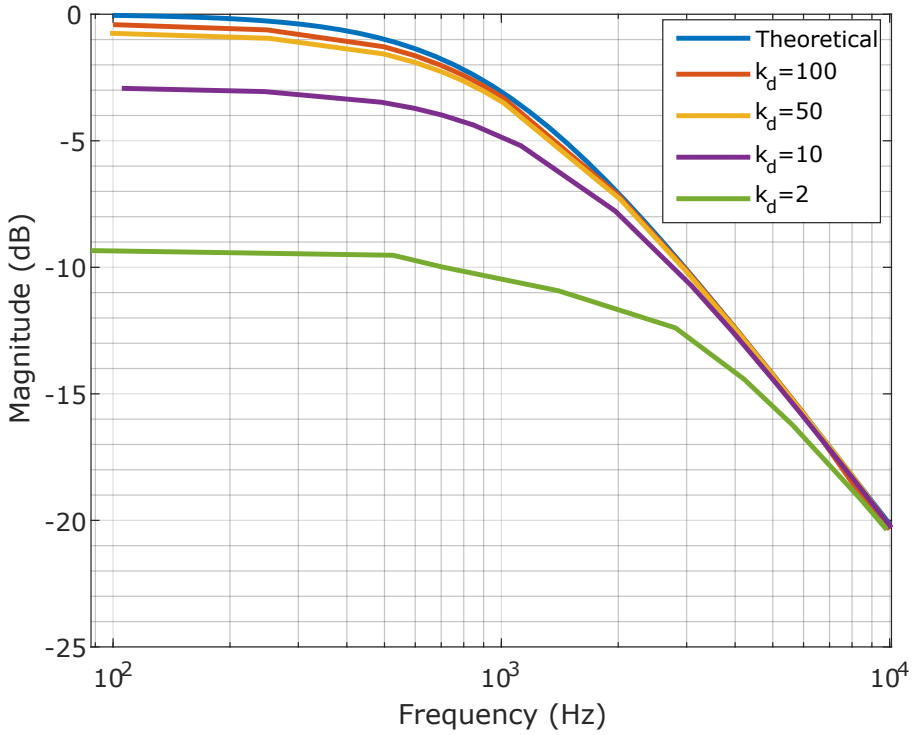

FIGURE 7.6: Effect of finite k_d.

V_{DD} of the analog circuit is 0.9 V, and the V_{bias} in the gate of the SFs is 0.45 V. The full scale range of the VCOs is then 0.18 V.

Figure 7.7 shows the simulated PSD of the input signal and the filtered output for a normalized *sinc* input signal with frequency of 2 kHz and amplitude of 44.7 mV. The results are compared with a Bode swept of the system implemented in MATLAB Simulink. From Fig. 7.7 the attenuation in the pass-band is 2.82 dB, for a k_d=11.5, which is in line with the previous discussion regarding the results of Fig.7.6.

The power consumption of the circuit of Fig. 7.5 is 8.4 nW, including the input VCO, VCO_1. The total area occupied by the circuit has been estimated from the schematic assuming a 50% more area due to routing. This total estimated area is $0.0103mm^2$, including again VCO_1. Table 7.1 shows a comparison with the state of the art, where our proposal includes estimations based on schematic and simulations, respectively of the area and power consumption of the input VCO and the low pass filters and ADCs of 20 channels without the multiplexers and the energy extractor.

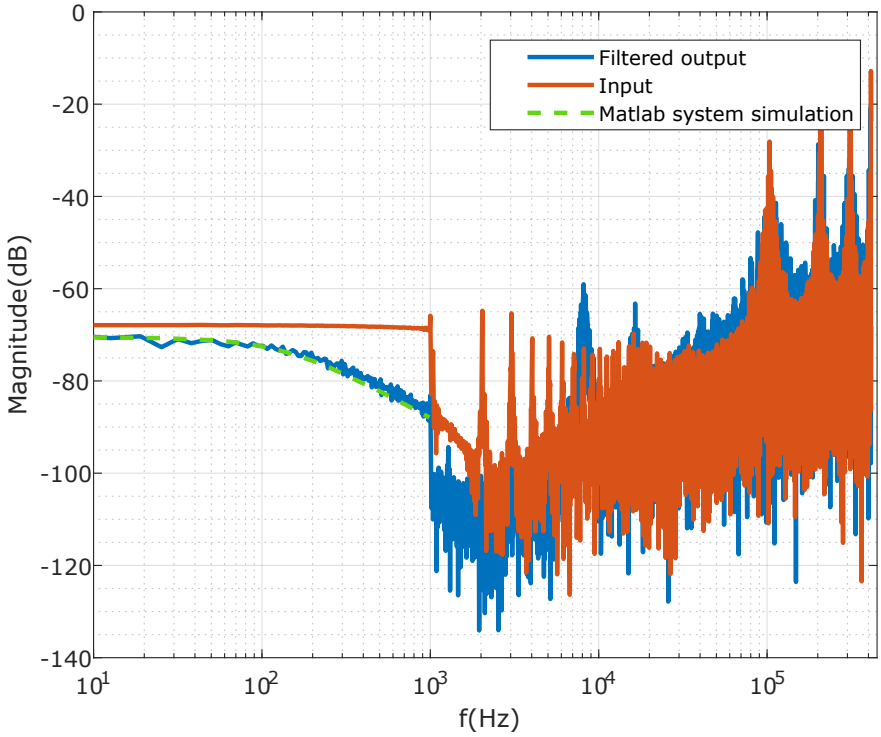

FIGURE 7.7: PSD of the simulation results of the filter implemented in TSM 65nm for a sinc input signal.

TABLE 7.1: Comparison of area and power.

Parameter	**This Work** [a]	**Badami JSSC 2016 [94]**	**Fuketa, TCAS-II 2021 [95]**	**M.Yang, JSSC 2019 [97]**	**M.Croce, JSSC 2021 [98]**
Power (μW)	0.092	0.710	0.154	0.38	0.76
Area (mm^2)	0.2	2 [b]	1.2	1.6	0.14

[a] Estimated power and area for LPF and ADC for 20 channels (Not included muxes and energy extractor)

[b] Includes mixed-signal classifier

7.2.3 Extension to second order

Figure 7.8 shows the schematic of a second order low pass filter implemented usig FDRs and VCOs. Recalling the formula of the second order low pass filter,

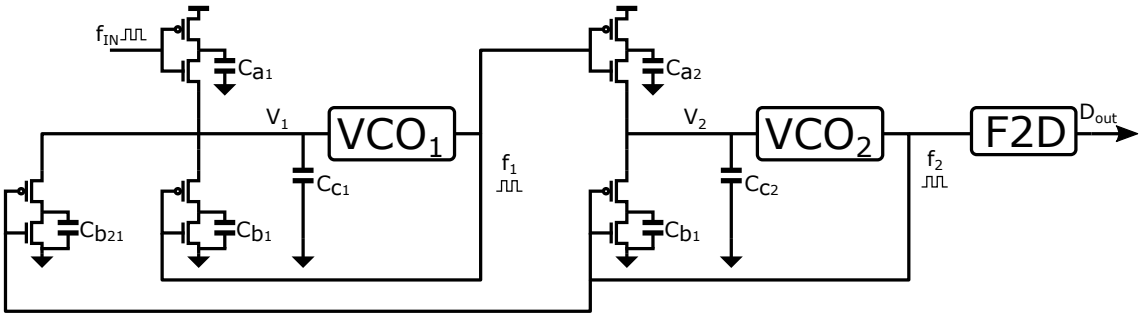

FIGURE 7.8: Schematic of the FDR + VCO based low pass filter.

the filter transfer function is given by:

$$\frac{f_{out}}{f_{in}}(s) = \frac{k\omega_0^2}{s^2 + s\frac{\omega_0}{Q} + \omega_0^2} \tag{7.10}$$

Where ω_0, k and Q are given by the following expressions:

$$\omega_0 = \sqrt{\frac{k_{VCO_1}k_{VCO_2}}{C_{C_1}C_{C_2}}(V_1C_{b_1}V_2C_{b_2}) + (V_1C_{b_{21}}(V_{DD} - V_2)C_{a_2})} \tag{7.11}$$

$$k = \frac{C_{a_1}C_{b_1}(V_{DD} - V_1)(V_{DD} - V_2)}{(V_1C_{b_1}V_2C_{b_2}) + (V_1C_{b_{21}}C_{a_1}(V_{DD} - V_2)} \tag{7.12}$$

$$Q = \frac{\sqrt{C_{C_1}C_{C_2}k_{VCO_1}k_{VCO_2}((V_1C_{b_1}V_2C_{b_2}) + (V_1C_{b_{21}}C_{a_2}(V_{DD} - V_2)))}}{(V_2C_{C_1}C_{b_2}k_{VCO_2}) + (V_1C_{C_2}C_{b_1}k_{VCO_1})} \tag{7.13}$$

This filter has been simulated at system level with $C_{a_1} = C_{a_2} = 6fF$, $C_{b_1} = C_{b_{21}} = 3fF$, $C_{b_2} = 6fF$, $V_{DD} = 0.9V$, $V_1 = V_2 = 0.45V$, $C_{C_1} = C_{C_2} = 5pF$, $f_0 = 103.7kHz$ and $k_{VCO_1} = k_{VCO_2} = 1.16MHz/V$. The cut-off frequency of the filter is 100 Hz and the $k_d = 11.2$. A sweep of the input tone has been done to obtain the magnitude response of the filter trough simulation.Results are plotted in Fig. 7.9 together with the theoretical bode. It can be seen that due to the low k_d there is a 5dB attenuation in the pass-band. Then, after the cut-off frequency the slope is -40 dB/dec.

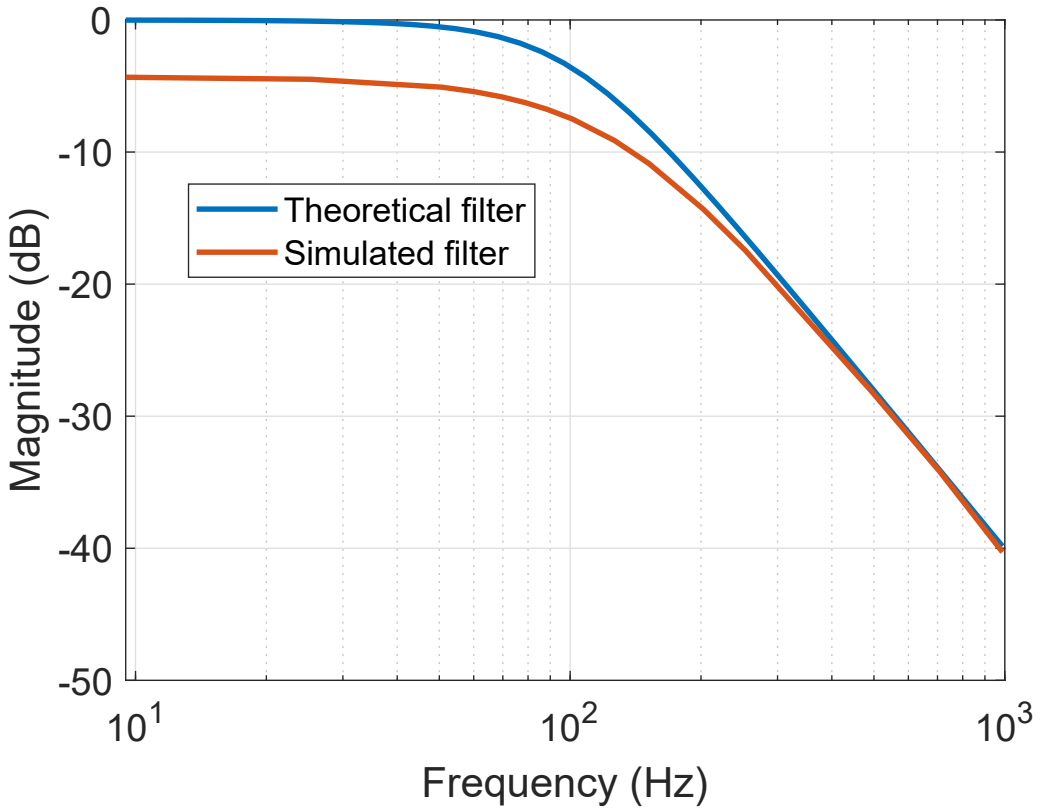

FIGURE 7.9: Simulated magnitude response of the second order filter vs theoretical.

Part IV

Conclusions

Chapter 8

Conclusions

In this thesis we have studied the use of time-encoding ADCs for MEMS microphones focusing on ring oscillator (RO) ADC topologies. Firstly we have studied at system level the implementation of Sigma-Delta modulators of second and third order with a noise-shaping dual-slope quantizer. This quantizer used a multibit feedback and thus operated similarly to a SAR-ADC. By not resetting the integrator capacitor, first order noise-shaping could be achieved. The design of Sigma-Delta loops with this noise-shaping quantizer has been analyzed.

After that we have turned our attention to the use of RO-ADCs to implement MEMS digital microphones. In this topic we have emphasized the two main circuit impairments of this type of converters, i.e. the non-linear tuning curve of the oscillator and the phase noise. Mitigation of these problems through optimized circuit design and feedback techniques has been studied in this thesis. A MEMS digital microphone chip has been fabricated and measured to test the findings of the thesis. We have focused in the analog front-end in this dissertation, leaving the digital frequency-to-digital converter to be presented in the thesis of the coauthor of the chip. The use of a single transistor source follower to interface with the MEMS sensor has proven to be a power efficient alternative for RO-ADCs. PVT variations can be a problem when using a single transistor source follower. We have proposed two ways to mitigate these problems, the use of a DAC to control the gate bias voltage and the use of a resistor between the source follower and the VCO. The addition of this resistor is a novel method that allows to trade power by SQNR controlling the current consumption and rest frequency. This resistor also helps to mitigate PVT variations and improve linearity thanks to negative feedback. The fabricated chip shows a good linearity and a good figure of merit. In addition, it is fully MEMS compatible, thanks to its high input impedance.

We have also studied the use of a frequency-to-current feedback in RO-ADCs. We have proven experimentally a simple inverter based frequency dependent resistor (FDR) to compensate the nonlinearity of a VCO-ADC. With this FDR we have implemented two FDR closed-loop RO-ADCs topologies. We have demonstrated the linearity improvement in both of them. Also phase noise improvement has been shown in measurements. The first of these structures makes use of an operational amplifier to implement a high gain loop. As a difference to previously published solutions, our circuit does not requiere non overlapped clocks

and is immune to supply variations. The chip shows a high linearity but power consumption is also elevated, mostly because of the operational amplifier. Although we have not implemented a high impedance input, this oscillator is fully compatible with a source degenerated transcondutor and thus can be made fully MEMS compatible without any power penalty.

A second FDR based feedback topology has been developed. This topology does not need the operational amplifier saving power and making it more adequate for nanometer technologies preserving the mostly digital nature of VCO-ADCs. The linearization and noise suppression are effective although more limited than in the case of the first experimental chip using an operational amplifier. Nevertheless it is a good alternative to implement the CCO with a transconductor at low voltages, with short channel transistors and high oscillator gain.

Finally, some other uses of the FDR have been explored. We have proposed a direct connection of the MEMS, making the sensor to be part of the FDR circuit to implement a capacitance to digital converter (CDC). This topology has the advantage of responding linearly to the distance between plates of the MEMS capacitor. The main limitation is its low sensitivity, limited by that of the MEMS sensor. This limits the SNDR.

The use of the FDR to implement time-encoded filters have also been explored for a voice activity detection (VAD) application. The proposed topology can be used to implement a filter with a digitally programmable cut-off frequency for FM encoded signals. Simulations show low power and area.

The main contributions of this thesis are the following:

- The contributions for the use of a SAR-NSQ based on the dual-slope architecture in Sigma-Delta loops presented in Chapter 2. This work is a first analysis of the impact of the NSQ in the design of the NTF. Further work in this area is required before reaching a functional prototype.

- The design of a MEMS digital microphone with high linearity and competitive power consumption presented in Chapter 4. The use of a SF interface is shown as a good advantage for noise and linearity optimization. Methods to deal with PVT and power regulation of the SF+ VCO architecture are implemented. This includes a novel resistor array between the SF and the VCO that is used to regulate the power consumption and rest frequency of the oscillator. This allow power mode changes during chip operation. In addition it has been shown that this resistor improves PVT and linearity of the VCO. The effectiveness of these techniques are demonstrated in a 130nm chip.

- The linearized ring oscillator using an FDR and operational amplifier presented in Chapter 5. This topology does not require a complicated control circuitry for the FDR that is implemented using inverters. Is shows a good linearity improvement over an open loop oscillator. In addition it presents

a second order phase noise transfer function that reduces the oscillator and operational amplifier noise contributions. Some useful equations and guidance for the designer are provided to optimize this transfer function. The effectiveness of this technique is demonstrated in a 130nm chip.

- A second linearized ring oscillator chip using an FDR without operational amplifier in Chapter 6. Although the linearity and noise mitigation of this topology are more limited than in the alternative with the operational amplifier, it is a very interesting choice to implement ring oscillators in nanometer technologies. The linearity improvement has been analyzed focusing on design trade-offs. Two chips using this topology are presented. The first one is a 130 nm chip where the linearity and phase noise improvement thanks to feedback are demonstrated. The second one is a power optimized oscillator in 55nm showing very good power consumption and dynamic range.

- Different uses of the FDR in chapter 7. The first one shows a CDC that linearly reacts to the change of distance between plates of the capacitor. The second, an FDR+VCO based programmable low pass filters for use in VAD applications. The feasibility of both topologies has been shown in simulation.

With these results, future research works could be oriented to:

- Further work in the use of dual-slope based SAR-NSQ in Sigma-Delta loops could focus in the implementation of a working prototype. It could also include the analysis of different topologies. Of special interest is the analysis of MASH topologies as the quantization error is readily available in voltage in the dual-slope based SAR-NSQ.

- More work in the analysis of the FDR system is needed. The PFM behaviour should be explored. The implementation a prototype optimized for noise as well as linearity, with an optimum placement of the zeros of the phase noise transfer function. Also it could be of interest to explore the implementation of single ended RO-ADCS.

- Explore the implementation of linear VCOs with the FDR in and near subthreshold using nanometer technologies.

- Design of an FDR based CDC for MEMS sensors.

- Explore the use of FDR + VCO circuits in the field of neural network seizing its FM to PFM conversion capabilities.

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