Alvero-Gonzalez, L. M., Hernandez Corporales, L. & Gutierrez, E. (2020, 18 noviembre). High-Speed and Energy-Efficient Ring-Oscillator for Analog-to-Digital Conversion. 2020 XXXV Conference on Design of Circuits and Integrated Systems (DCIS).

DOI: 10.1109/dcis51330.2020.9268623

High-Speed and Energy-Efficient Ring-Oscillator for Analog-to-Digital Conversion

Leidy Mabel Alvero-Gonzalez, Luis Hernandez Corporales, and Eric Gutierrez
Electronics Technology Department
Carlos III University of Madrid
Leganes, Spain
lalvero@ing.uc3m.es

***Abstract*—Highly dependence of the power consumption with respect to the voltage supply makes current finer CMOS technologies become supplied with lower-than-1 V. Voltage-controlled-oscillator based analog-to-digital converters implemented with ring-oscillators scales properly with that requirement. However, conventional implementations of ring-oscillators limit the oscillation frequency due to the lack of available voltage to feed high currents. In this manuscript, we propose a novel circuit for a ring-oscillator that overcomes this issue. With only two devices between the supply nodes a delay cell is built. This allows us to reduce the voltage supply for certain oscillation requirements. In addition, the lower number of devices connected to the output nodes supposes lower parasitic capacitance and a reduction in the minimum achievable time delay, which increases the potential resolution. The proposed circuit is theoretically described and validated by simulation in a 65-nm CMOS process. Comparisons to the conventional implementations are made, showing improvements in terms of resolution, power, and area.**

***Index Terms*—Analog-to-digital conversion, low overhead voltage, voltage-controlled oscillator, inverting CMOS cells**

I. Introduction

Deep-submicron CMOS processes impose new challenges when implementing mostly-analog data converters, such continuous-time $\Delta\Sigma$ modulators or flash converters. Low intrinsic gain and higher mismatch between devices, along with low voltage supplies that limit voltage overhead, make analog design highly complex [1]. In consequence, trends towards mostly digital implementations has become of special interest nowadays. Additionally, apart from overcoming previous issues with much simpler designs, digital architectures benefit from scaling, area savings and speed as devices' size is reduced.

Voltage-controlled oscillator based analog-to-digital converters (VCO-based ADCs) exploit digital scalability of the newest design processes when they are implemented with ring-oscillators [2]. Different applications, including biomedical, audio or sensing ones, make use of them due to the excellent sensitivity they have, intrinsic first-order noise-shaping spectral properties and remarkable noise performance [3]–[5]. If we focus on ring-oscillator based open-loop structures, the main limitation will become the non-linear voltage/current to frequency relation [6]. Some techniques to overcome that issue can be found in the literature, which includes limiting the input signal swing [7] or adding digital calibration [5].

Whereas oversampling allows us to get enough resolution for low-bandwidth architectures, this is not the case for high-bandwidth ones (whose bandwidth may be around dozens of MHz). For these applications, minimum delay cells that compose the ring-oscillator turns out to be a limiting factor, strongly limiting the final resolution we may get from the data converter, specially if we limit the voltage supply to reduce power consumption. In this manuscript we propose a new delay cell for the implementation of high-speed low-power ring-oscillators, with a minimum delay which is lower than the one achieved for the conventional delay cell used in ring-oscillators. We will see that the power consumption will depend on the number of cells in the ring-oscillator, unlike it occurs conventionally. Then, our solution will be of interest when using a reduced number of cells in the ring-oscillator in such a way that we move the computing charge from the oscillator to the digital logic afterwards. In consequence, high speed digital logic implemented with a narrow CMOS process is a must. The new delay cell is highly portable between technology nodes and suitable with high-bandwidth applications such as wireless and IoT-related devices.

The outline of the manuscript is as follows. Section II summarizes the foundations of ring-oscillator based ADCs and the conventional approach typically made. Section III describes the new delay-cell proposed for the implementation of low power and high speed ring-oscillators. In Section IV a ring-oscillator with the new delay-cell implemented in a 65-nm CMOS process is presented along with some transient simulations to validate the approach. Finally, Section V concludes the manuscript.

II. Ring-oscillators for analog-to-digital conversion

A. Open-loop structure for VCO-based ADCs

Fig.1 depicts the general scheme of an open-loop ring-oscillator based ADC [7], where the ring-oscillator may be built either as a voltage-controlled-oscillator (VCO) or as a current-controlled-oscillator (CCO). Input signal $x(t)$ modulates the oscillation frequency according to the following expression:

$$f_{\text{osc}}(t) = f_{\text{o}} + K_{\text{VCO}} \cdot g_{\text{m}} \cdot x(t) \tag{1}$$

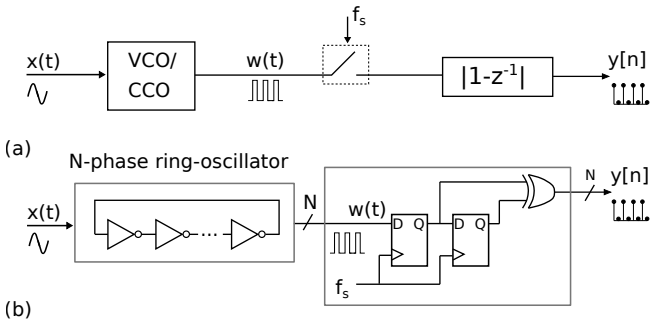


Fig. 1: (a) Open-loop structure of VCO-based ADC, and (b) possible circuit implementation of (a).

where f_o is the rest oscillation frequency and K_{VCO} is the oscillator gain. The output phases of the ring-oscillator are then sampled and first-differentiated to generate the output data $y[n]$, which are first-order noise-shaped.

A possible circuit for Fig. 1(a) is shown in Fig. 1(b), where the mostly-digital implementation of these systems can be observed. The structure of the digital logic depends on the relationship between the sampling frequency (f_s) and the highest oscillation frequency in the ring-oscillator. In the case of having f_{osc} restricted to lower than f_s/2 the implementation of Fig. 1(b) is suitable. Otherwise, asynchronous more-than-one-bit digital counters connected to the output phases will be required. This is of high relevance for us because in our new proposal we will limit the number of cells that compose the ring-oscillator to save power, usually leading to oscillation frequencies higher than f_s/2.

B. Conventional ring-oscillator circuit for VCO-based ADCs

The most common circuit for a ring-oscillator is shown in Fig. 2. A voltage-to-current conversion is made by M_1 and the output current I_{RO} flows through a ring configuration built with CMOS inverters. The higher I_{RO}, the lower the delay of the inverters and the higher the oscillation frequency. C_L represents the equivalent load of the digital logic connected to each phase and needed to generate the output data.

It is important to note here that the current I_{RO} flows only through those delay cells whose state is changing. This means that the power consumption of the structure does not depend on the number of delay cells, as opposite to the new delay cell that will be proposed afterwards.

The lowest delay we may have in the cells will define the highest time resolution we will achieve from the converter. This becomes a limitation when oversampling ratio is low due to high bandwidths, such as in wireless or IoT applications.

III. High-speed delay cell for ring-oscillator

To overcome the resolution limitation described above, we propose to use the delay-cell of Fig. 3 to implement ring-oscillators. This cell has the same structure of a common-source amplifier where the gate of the active load is connected

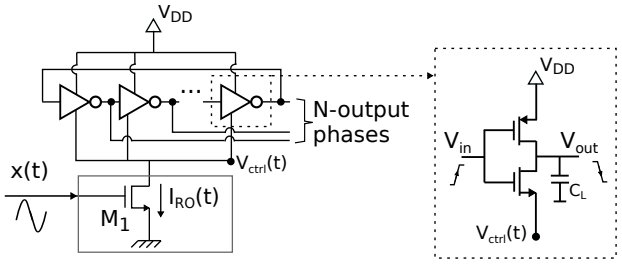


Fig. 2: Conventional ring-oscillator implementation for VCO-based ADCs.

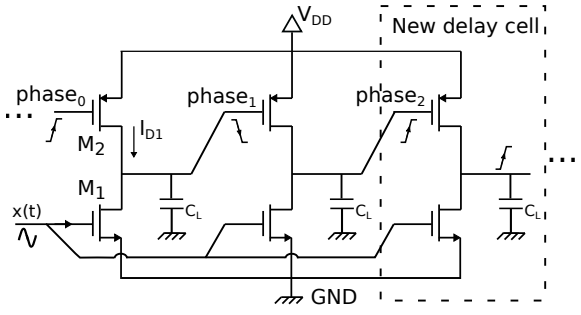


Fig. 3: New high-speed delay cell for ring-oscillators.

to the previous cell. M_1 makes the voltage-to-current conversion and controls the oscillation frequency similarly to M_1 of Fig 2.

Whereas the conventional delay cell is composed of three devices, the inverter cell itself and the M_1 transistor; in the new approach each cell is only composed of two devices. Firstly, this alleviates headroom voltage of M_1, allowing us to decrease the voltage supply V_{DD}. Secondly, the parasitic capacitance at the output nodes is reduced, which increases the highest possible oscillation frequency. Finally, we have a penalty in the power consumption due to the static current when the M_2 is enabled. We will see later on how to deal with this issue to get an energy-efficient solution.

A. Delay cell's start-up conditions

If the sizes for both M_1 and M_2 devices are not correctly selected, there might be a solution for the operating region of both devices in which the input and the output of cell have the same voltage value, leading to a non-oscillating operating point. Looking at Fig. 3 and considering three consecutive delay cells, a non-oscillating operating point will be achieved when the operating regions of M_1 and M_2 are reversed for each consecutive cell. The boundary between the non-oscillating operating point and the oscillating operating point occurs when the sizes of M_1 and M_2 are linear and saturation region, respectively, and interchanged for the next delay cell. This condition will provide minimum sizes for M_1 and M_2. Going away from the calculated minimum sizes will make $phase_0$ become closer to V_{DD}, $phase_1$ become closer to GND, and $phase_2$ become closer to V_{DD}.

Below, we will calculate what is the minimum size for both devices needed to make the structure oscillate. Let's focus on the first cell of Fig. 3 and assume that M_1 is working in linear region and M_2 in saturation region. If we suppose that capacitor C_L is charged we may equal the currents that flow through M_1 and M_2:

$$0.5K_P^{'}\left(\frac{W}{L}\right)_{M2}\left(V_{DD}-V_{ph,0}-|V_{th,P}|\right)^2\cdot \cdot\left(1+\lambda_P\left(V_{DD}-V_{ph,0}\right)\right)= K_N^{\prime}\left(\frac{W}{L}\right)_{M1}\left(x(t)-V_{th,N}-\frac{V_{ph,1}}{2}\right)V_{ph,1}, \quad (2)$$

where K is , BLA, BLA,etc.

We may do the same for the next cell, but reversing the operating regions of M_1 and M_2:

$$K_P^{\prime}\left(\frac{W}{L}\right)_{M2}\left(V_{DD}-V_{ph,1}-|V_{th,P}|-\frac{V_{DD}-V_{ph,2}}{2}\right)\cdot \cdot\left(V_{DD}-V_{ph,2}\right)= 0.5K_N^{'}\left(\frac{W}{L}\right)_{M1}\left(x(t)-V_{th,N}\right)^2\left(1+\lambda_N V_{ph,2}\right) \quad (3)$$

where $V_{ph,2}$ equals $V_{ph,0}$. If we now take both equations (2) and (3) and solve the resulting system of equations, we will achieve an oscillating operation point if both $V_{ph,1}$ and $V_{ph,0}$ are real and compatible with the initial operating points considered for M_1 and M_2 in two consecutive cells. The solution depends on the value assigned to the input signal $x(t)$, where the maximum value of $x(t)$ defines the worst case possible to get oscillation.

If we consider the boundary between linear and saturation region for both M_1 and M_2 devices, we may calculate the minimum size ratio required to make the structure oscillate, which is as follows:

$$\frac{(W/L)_{M2}}{(W/L)_{M1}}\geq\frac{K_N^{'}}{K_P^{'}}\cdot\frac{\left(x(t)-V_{th,N}\right))^2}{\left(V_{DD}-|V_{th,P}|\right))^2}. \quad (4)$$

For the sake of simplicity, we have not considered channel modulation in (4). If assumed we would observe that the minimum ratio defined in (4) would decrease, making it more suitable for newer processes. When the designed size ratio is lower than the value provided by (4) we will not have oscillation at the output nodes.

To provide some intuition about the reference values we may find for the minimum size ratio, we have taken the values for a 50-nm and a 1-μm CMOS technologies [9]. Whereas for the 50-nm process the minimum size equals approximately 2, for the 1-μm process it equals approximately 3. This minimum size ratio value must be found out for each process, making use of it to reduce the occupied area and also speed up the oscillation frequency.

B. Energy-efficient delay cell configuration

The proposed delay cell has the disadvantage of consuming static power when the input of the delay cell is at low state. When included into a ring-oscillator configuration all the cells will spend half of the time at low state. Consequently, the higher the number of taps the higher the power consumption. According to [8], resolution in a VCO-based ADC depends on the effective oscillation frequency, which is defined as follows:

$$f_{osc,eff}(t)=N\cdot f_{osc}(t), \quad (5)$$

where N is the number of delay cells in the ring-oscillator. This means that similar resolution can be achieved with different number of delay cells while the effective oscillation frequency remains constant. This way, resoluti

To reduce power consumption in the new proposal and go to an energy-efficient architecture we propose to limit the number of cells in the ring-oscillator, keeping the same effective oscillation frequency, and moving the computing charge from the analog side to the digital side, what requires of high-speed logic. That is the reason why our proposal is specially suitable for newer narrow CMOS process.

IV. Practical validation and simulations

Both the oscillators of Fig. 2 and Fig. 3 have been designed in a 65-nm CMOS process with the goal of validating the advantages of the new approach and verifying its performance.

We have designed several ring-oscillators with both cells using different number of cells and with the same oscillation parameters, Fig. **??** and Fig. **??**. In both figures it should be appreciated that, whereas the power consumption for the conventional ring-oscillator only depends on the effective oscillation frequency regardless the number of cells, it is not the case for the new one. For the new ring-oscillator the power consumption depends on both terms, the effective oscillation frequency but also the number of cells. The most efficient solution is achieved when, for a given effective oscillation frequency, we design a ring-oscillator with the lowest number of cells possible.

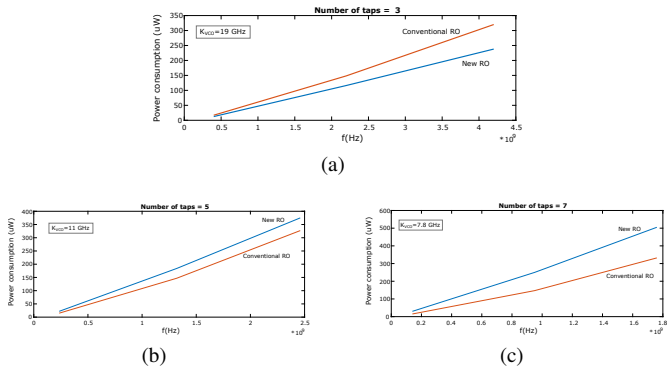
In Fig. **??** the ring-oscillators are designed for the same voltage supply, which is 0.8 V. Here the delay for the conventional cell is minimized while not for the new one, what proves the possibility of reducing the minimum time delay achievable. 3-, 5-, and 7-cell ring-oscillators were simulated. The new oscillator consumes less than the conventional one for the 3-cell implementation, but not for the 5- and 7-cell ones. In this particular case the new approach is more energy efficient if less than 5-cell ring-oscillators are used. This limit could be enhanced if faster delay cells were used for the new ring-oscillator and the voltage supply were reduced.

ver por qué tanto espacio entre el título de la fig y la figura

In Fig. **??** the voltage supply is set to 0.7 V for the new circuit, keeping the oscillation parameters of the previous analysis. In this case the new oscillator consumes less than the conventional one for the 3- and 5-cell implementation, but not 7-cell one, increasing the limit we have observed in Fig. **??**.

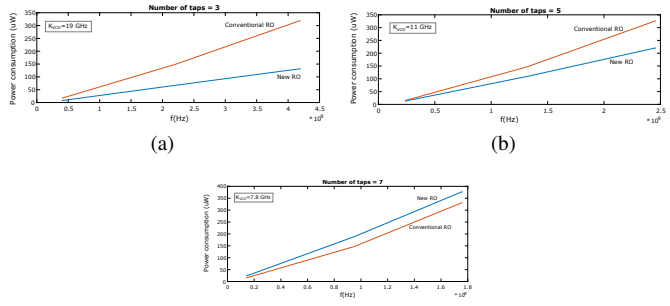
en este cason deja tanto espacio entre el título y la figura

Finally, using a 3-cell implementation for both configurations, we test a reduction of overhead voltage and studied the performance in terms of speed, power consumption and



(a) (b) (c)

Fig. 4: Conventional oscillator vs proposed power consumption with voltage supply of 0.8 V



(a) (b) (c)

Fig. 5: Conventional oscillator vs proposed power consumption with voltage supply of 0.8 V and 0.7 V respectively

area. The voltage supply was decreased and, this time, the oscillation frequency parameter was examined.

verificando:For three values -900 mV, 800 mV, and 700 mV- the oscillation frequency for a RO structure composed of CMOS inverters slow downed (more than 1.5 GHz) finally getting a value of $f_{\max}$= 2.2 GHz, consequently, the current is reduced as well. For our RO, the oscillation is not affected and the current is significantly decreased. For same oscillation parameters (f_o= 2.4 GHz and K_{VCO}= 15 GHz), the conventional RO and the proposed RO feed with 1 V and 700 mV respectively, the power consumption of the first one is nearly twice of the second one.

Analyzing both RO structures, it could be said, in rough terms, that the most common structure for RO is not totally power-efficient if it is composed by a few taps. In addition, this kind of configuration is limited by the transconductor that controls the current through CMOS inverters and defines the oscillation frequency: the miniaturization of CMOS processes suppose a constant falling of voltage supply, which penalizes the good performance for the conventional RO. On the contrary, the new cell constitutes a potential solution to the overhead voltage issue, keeping a small number of taps for VCO. The circuit proposed manages a lower load compared with typical RO because the output is connected to only one gate terminal of transistor, therefore, the size of transistors will be lower for certain oscillation frequency or faster oscillator can be obtained.

V. Conclusion

A novel inverting cell of ring-oscillator for the implementation of oversampled ADCs has been formulated. The proposed circuit is composed by one NMOS -as a transconductor- and one PMOS, which keep an oscillating regimen depending on the size ratio between both devices. This particular configuration allows us to built RO with a higher oscillation frequency, lower power consumption and area, in comparison with the conventional structures of RO used for VCO-based ADCs. The new RO is validated by transient simulation in a 65-nm CMOS process, showing proper performance for very small overhead voltage. Additionally, a circuit devoted to digitize the output signals (level-shifter) is not especially important, replacing it by another simpler circuit, and simplifying the whole conversion architecture. This features offers a good solution for ADC architectures based on oscillators in view of the development of deep-submicron CMOS processes. The new cell could be applied either open-loop configurations or closed-loop configurations.

References

[1] W. Sansen, "1.3 Analog CMOS from 5 micrometer to 5 nanometer," 2015 IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers, San Francisco, CA, 2015, pp. 1-6, doi: 10.1109/ISSCC.2015.7062848.

[2] J. Jalil, M. B. I. Reaz, and M. A. M. Ali, "CMOS Differential Ring Oscillators:Review of the Performance of CMOS ROs in Communication Systems," IEEE Microwave Magazine, vol. 14, no. 5, pp. 97–109, July 2013.

[3] E. Gutierrez, P. Rombouts and L. Hernandez, "Why and How VCO-based ADCs can improve instrumentation applications," 2018 25th IEEE International Conference on Electronics, Circuits and Systems (ICECS), Bordeaux, 2018, pp. 101-104, doi: 10.1109/ICECS.2018.8618004.

[4] A. Babaie-Fishani and P. Rombouts, "A Mostly Digital VCO-Based CTSDM With Third-Order Noise Shaping," IEEE Journal of Solid-State Circuits, vol. 52, no. 8, pp. 2141–2153, Aug 2017.

[5] W. Jiang, V. Hokhikyan, H. Chandrakumar, V. Karkare and D. Marković, "A ±50-mV Linear-Input-Range VCO-Based Neural-Recording Front-End With Digital Nonlinearity Correction," in IEEE Journal of Solid-State Circuits, vol. 52, no. 1, pp. 173-184, Jan. 2017, doi: 10.1109/JSSC.2016.2624989.

[6] J. Kim, T. K. Jang, Y. G. Yoon, and S. Cho, "Analysis and Design of Voltage-Controlled Oscillator Based Analog-to-Digital Converter," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 57, no. 1, pp. 18–30, Jan 2010.

[7] V. Nguyen, F. Schembari and R. B. Staszewski, "A 0.2-V 30-MS/s 11b-ENOB Open-Loop VCO-Based ADC in 28-nm CMOS," in IEEE Solid-State Circuits Letters, vol. 1, no. 9, pp. 190-193, Sept. 2018, doi: 10.1109/LSSC.2019.2906777.

[8] E. Gutierrez, L. Hernandez, F. Cardes and P. Rombouts, "A Pulse Frequency Modulation Interpretation of VCOs Enabling VCO-ADC Architectures With Extended Noise Shaping," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 65, no. 2, pp. 444-457, Feb. 2018.

[9] R. Jacob Baker. 2010. "CMOS Circuit Design, Layout, and Simulation" (3rd. ed.). Wiley-IEEE Press.