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Doctoral Thesis

Data Acquisition Techniques Based on Frequency-Encoding Applied to Capacitive MEMS Microphones

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Tesis Doctoral

Data Acquisition Techniques Based on Frequency-Encoding Applied to Capacitive MEMS Microphones

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Abstract

This thesis focuses on the development of capacitive sensor readout circuits and data converters based on frequency-encoding. This research has been motivated by the needs of consumer electronics industry, which constantly demands more compact readout circuit for MEMS microphones and other sensors. Nowadays, data acquisition is mainly based on encoding signals in voltage or current domains, which is becoming more challenging in modern deep submicron CMOS technologies.

Frequency-encoding is an emerging signal processing technique based on encoding signals in the frequency domain. The key advantage of this approach is that systems can be implemented using mostly-digital circuitry, which benefits from CMOS technology scaling. Frequency-encoding can be used to build phase referenced integrators, which can replace classical integrators (such as switched-capacitor based integrators) in the implementation of efficient analog-to-digital converters and sensor interfaces. The core of the phase referenced integrators studied in this thesis consists of the combination of different oscillator topologies with counters and highly-digital circuitry.

This work addresses two related problems: the development of capacitive MEMS sensor readout circuits based on frequency-encoding, and the design and implementation of compact oscillator-based data converters for audio applications.

In the first problem, the target is the integration of the MEMS sensor into an oscillator circuit, making the oscillation frequency dependent on the sensor capacitance. This way, the sound can be digitized by measuring the oscillation frequency, using digital circuitry. However, a MEMS microphone is a complex structure on which several parasitic effects can

influence the operation of the oscillator. This work presents a feasibility analysis of the integration of a MEMS microphone into different oscillator topologies. The conclusion of this study is that the parasitics of the MEMS limit the performance of the microphone, making it inefficient. In contrast, replacing conventional ADCs with frequency-encoding based ADCs has proven a very efficient solution, which motivates the next problem.

In the second problem, the focus is on the development of high-order oscillator-based $\Sigma\Delta$ modulators. Firstly, the equivalence between classical integrators and phase referenced integrators has been studied, followed by an overview of state-of-art oscillator-based converters. Then, a procedure to replace classical integrators by phase referenced integrators is presented, including a design example of a second-order oscillator-based $\Sigma\Delta$ modulator. Subsequently, the main circuit impairments that limit the performance of this kind of implementations, such as phase noise, jitter or metastability, are described.

This thesis also presents a methodology to evaluate the impact of phase noise and distortion in oscillator-based systems. The proposed method is based on periodic steady-state analysis, which allows the rapid estimation of the system dynamic range without resorting to transient simulations. In addition, a novel technique to analyze the impact of clock jitter in $\Sigma\Delta$ modulators is described.

Two integrated circuits have been implemented in 0.13 μm CMOS technology to demonstrate the feasibility of high-order oscillator-based $\Sigma\Delta$ modulators. Both chips have been designed to feature second-order noise shaping using only oscillators and digital circuitry. The first testchip shows a malfunction in the digital circuitry due to the complexity of the multi-bit counters. The second chip, implemented using single-bit counters for simplicity, shows second-order noise shaping and reaches 103 dB-A of dynamic range in the audio bandwidth, occupying only 0.04 mm^2.

Resumen

Esta tesis se centra en el desarrollo de conversores de datos e interfaces para sensores capacitivos basados en codificación en frecuencia. Esta investigación está motivada por las necesidades de la industria, que constantemente demanda reducir el tamaño de este tipo de circuitos. Hoy en día, la adquisición de datos está basada principalmente en la codificación de señales en tensión o en corriente. Sin embargo, la implementación de este tipo de soluciones en tecnologías CMOS nanométricas presenta varias dificultades.

La codificación de frecuencia es una técnica emergente en el procesado de señales basada en codificar señales en el dominio de la frecuencia. La principal ventaja de esta alternativa es que los sistemas pueden implementarse usando circuitos mayoritariamente digitales, los cuales se benefician de los avances de la tecnología CMOS. La codificación en frecuencia puede emplearse para construir integradores referidos a la fase, que pueden reemplazar a los integradores clásicos (como los basados en capacidades conmutadas) en la implementación de conversores analógico-digital e interfaces de sensores. Los integradores referidos a la fase estudiados en esta tesis consisten en la combinación de diferentes topologías de osciladores con contadores y circuitos principalmente digitales.

Este trabajo aborda dos cuestiones relacionadas: el desarrollo de circuitos de lectura para sensores MEMS capacitivos basados en codificación temporal, y el diseño e implementación de conversores de datos compactos para aplicaciones de audio basados en osciladores.

En el primer caso, el objetivo es la integración de un sensor MEMS en un oscilador, haciendo que la frecuencia de oscilación depende de la

capacidad del sensor. De esta forma, el sonido puede ser digitalizado midiendo la frecuencia de oscilación, lo cual puede realizarse usando circuitos en su mayor parte digitales. Sin embargo, un micrófono MEMS es una estructura compleja en la que múltiples efectors parasíticos pueden alterar el correcto funcionamiento del oscilador. Este trabajo presenta un análisis de la viabilidad de integrar un micrófono MEMS en diferentes topologías de oscilador. La conclusión de este estudio es que los parasíticos del MEMS limitan el rendimiento del micrófono, causando que esta solución no sea eficiente. En cambio, la implementación de conversores analógico-digitales basados en codificación en frecuencia ha demostrado ser una alternativa muy eficiente, lo cual motiva el estudio del siguiente problema.

La segunda cuestión está centrada en el desarrollo de moduladores $\Sigma\Delta$ de alto orden basados en osciladores. En primer lugar se ha estudiado la equivalencia entre los integradores clásicos y los integradores referidos a la fase, seguido de una descripción de los conversores basados en osciladores publicados en los últimos años. A continuación se presenta un procedimiento para reemplazar integradores clásicos por integradores referidos a la fase, incluyendo un ejemplo de diseño de un modulador $\Sigma\Delta$ de segundo orden basado en osciladores. Posteriormente se describen los principales problemas que limitan el rendimiento de este tipo de sistemas, como el ruido de fase, el jitter o la metaestabilidad.

Esta tesis también presenta un nuevo método para evaluar el impacto del ruido de fase y de la distorsión en sistemas basados en osciladores. El método propuesto está basado en simulaciones PSS, las cuales permiten la rápida estimación del rango dinámico del sistema sin necesidad de recurrir a simulaciones temporales. Además, este trabajo describe una nueva técnica para analizar el impacto del jitter de reloj en moduladores $\Sigma\Delta$.

En esta tesis se han implementado dos circuitos integrados en tecnología CMOS de 0.13 μm, con el fin de demostrar la viabilidad de los moduladores $\Sigma\Delta$ de alto orden basados en osciladores. Ambos chips han sido diseñados para producir conformación espectral de ruido de segundo orden, usando únicamente osciladores y circuitos mayoritariamente digitales. El primer chip ha mostrado un error en el funcionamiento de los

circuitos digitales debido a la complejidad de las estructuras multi-bit utilizadas. El segundo chip, implementado usando contadores de un solo bit con el fin de simplificar el sistema, consigue conformación espectral de ruido de segundo orden y alcanza 103 dB-A de rango dinámico en el ancho de banda del audio, ocupando solo 0.04 mm^2.

Acknowledgments

I would like to express my most sincere gratitude and appreciation to all the people who have contributed to make this thesis possible.

First and foremost, I would like to express my gratitude to my PhD advisor, Luis, for his extensive support during these years. His continued guidance and brilliant ideas have made this research possible.

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Contents

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List of abbreviations

ADC	Analog-to-digital converter
AM	Amplitude modulation
AOP	Acoustic overload point
ASIC	Application-specific integrated circuit
CCO	Current-controlled oscillator
CMOS	Complementary metal-oxide-semiconductor
CMRR	Common-mode rejection ratio
CT	Continuous time
DAC	Digital-to-analog converter
DBP	Dual backplate
DCO	Digitally-controlled oscillator
DEM	Dynamic element matching
DR	Dynamic range
DSP	Digital signal processing
DT	Discrete time
DWA	Data weighted averaging
F2D	Frequency-to-digital
FM	Frequency modulation
FoM	Figure-of-merit
HB	Harmonic balance
IRPN	Input referred phase noise
LDO	Low dropout regulator
MASH	Multi-stage noise-shaping
MEMS	Microelectromechanical system
MOS	Metal-oxide-semiconductor
NCF	Noise cancellation filter
NRZ	Non-return-to-zero

NTF	Noise transfer function
OSR	Oversampling ratio
PCB	Printed circuit board
PFM	Pulse frequency modulation
PLL	Phase-locked loop
PM	Phase modulation
PRI	Phase referenced integrator
PSD	Power spectral density
PSS	Periodic steady-state
RMS	Root mean square
RO	Ring oscillator
RZ	Return-to-zero
SBP	Single backplate
SC	Switched-capacitor
ΣΔM	Sigma-Delta modulator
SDR	Signal to distortio ratio
SNDR	Signal to noise and distortion ratio
SNR	Signal to noise ratio
SPL	Sound pressure level
STF	Signal transfer function
THD	Total harmonic distortion
UDC	Up-down counter
VCO	Votlage-controlled oscillator
VCRO	Votlage-controlled ring oscillator
ZOH	Zero-order hold

Introduction

Over the last decades, the semiconductor industry has experienced a revolution due to countless improvements achieved in production techniques. The minimum size of MOS transistors has been reduced in several orders of magnitude, allowing the fabrication of several billions of transistors on a single integrated circuit. These technological advances have increased the competitiveness of digital circuits, which are nowadays incomparably more efficient in terms of silicon area and power consumption than its analog counterparts.

However, digital systems are not directly compatible with most of the real-world magnitudes with which human beings interact, such as temperature, pressure, acceleration, etc. These magnitudes (known as "measurands") can be transformed into electrical signals by means of transducers, which generate analog signals proportional to the measured magnitude. Analog signals can take any value in a certain range, and can change at any time. Conversely, digital signals can only take a finite number of values at a finite number of instant per unit of time. In other words, a digital system operates in discrete-time and requires a quantized signal. In consequence, modern sensors are typically composed of two stages: the first stage is based on a transducer element which transforms the measurand into an analog signal, whereas the second stage transforms this signal into a digital sequence compatible with digital circuitry.

In the past, the use of sensors was limited to industry, defense, and a few specific applications. However, nowadays, sensors are present in everyday life, and the evolution of smart phones, wearable devices and Internet of Things have boosted demand for CMOS-based integrated

sensors. Given that these devices are frequently powered using batteries, the development of low-power sensors is essential to extend battery life. The other main interest of this industry is reducing the silicon area occupied by each sensor, which reduces fabrication costs and facilitates the integration of the device in compact packages.

Audio acquisition is one of the most active sectors in the development of sensors, due to its relevance in mobile telephony and its potential applications in noise cancellation, voice recognition, and voice-controlled devices. Miniaturized microphones are typically fabricated as micro-electromechanical systems (MEMS), built over a semiconductor material with moving parts. MEMS microphones are connected to CMOS readout circuits, which measure the capacitance of the sensor and generate the digital output of the sensor. In most of the cases, readout circuits are based on injecting an electrical charge into the MEMS capacitor and reading out the capacitor voltage through a conventional analog-to-digital converter (ADC), typically a $\Sigma\Delta$ modulator, as shown in Figure I.1.

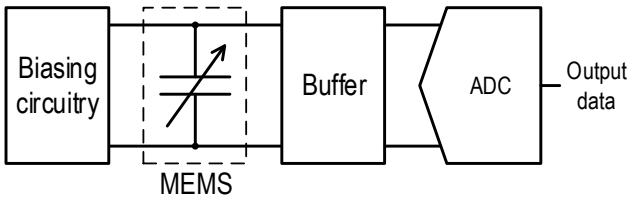

Figure I.1: Simplified diagram of a typical readout circuit for MEMS microphones.

There are strong trends towards reducing the power consumption, the silicon area, and the power supply of miniaturized sensors. Unfortunately, meeting these specifications following the current approach present important challenges. On one hand, the biasing circuitry required to maintain the MEMS charged at a constant charge frequently operates at relatively high voltages (typically between 3 V and 8 V), which hinders the implementation of this kind of systems in modern CMOS technologies. On the other hand, reducing the area, the power consumption, and the supply voltage of classical $\Sigma\Delta$ modulators built with operational amplifiers is not evident.

Motivation and objectives of this thesis

Frequency-encoding is an emerging technique which has great potential for development of compact circuits in CMOS technology. In short, frequency-encoding consists on using the input signal to modulate the frequency of a carrier signal, which can be efficiently post-processed (typically using mostly-digital circuitry) to recover the original signal. The main objective of this thesis is the study of frequency-encoding approaches to design efficient readout circuits for sensors, and specifically for capacitive MEMS microphones.

Figure I.2 illustrates the two frequency-encoding based readout circuits considered in this thesis. In both cases, the changes in the MEMS capacitance due to sound pressure variations modulate the oscillation frequency of an oscillator, whose output is digitized using a frequency-to-digital converter. In the architecture of Figure I.2(a) the MEMS is used as part of the oscillator, influencing its time constant. In consequence, any change in the MEMS capacitance alters the oscillation frequency. In this case the biasing circuitry is not required, and the system can theoretically operate at low supply voltages. However, the direct connection between the MEMS and the oscillator may be problematic due to MEMS parasitics. On the other hand, Figure I.2(b) depicts a readout circuit based on the classical biasing shown in Fig. I.1, on which the analog-to-digital conversion is performed using an oscillator-based $\Sigma\Delta$ modulator. Although this approach requires a biasing circuitry, the interconnection between the readout circuit and the MEMS is not a problem.

Digital MEMS microphones typically feature a single-bit digital output with a sampling rate of several MHz. This requirement prevents the use of first-order $\Sigma\Delta$ modulators, which would require higher sampling frequencies of multi-bit quantizers in order to reach the target dynamic range (typically higher than 96 dB). In contrast, high-order $\Sigma\Delta$ modulators are better suited for this application since the target resolution can be reached with a digital output compatible with current interfaces. For this reason, this work proposed the implementation of high-order oscillator-based $\Sigma\Delta$ modulators for MEMS microphones

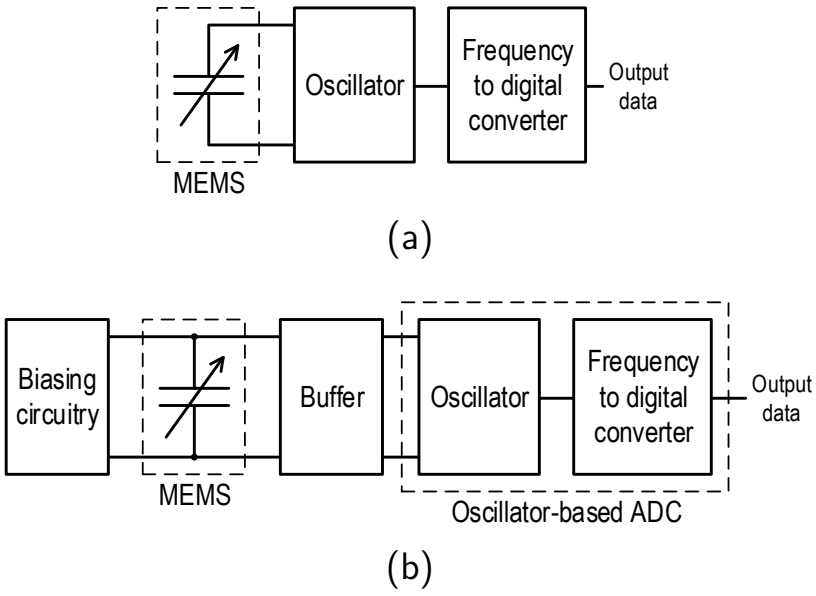

Figure I.2: Simplified diagrams of two possible time-encoding based readout circuits. (a) Direct connection between MEMS and oscillator. (b) Classical MEMS biasing with oscillator-based ADC.

readout circuits.

In addition to the evaluation of these two approaches, this thesis also aims at studying the main circuit impairments that limit the performance of oscillator-based systems. On one hand, phase noise and distortion limit the accuracy of the frequency-encoding process in oscillators. The influence of these two effects in the performance of the system could be evaluated through the in-depth analysis of the oscillator circuit. However, this calculation is in most of the cases very tedious, and circuit-level simulations are preferred. Unfortunately, in some applications the computing time required to obtain transient simulations with enough number of points is too long. In consequence, another objective proposed for this thesis is the development of a simulation methodology to estimate the limitations of phase noise and distortion without resorting to time-consuming transient simulations.

On the other hand, random variations in the sampling period (known as clock jitter) degrade the performance of ADCs, specially in the case of continuous-time $\Sigma\Delta$ modulators. Although this phenomenon has been widely studied during the last decades, most of the analysis are based on

assumption valid for specific modulator topologies, and the subsequent analysis can not be applied to different ADC architectures. Another objective of this thesis is the development of an analysis strategy to estimate the influence of clock jitter in continuous-time $\Sigma\Delta$ modulators and oscillator-based modulators.

In summary, the main objectives are:

- To study the feasibility of oscillator-based readout circuits for capacitive MEMS microphones where the sensor is part of the oscillator, making a survey of possible capacitance-controlled oscillators.
- To develop novel high-order oscillator-based $\Sigma\Delta$ modulators suitable for sensor applications, specially for MEMS microphones.
- To implement one or several prototypes in 0.13 μm CMOS technology to demonstrate the feasibility of this approach for MEMS microphones.
- To study the influence of phase noise and distortion in the performance of oscillator-based systems.
- To proposed a methodology to study the influence of clock jitter in continuous-time $\Sigma\Delta$ modulators compatible with oscillator-based implementations.

Structure of this document

This dissertation is organized in four parts:

- Part I: Oscillator-based MEMS microphones.
  - ◇ Chapter 1 provides a compact introduction to sensors, capacitive MEMS microphones, and analog-to-digital conversion techniques.
  - ◇ In Chapter 2 we analyze the feasibility of a microphone where the MEMS sensor is part of the oscillator, in order to modulate the oscillation frequency without the need for a biasing

circuitry. We conclude that this approach is not efficient for this kind of sensors.

- Part II: High-order oscillator-based $\Sigma\Delta$ modulators

  - ◇ Chapter 3 presents an overview of frequency-encoding data converters, including an introduction to phase referenced integration and the state-of-the-art in oscillator-based $\Sigma\Delta$ modulators.
  - ◇ In Chapter 4 we propose architectures and implementation alternatives for high-order single-loop oscillator-based $\Sigma\Delta$ modulators. We focus on second-order low-pass modulators intended for the digitalization of the signals captured by analog MEMS microphones.
  - ◇ Chapter 5 describes the influence of phase noise and distortion in oscillator-based ADCs, and proposes an efficient methodology to estimate the performance of a converter.
  - ◇ Chapter 6 presents a new approach to study the influence of sampling clock jitter in $\Sigma\Delta$ modulators. The proposed method is based on representing the system under analysis in a time-base on which the sampling period is constant. Two examples of how the proposed time-base projection can be applied to different continuous-time $\Sigma\Delta$ modulators are provided.

- Part III: Experimental results

  - ◇ Chapter 7 presents the design and implementation of a second-order oscillator-based $\Sigma\Delta$ converter with multi-bit interstage connections. This modulator is derived from the architectures described in Chapter 4, tailored for audio applications. The resulting chip has also been used to verify part of the derivations presented in Chapter 5.
  - ◇ Chapter 8 shows the design and implementation of a second-order oscillator-based $\Sigma\Delta$ modulator with single-bit interstage connections. This chip is aimed to improve the performance of the design presented in Chapter 7, which did not reach the target performance due to the multi-bit interconnections.

- Part IV: Conclusions
  - ◇ Finally, Chapter 9 draws the conclusions of this thesis and presents potential research activities that may be explored in the future.

  In addition, the description of the main parameters used to evaluate the performance of audio ADCs and sensors can be found in appendix A.

List of publications of the author

Publications connected to this dissertation

Journal papers

- F. Cardes, E. Gutierrez, A. Quintero, C. Buffa, A. Wiesbauer and L. Hernandez, "0.04-mm^2 103-dB-A Dynamic Range Second-Order VCO-Based Audio $\Sigma\Delta$ ADC in 0.13-μm CMOS," accepted for publication in IEEE Journal of Solid-State Circuits.
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- F. Cardes, R. Jevtic, L. Hernandez, A. Wiesbauer, D. Straeussnigg and R. Gaggl, "A MEMS microphone interface based on a CMOS LC oscillator and a digital sigma-delta modulator," 2015 IEEE International Symposium on Circuits and Systems (ISCAS), Lisbon, 2015, pp. 2233-2236.
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Patents

- A. Wiesbauer, D. Straeussnigg, L. Hernandez, and F. Cardes, "System and method for an oversampled data converter," United States Patent 20 140 270 261, Sept. 18, 2014.

Publication not connected to this dissertation

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- E. Gutierrez, L. Hernandez, F. Cardes and P. Rombouts, "A Pulse Frequency Modulation Interpretation of VCOs Enabling VCO-ADC

Architectures with Extended Noise shaping", accepted for presentation at 2018 IEEE International Symposium on Circuits and Systems (ISCAS), Florence.

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- A. Quintero, F. Cardes, L. Hernandez, C. Buffa and A. Wiesbauer, "A Capacitance-to-Digital Converter Based on a Ring Oscillator with Flicker Noise Reduction," 2016 Austrochip Workshop on Microelectronics (Austrochip), Villach, 2016, pp. 40-44.

Part I

Oscillator-based MEMS microphones

CHAPTER 1

Signal acquisition methods for capacitive MEMS microphones

1.1 Introduction

This chapter provides an overview of MEMS microphones and readout circuits for audio applications. Firstly, we present a compact introduction to capacitive sensors and miniaturized microphones, including the description of typical packaging alternatives. Then we describe classical readout strategies and analog-to-digital conversion techniques, with special emphasis on $\Sigma\Delta$ modulators. Basic concept of analog-to-digital conversion such as quantization noise and noise shaping are introduced. Finally, we give an introduction to time-encoding systems and frequency-encoding based $\Sigma\Delta$ modulators.

1.2 Background on MEMS microphones

1.2.1 Capacitive sensors

A sensor is a type of transducer that detects a physical magnitude and transforms it into a different type of signal, typically an electrical signal.

Therefore, a sensor performs the opposite operation of an actuator, which modifies a physical magnitude in function of a control signal. There is a vast variety of sensors designed to measure countless different physical magnitudes. The structure and composition of a sensing element is selected to make an electrically measurable magnitude, such as current, voltages, and resistances, dependent on the measurand.

Capacitive sensors have become very popular in the last years due to its scalability, versatility, and reduced cost and power consumption. A capacitive sensor is typically composed of two or more superposed plates separated by a dielectric material forming a capacitor whose capacitance is measured by a readout circuit. Figure 1.1 describes an ideal parallel plates capacitor, whose capacitance C is:

$$C = \frac{\epsilon_0 \epsilon_r A}{d}, \tag{1.1}$$

where ϵ_0 is the vacuum permittivity, ϵ_r is the relative permittivity of the material between the plates, A is the area of overlap of the two plates, d is the distance between the plates.

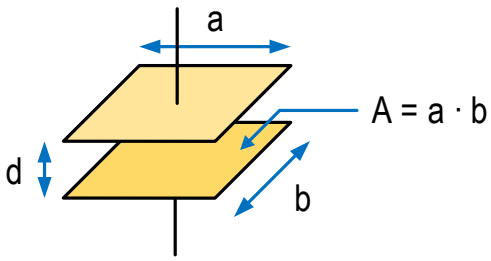


Figure 1.1: Ideal capacitor made of two parallel square plates.

One way to use a capacitor as a sensor is making the overlapped area depend on the measurand. In the sensor shown in Figure 1.2, one of the plates is fixed whereas the second plate is mobile and can be displaced along the horizontal axis. Therefore, the overlapped area (A) and consequently the capacitance depend linearly on the position of the plate.

Figure 1.3(a) describes another capacitive sensor architecture on which the measurand modifies the distance between the plates (d), i.e., the mobile plate can be displace along the vertical axis. In this case, according

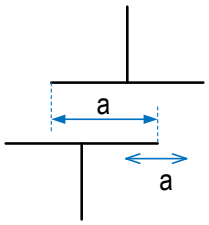


Figure 1.2: Capacitive sensor based on the modification of the overlapped area.

to equation (1.1), the capacitance variation is inversely proportional to the displacement. This single-ended configuration can be transformed into a differential sensor by adding a third plate at the other side of the mobile plate, as shown in Figure 1.3(b). This results in two capacitors, C_p and C_n, which are affected by a vertical displacement ($\Delta d(t)$) of the central plate in opposite ways:

$$C_p(t) = \frac{\epsilon_0 \epsilon_r A}{d_p + \Delta d(t)}, \tag{1.2}$$

$$C_n(t) = \frac{\epsilon_0 \epsilon_r A}{d_n - \Delta d(t)}. \tag{1.3}$$

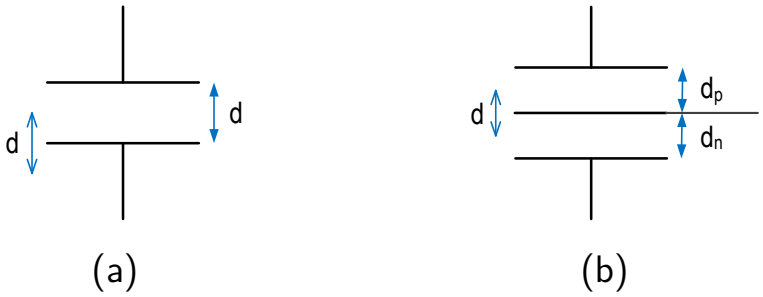


Figure 1.3: Capacitive sensor based on the modification of the distance between the plates. (a) Single-ended sensor. (b) Differential sensor.

1.2.2 Capacitive MEMS microphones

In addition to the reduction of the transistor size, the advances on semiconductor fabrication techniques have allowed the production of minia-

turized electromechanical devices called microelectromechanical systems or MEMS. These new techniques enable the integration of sensing elements, actuators, and other kind of structures in very compact packages. Figure 1.4 shows a photography of a MEMS gear chain close to a mite, courtesy of Sandia National Laboratory.

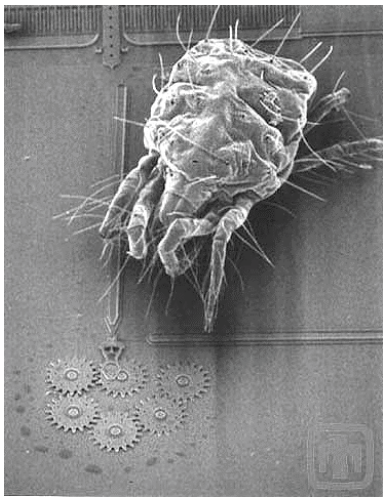


Figure 1.4: A gear chain with a mite approaching. Image courtesy of Sandia National Laboratory (http://www.sandia.gov)

The reduction of the size and cost of these miniaturized devices has been exploited in different applications. In the case of capacitive sensors, MEMS technology has been very relevant in the last years because it allows the development of very compact capacitors with mobile parts, which can be used to measure different physical magnitudes such as acceleration, atmospheric pressure and sound.

Figure 1.5(a) shows the cross section of a flexible membrane that separates two chambers, A and B. When the pressure of the air contained in both chambers is the same ($P_A = P_B$) the membrane stays at rest, since the force applied by the pressurized air of one chamber is counterbalance by the force applied by the air at the other side of the membrane. In contrast, if the pressure of one of the chambers is increased (for example $P_A < P_B$), a net force F_p appears shifting the membrane towards chamber A, as shown in Figure 1.5(b). Assuming that the volume of both chambers is large enough such that the displacement of the membrane has no effect on its pressure, the final position of the membrane is determined by the elastic force F_k that counterbalances F_p, which depends

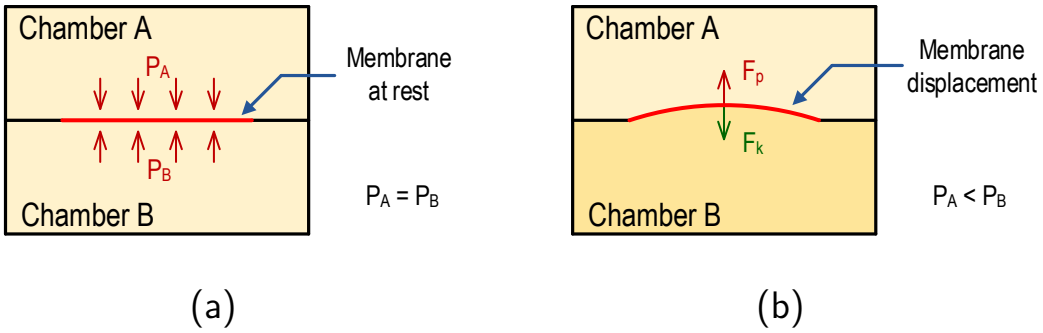


Figure 1.5: Pressure measurement using a flexible membrane. (a) Equilibrium condition. (b) Equilibrium between F_p and F_k for $P_A < P_B$.

on the material properties and construction of the membrane.

This phenomenon can be used to build a capacitive sensor capable of measuring the ambient pressure. One of the chambers is fabricated in silicon and its hermetic. The pressure at one of the sides of the membrane is constant and defined during the fabrication process. The other chamber is opened, and its pressure is equal to the atmospheric pressure. In consequence, a change in the ambient pressure causes a displacement of the membrane. A stiff backplate (typically perforated to enable the air flow) can be attached as a parallel membrane to build a two-plate variable capacitor whose capacitance variation is inversely proportional to the variation of the relationship between the ambient and the reference pressures.

This structure can be optimized for sound sensing by means of two minor variations. On one hand, the mechanical properties of the membrane must be carefully chosen to achieve the desired flat frequency response of membrane displacement for acoustic input at frequencies in the whole audio band (typically from 20 Hz to 20 kHz). On the other hand, slow pressure variations (typically caused by altitude or meteorological condition changes) must be rejected by the sensor in order to achieve uniform polarization conditions over time. This can be done by adding small holes to the membrane that enable slow air flows to balance the average pressure inside and outside of the reference chamber without allowing fast flows that would reduce the sensitivity of the sensor in the audio band.

Figure 1.6 shows the cross section of two commonly used MEMS microphone configuration [1]. Figure 1.6(a) is a single backplate (SBP) MEMS, which is the topology explained in the previous paragraphs and corresponds to the single-ended capacitive sensor depicted in Fig. 1.3(a). Conversely, Figure 1.6(b) shows a dual backplate (DBP) MEMS microphone, which is the result of adding a second backplate at the opposite side of the membrane, so it operates as the differential capacitive sensor described in Fig. 1.3(b).

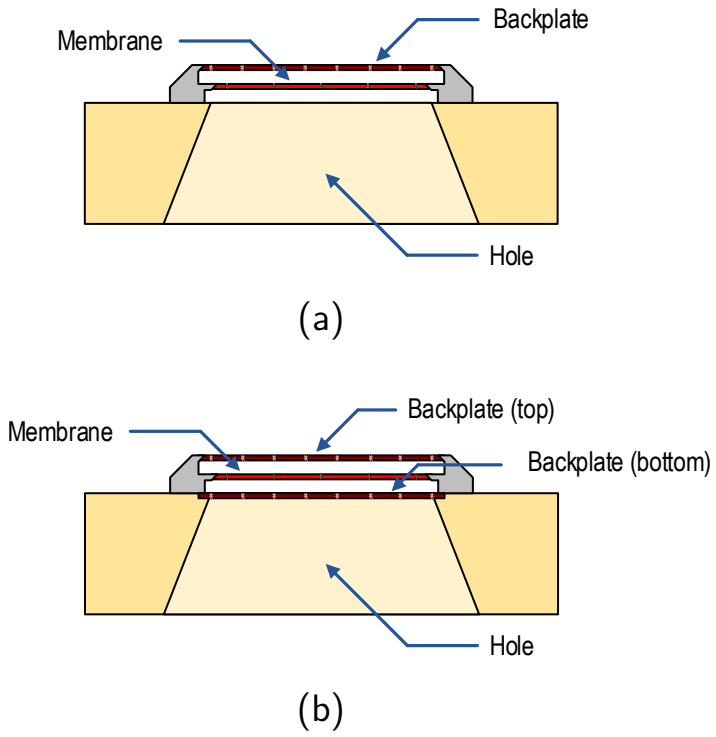


Figure 1.6: Construction of MEMS microphones combining stiff backplates with a semipermeable flexible membrane. (a) Single backplate structure . (b) Dual backplate structure.

There are two different trends in the fabrication of MEMS microphones: analog and digital outputs. In some cases, the company that integrates the microphone in the end product (e.g., a smartphone or wearable manufacturer) prefers a sensor that provides an analog signal. In this case, the signal digitalization can be tailored to the product needs in a separate codec chip. On the other hand, other manufacturers prefer sensors that integrate the ADC in the same package. Nowadays, the

market size of analog microphones is considerably larger that the market of digital microphones, although the latter have gained popularity during the last years.

Figure 1.7(a) depicts the typical block diagram of an analog microphone. The microphonic capsule (a capacitive MEMS in our case) is followed by a readout circuit that generates a voltage proportional to the sound pressure. An example of a commonly used readout circuit will be provided in Section 1.2.3. In addition to the circuits in the signal path, power management and auxiliary subsystems are typically required for the proper operation of the microphone.

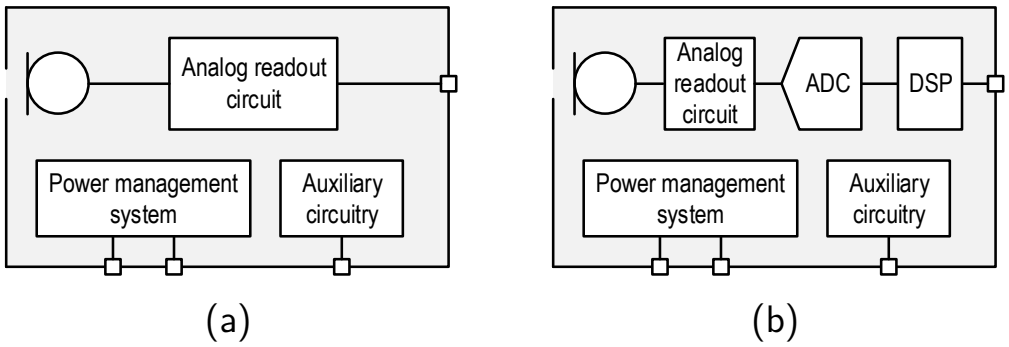


Figure 1.7: Typical block diagram of commercial MEMS microphones. (a) Analog microphone. (b) Digital microphone.

Digital microphones also require an ADC to digitize the analog signal, as shown in Figure 1.7(b). Moreover, the output of the ADC may require some kind of digital post-processing, such as decimation or filtering. The specifications for the output signal differ from one manufacturer to other since the there are several commonly used data rates and communication protocols. Furthermore, digital microphones incorporate different operation modes with varying bandwidths, resolutions and power consumptions [2, 3].

The manufacturing processes used in the fabrication of the MEMS are generally not compatible with the CMOS processes required to fabricate the electronics, and two different dies must be independently bonded together inside the package. Figure 1.8(a) shows the cross section of an example of the integration of a MEMS and the readout ASIC inside

an acoustic package. In this example, the hole that allows the contact between the membrane and the atmosphere is at the bottom of the package, and requires another hole in the printed circuit board (PCB). Therefore, the reference pressure is determined by the pressure of the air contained inside the package. An alternative packaging is shown in Figure 1.8(b), where the hole is in the lid of the package and the reference pressure is determined by the air trapped between the membrane and the bottom of the package.

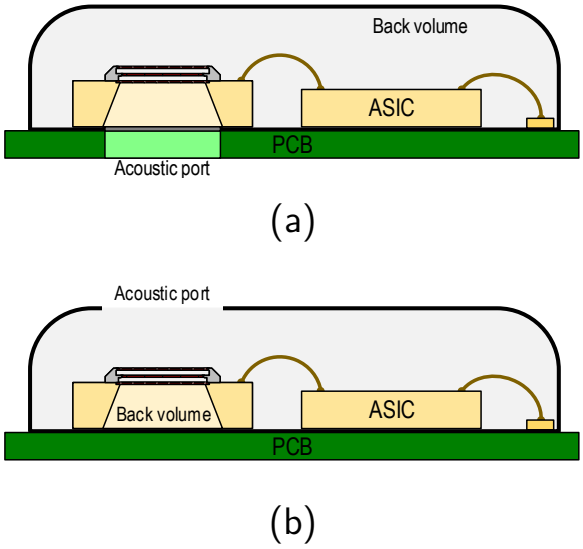


Figure 1.8: MEMS microphone and readout ASIC inside an acoustic package. (a) Acoustic port at the bottom of the package (and PCB). (b) Acoustic port at the lid of the package.

1.2.3 Classical MEMS microphone readout circuits

One of the most common circuits to generate a voltage proportional to the acoustic signal is based on biasing the MEMS capacitor through a very high-ohmic resistor [4, 5], as shown in Figure 1.9. In the absence of sound, membrane and backplate are separated by the nominal distance (d), and the MEMS is at its nominal capacitance (C_0):

$$C_{MEMS}(t) = \frac{\epsilon_0 \epsilon_r A}{d} = C_0. \tag{1.4}$$

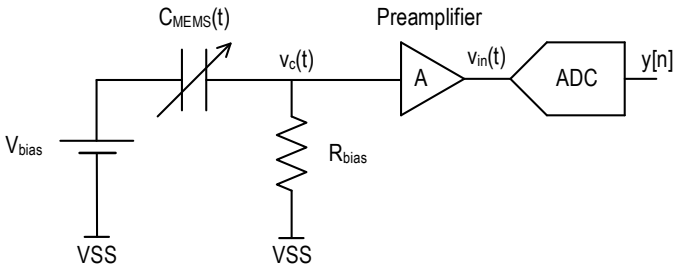


Figure 1.9: Simplified diagram of a typical readout circuit for digital MEMS microphones.

The amount of electric charge stored in the MEMS is

$$Q_{MEMS}(t) = V_{MEMS} \cdot C_{MEMS}(t), \tag{1.5}$$

which in steady state (i.e., $v_c(t) = 0$ and $C_{MEMS}(t) = C_0$) is almost equal to

$$Q_{MEMS}(t) \approx V_{bias} \cdot C_0 = Q_0. \tag{1.6}$$

In presence of sound, the distance between membrane and backplate is modulated by pressure variation, so the MEMS capacitance is

$$C_{MEMS}(t) = \frac{\epsilon_0 \epsilon_r A}{d + \Delta d(t)}. \tag{1.7}$$

Despite this change in the capacitance, the charge stored in the MEMS is in practice constant if the high-ohmic biasing resistor is large enough to prevent any significant current to flow. Assuming that this condition is met, the voltage $v_c(t)$ can be expressed as:

$$v_c(t) = V_{bias} - V_{MEMS} \approx V_{bias} - \frac{Q_0}{C_{MEMS}(t)} = V_{bias}\frac{-\Delta d(t)}{d}. \tag{1.8}$$

Given that the sensitivity of this readout circuit is proportional to the biasing voltage, V_{bias} is typically higher than common supply voltages, in the range from 3 V to 8 V. In order to minimize current leakage through the biasing resistor, R_{bias} is in the range of several gigaohms. Nevertheless, some variations on the MEMS charge are unavoidable for

large sound pressure levels. Figure 1.10 shows the system architecture of a real implementation in 0.13 μm CMOS technology recently published in [5], on which a differential MEMS is read out using a high-voltage and high-ohmic biasing circuit similar to the one described in this section. Note that due to the long time constants involved in this circuit, the noise generate by the biasing resistor is mostly concentrated at very low frequencies, on which noise power is attenuated by A-weighting (see appendix A).

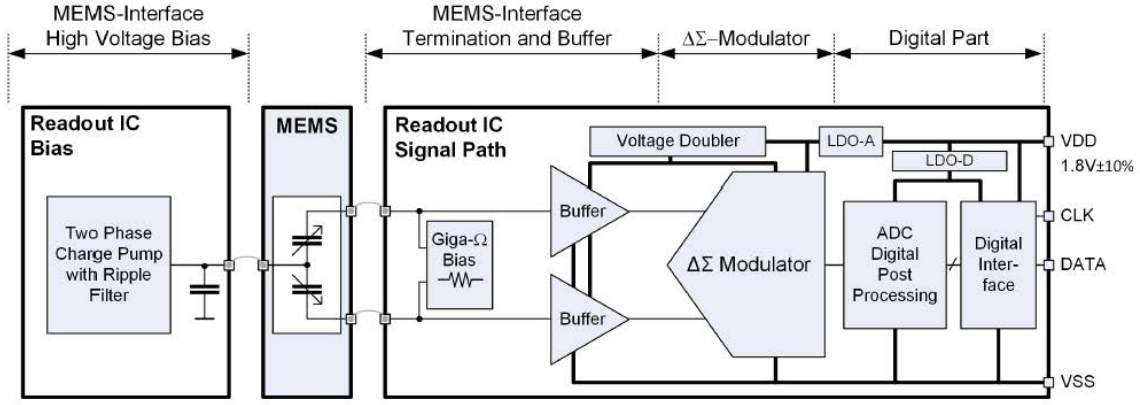


Figure 1.10: System architecture of the digital microphone reported in [5] (©2017 IEEE).

1.3 Background on analog-to-digital converters

Analog to digital converters serve as a bridge between the analog representation of the physical magnitudes that surround us and the digital systems that we want to use to process, store, and transmit these information. Figure 1.11 illustrates the analog to digital conversion process, on which an analog signal is discretized in time (sampled) and in amplitude (quantized) to obtain a digital signal.

On one hand, the requirements for the sampling process depend on the properties of the analog signal. According to the Nyquist-Shannon sampling theorem [6, 7], a continuous-time signal whose spectral components are below a frequency BW can be sampled without loss of informa-

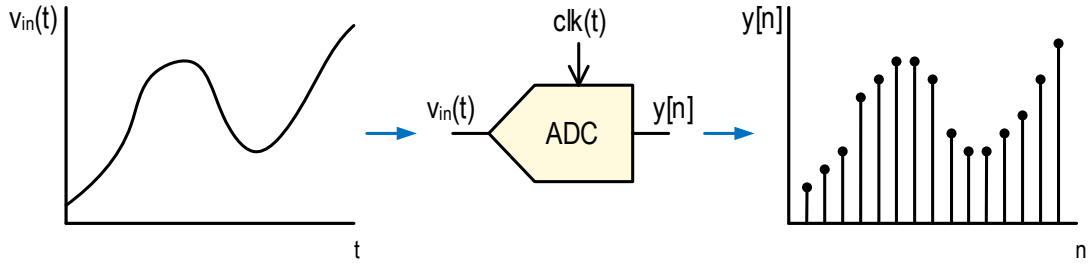


Figure 1.11: Analog-to-Digital conversion process.

tion using a constant sampling rate equal to $2BW$ (or higher). On the other hand, the power of the errors introduced during the quantization process depends on the quantization step, which is related to the range and number of bits of the quantizer. Moreover, the sampling frequency also influences the spectral distribution of these quantization errors. The signal to noise ratio (SNR) of the converter is determined by the noise power inside the band of interest, since it is assumed that noise out of this band is filtered afterwards.

There is a wide variety of ADC architectures, which can be divided into Nyquist-rate and oversampled converters depending on the sampling frequency used. Nyquist-rate ADCs are based on using a sampling frequency equal to or slightly higher than the minimum frequency required to meet the Nyquist-Shannon criterion. Conversely, in oversampled data converters the sampling frequency used is well above the Nyquist frequency. The oversampling ratio (OSR) is defined as the ratio between the actual sampling frequency and the Nyquist sampling rate:

$$OSR = \frac{f_S}{2BW}. \tag{1.9}$$

The main benefit of oversampling is that quantization noise is spread out a wider range of frequencies. Assuming that its spectral distribution is nearly flat and the total power is independent of the sampling frequency, increasing the oversampling ratio decreases the power spectral density of the noise, what reduces the total noise power present in the band of interest. Moreover, some ADC architectures allow the modulation of quantization error, shaping its spectral distribution and decreasing the power inside the band of interest at the expense of increasing the

noise power at other regions of the Nyquist bandwidth. This technique is called "noise shaping" and is characteristic of ΣΔ modulators.

1.3.1 Sigma-Delta modulators

As mentioned above, ΣΔ data converters are very popular for low-bandwidth high-resolution applications due to their noise shaping properties [8]. Figure 1.12(a) depicts a generic single-stage ΣΔ modulator which consists of a loop filter, a quantizer, and a sampler. Figure 1.12(b) describes a linear equivalent of this system on which the quantizer has been replaced by an adder that injects the quantization error signal $e_q(t)$. The influence of this error in the output $y[n]$ is determined by the noise transfer function (NTF), which depends on the loop filter architecture. An optimum NTF minimizes the noise power inside the band of interest without compromising other properties such us system stability or insensitivity to clock jitter. On the other hand, the signal transfer function (STF) describes the influence of the input signal $v_{in}(t)$ in the output of the system. Figure 1.12(c) illustrates NTF examples for low-pass ΣΔ modulators of different orders. Although high-order loop filters are more complex and may suffer from stability problems, they achieve lower the noise power inside the band of interest.

Figure 1.13 depicts the simplified block diagram of two continuous-time (CT) ΣΔ modulators. Fig. 1.13(a) shows a first-order CT-ΣΔM on which the loop filter is an integrator. The maximum signal to quantization noise (SQNR) of a first-order low-pass ΣΔ modulator can be estimated using the following expression [9]:

$$SQNR_{max} \approx 6.02 \cdot N + 1.76 - 5.17 + 30 \log_{10}(OSR), \tag{1.10}$$

where N is the full-scale number of bits. On the other hand, the modulator represented in Fig. 1.13(b) achieves second-order noise shaping due to the second-order filter loop. In consequence, the maximum SQNR is theoretically:

$$SQNR_{max} \approx 6.02 \cdot N + 1.76 - 12.9 + 50 \log_{10}(OSR). \tag{1.11}$$

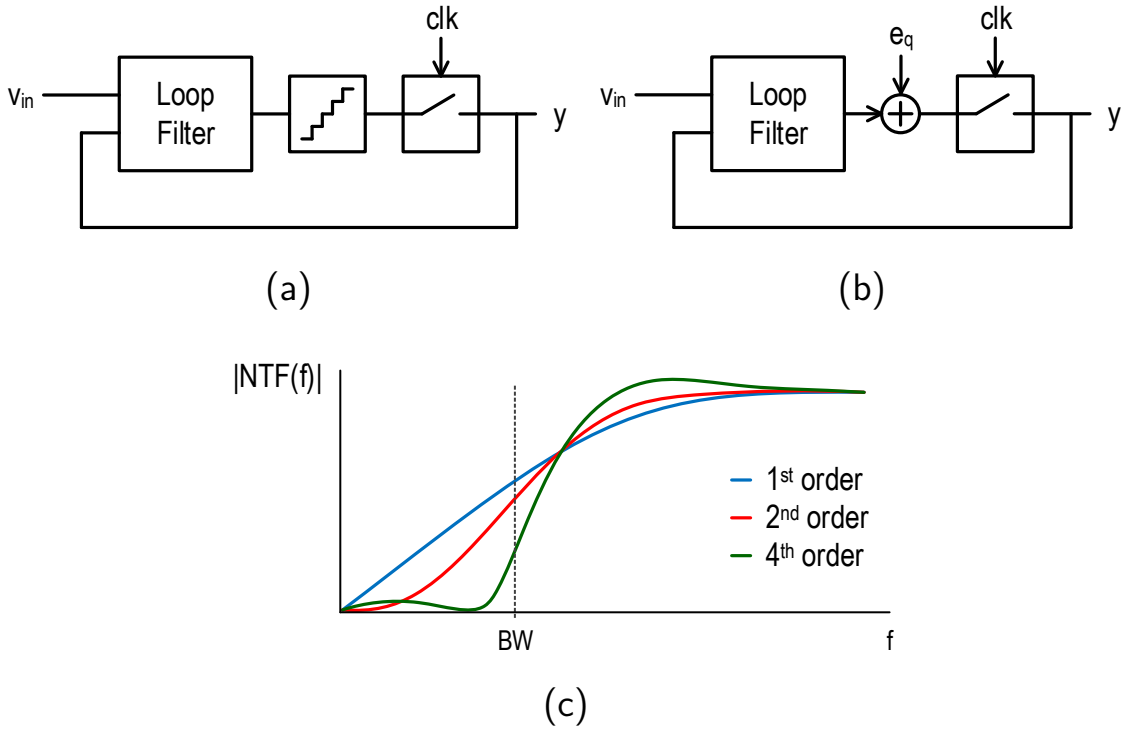


Figure 1.12: (a) Generic single-stage ΣΔ modulator. (b) Linearization of the quantization process modeled as the addition of quantization noise (e_q). (c) Example of different NTFs for low-pass ΣΔ modulators.

Other modulator topologies can be implemented combining different number of integrators and different feedback and feedforward connections [10].

Alternatively, high-order noise shaping can be achieved using a multi-stage noise shaping (MASH) configuration, as shown in Fig. 1.14. In this case, the error of the first stage (E_1) is feed into the second stage for its digitalization. Finally, the output of both stages are combined through noise cancellation filters (NCFs). The output of the second stage cancels the noise of the first stage and, in consequence, the output of the modulator shows second-order noise shaping.

For any of these topologies, two additional subsystems are commonly required to obtain a functional ADC. On one hand, an antialiasing filter is typically required at the input of the modulator to remove the high-frequency components that may fall inside band of interest after after sampling due to aliasing. On the other hand, a digital signal processing

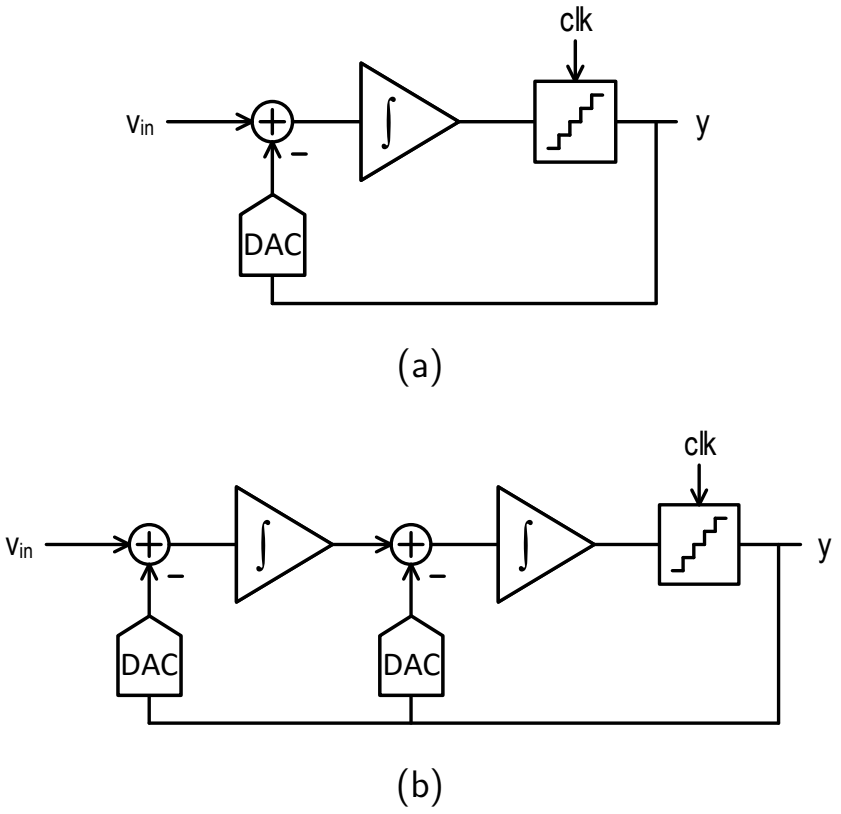


Figure 1.13: (a) First-order ΣΔ modulator. (b) Second-order ΣΔ modulator.

subsystem is frequently used to remove the noise out of the band and sometimes also to perform the decimation.

Two different approaches can be taken to implement ΣΔ modulators: discrete-time (DT) and continuous-time. DTΣΔ converters are typically implemented using switched-capacitors (SC) circuits, which operate transferring charges between different capacitors synchronized by signals synthesized from the sampling clock. In this kind of systems combine good accuracy, linearity, and are tolerant to clock jitter. However, switched-capacitor circuits require high-speed DACs and operational amplifiers, what increases the power consumption of the system. On the other hand, the operation of CTΣΔ is not based on switching elements and thus the power consumption is potentially lower. Moreover, given that sampling is performed after the loop filter (in contrast to what happens in SC-based modulators), the loop filter itself can work as antialiasing filter, eliminating the need for a dedicated filter.

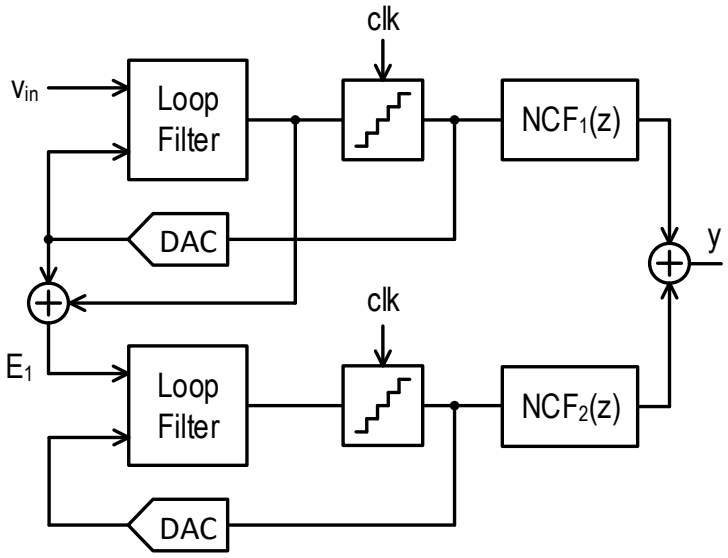


Figure 1.14: Multi-stage $\Sigma\Delta$ modulator.

1.3.2 Time-encoding based ADCs

The evolution of the semiconductor industry has allowed the reduction of the minimum MOS transistor size during the last decades [11]. The scaling of the CMOS technology has important advantages for digital circuits such as the reduction of the silicon area, the power consumption, and the increase in the operation frequency. In contrast, the performance of analog circuitry is sometimes negatively affected by this trend which reduces transistor gains and the voltage headroom available for stacking transistors. Therefore, some circuit architectures commonly used in the past are becoming more difficult to implement [12–14].

Time-encoding is an emergent alternative to the traditional voltage (or current) encoding. Time-encoding is based on using the input signal to modulate a timing property (such as the frequency, duty cycle, delay, etc.) of a carrier signal. One of the benefits of time-encoding systems is that they can be implemented using mostly-digital circuitry which is benefited from technology scaling.

One of the time-encoding techniques most popular to implement data converter is frequency-encoding, on which the input signal is encoded into the frequency of a carrier signal [15–17]. Figure 1.15 depicts a generic frequency-encoding based data converter, which consists of a

frequency-encoder connected to a frequency-to-digital (F2D) converter. Assuming that the input signal is a voltage, the frequency-encoder would be a voltage-to-frequency converter, which can be implemented using a voltage-controlled oscillator (VCO). Note that other alternatives like current-controlled oscillators (CCOs) or reactance-controlled oscillators are also valid frequency-encoders if the input signal is respectively a current or the value of a reactance. However, in this section we will take a VCO as case study for the sack of simplicity.

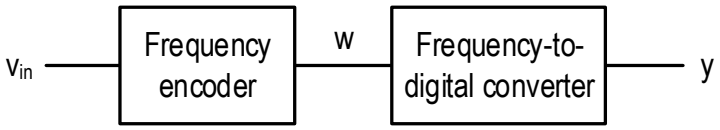


Figure 1.15: Generic frequency-encoding based data converter.

During the last years, several VCO-based ADCs have been published for different applications [17–23]. Figure 1.16 shows the simplified block diagram of one of the most commonly used VCO-based ADC architectures. In short, the input voltage modulates the frequency of a VCO whose output, which can be single-bit or multi-bit, is connected to a F2D converter, which consists of a counter, a sampler, and a digital first-difference ($1\text{-}z^{-1}$). The value of the counter is increased in one unit each time it receives a rising edge from the VCO. In consequence, the output of the F2D converter represents the number of oscillations that have occurred during the last sampling period. This value is proportional to the oscillation frequency, and therefore is also proportional to the input voltage.

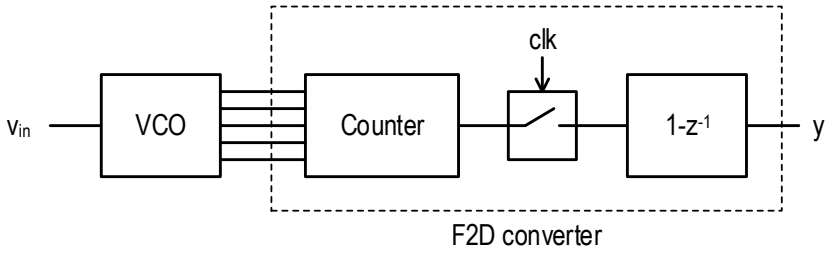


Figure 1.16: Simplified diagram of a VCO-based ADC.

Figure 1.17 shows the system of Fig.1.16 represented using the linear model of a VCO, which can be studied as a phase integrator. The VCO

gain is K_{VCO}, which describes the relationship between the input voltage variation and the oscillation frequency deviation. This model adds two errors after the integration: phase noise and phase quantization error. Phase noise is the random phase fluctuation due to electrical noise in the circuit, which will be explained in details in Chapter 5. Phase quantization error appears due to the fact that the F2D converter has limited information about the VCO phase (the counter only detects oscillation edges), and it is the time-encoding equivalent of the quantization error present in classical ΣΔ modulators. As shown in Fig. 1.17, both error sources are high-pass filtered by the digital first-difference.

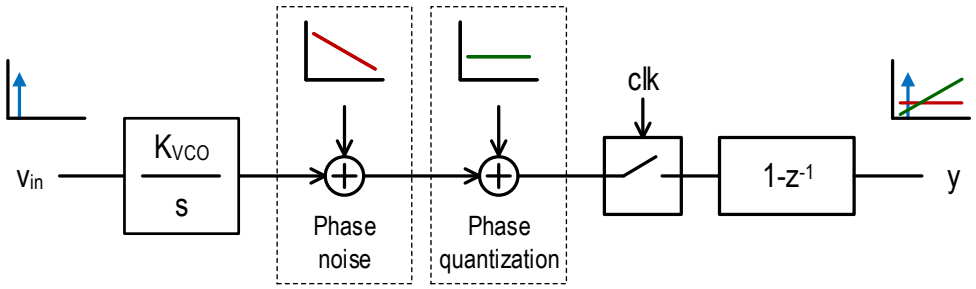


Figure 1.17: Linearized equivalent of the first-order VCO-based ADC of Fig. 1.16.

Therefore, assuming that the power spectral density of phase quantization noise is white, the output spectrum shows first-order noise-shaping, similar to a classical first-order ΣΔ modulator. Indeed, the maximum SQNR of first-order oscillator-based converters can be estimated using a similar approach:

$$SQNR_{max} \approx 20\log_{10}\left(\frac{2 \cdot K_{VCO} \cdot v_{in\text{-}FS}}{f_s}\right) + \tag{1.12}$$

$$+ 1.76 - 5.17 + 30\log_{10}\left(OSR\right), \tag{1.13}$$

where $v_{in\text{-}FS}$ is the full-scale input peak and therefore $2 \cdot K_{VCO} \cdot v_{in\text{-}FS}$ is the peak-to-peak full-scale oscillation frequency variation. This expression is only accurate when quantization noise is white, which is not necessary true in oscillator-based modulators. The equivalence between

a VCO-ADC and a $\Sigma\Delta$ modulator will be studied in-depth in Chapter 3. In addition, Chapter 4 will describe a novel high-order single-stage oscillator-based $\Sigma\Delta$ modulator.

CHAPTER 2

Design of oscillator-based capacitive MEMS microphones readout circuits

2.1 Introduction

As mentioned in 1.2.3, one of the most frequent ways to acquire an acoustic signal using a capacitive MEMS microphone is biasing the sensor with a high voltage to generate a voltage signal that can be digitalized by an ADC, as shown in Figure 1.10. This approach has two disadvantages: on one hand, it requires a high-voltage generator which increases the power consumption and area of the system; on the other hand, it can not be interfaced with some CMOS technologies due to the high voltage levels required. In this chapter we study the feasibility of the alternative approach presented in Figure 2.1(b), which is based on using the MEMS as part of the oscillator time constants in order to make the oscillation frequency dependent on the MEMS capacitance. Therefore, the oscillation $w(t)$ can be processed by a frequency to digital converter as is done in VCO-based ADCs to estimate the sound pressure level.

In this chapter we discuss several aspects of this kind of architec-

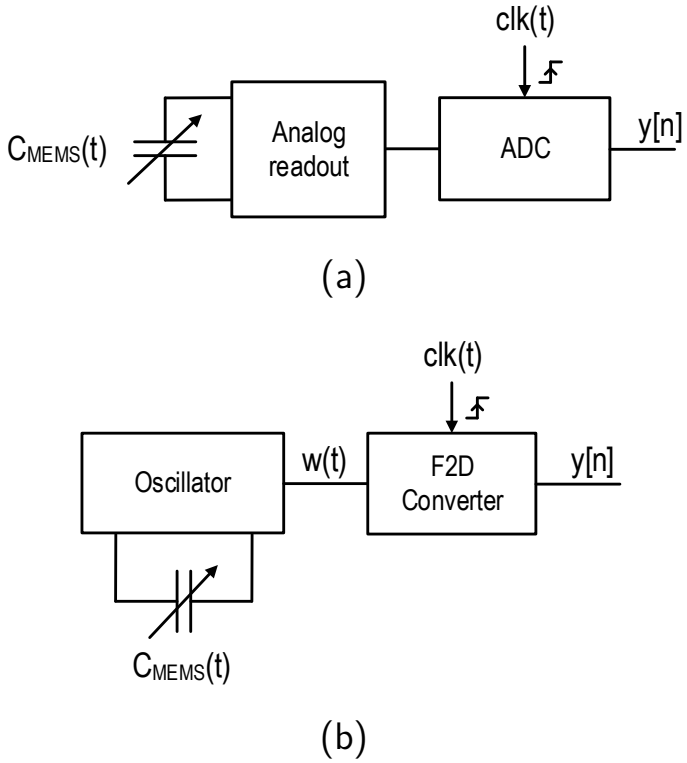


Figure 2.1: (a) Classical capacitive sensor readout circuit. (b) Capacitance-controlled oscillator based sensor readout circuit.

tures. Firstly, we describe MEMS microphones including examples of the parasitic effects that are typically present in the structure and in the interconnection with the ASIC, which must be considered during the integration of the MEMS in the oscillator. After that, an oscillator-based readout circuit is described. Finally, we analyze different oscillator topologies that may be suitable for this kind of readout circuits, including inductor-less and LC oscillators. The discussion presented in this chapter have been partially published in [24, 25]

2.2 Preliminary considerations about the MEMS-ASIC interconnection

This section provides an overview of some of the parasitic effects that may influence the performance of the oscillator-based readout circuit, including SBP and DBP MEMS microphones, and also the parasitics

derived from the bonding wires and pads required to connect the MEMS with the readout ASIC.

2.2.1 Single backplate MEMS

As explained in Section 1.2.2, an SBP MEMS microphone comprises a porous backplate placed on top of a membrane that separates the environment (whose pressure changes in presence of sound) and a reference chamber (whose pressure is equal to the average of the ambient pressure). The microphone typically has three pads: the membrane (MEM), the backplate (BP), and the substrate (SUB). Table 2.1 shows an example of the dimensions that this kind of MEMS typically have.

Table 2.1: Example of SBP MEMS microphone dimensions.

Parameter	Value
C_{MEMS} at rest	2.5 pF
Membrane diameter	1 mm
Membrane - backplate distance at rest	2.5 μm
Full-scale membrane variation (120 dB_{SPL})	$\pm$200 nm
Membrane variation at 1 Pa (94 dB_{SPL})	$\pm$10 nm

Ideally, this structure is equivalent to a capacitor whose capacitance variation is proportional to the sound pressure variations:

$$C_{MEMS}(t) = \frac{\epsilon_0 \epsilon_r A}{d_p + \Delta d(t)}. \tag{2.1}$$

However, there are several undesired effects that deviate the electromechanical behavior of the MEMS from a simple capacitor. Firstly, both membrane and backplate are fabricated using poly silicon, whose resistivity is not negligible. Figure 2.2 shows how the MEMS capacitor can be split into infinitesimal capacitors connected to each other by resistors. Therefore, the equivalent series resistance of each infinitesimal capacitor depends on its location respect to the metallic contact that connects the plate to the MEMS pad. Furthermore, not all the capacitors change in the same proportion for a given sound pressure variation

because the membrane is bonded to the substrate along its perimeter. Therefore, the capacitors associated to regions of the membrane close to the center of the MEMS are more sensitive to sound.

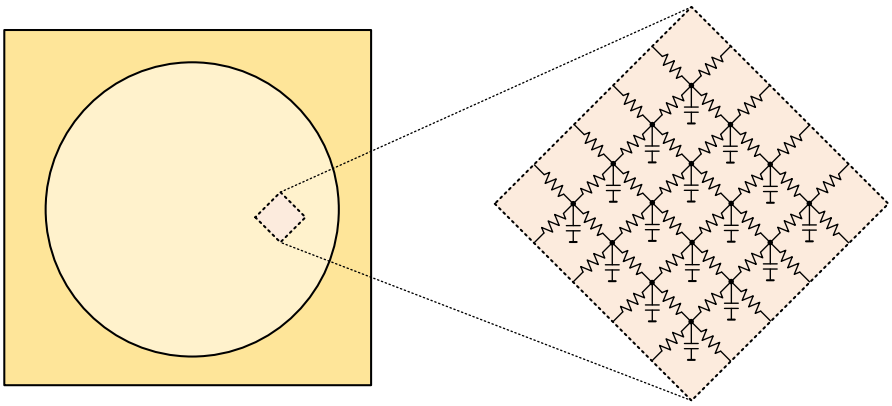


Figure 2.2: Distributed model of the membrane-backplate structure.

Although there are simulation models that take into account all these effects, an SBP MEMS microphone can be described electrically by the simplified diagram shown in Figure 2.3. The core of the sensor is the capacitance C_{MEMS}, which corresponds to the capacitor formed by the overlap of the membrane and the backplate and follows equation (2.1). R_{MEM} and R_{BP} are respectively the equivalent parasitic resistance of the membrane and backplate. R_{leak} is a parasitic resistance that bypasses $C_{MEM\text{-}BP}$, although its value is typically in the range of several GΩ and can be neglected in most of the cases. Finally, C_{mb}, C_{bs}, and C_{ms}, are parasitic capacitors between membrane, backplate, and substrate.

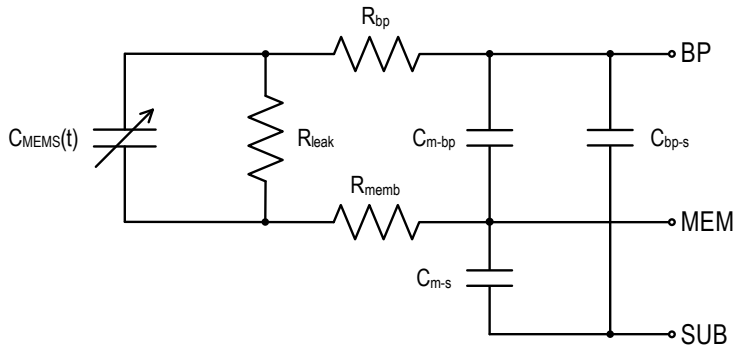


Figure 2.3: Simplified electrical model of the single backplate MEMS.

Table 2.2: Example of SBP MEMS parasitics values.

Parameter	Value	Parameter	Value
R_{leak}	> 1 GΩ	$C_{m\text{-}bp}$	200 fF
R_{memb}	600 Ω	$C_{bp\text{-}s}$	200 fF
R_{bp}	400 Ω	$C_{m\text{-}s}$	> 3 pF

2.2.2 Dual backplate MEMS

A dual backplate MEMS has many similarities with the SBP described before. In the DBP MEMS, the membrane (MEM) is enclosed by two backplates, one in the upper side (TOP) and the other one in the lower side (BOT), as shown in Figure 1.6(b). This structure comprises two capacitors with opposite reactions to sound pressure variations, which can be used to build differential circuits.

The simplified electrical model of the DBP microphone is depicted in Figure 2.4. In addition to the parasitics already described in Section 2.2.1, we can observe that the membrane resistance (R_{MEM}) is common to both capacitors. This may be a source of interferences between both sides of the differential system, because a current from TOP to MEM induces a voltage variation between MEM and BOT.

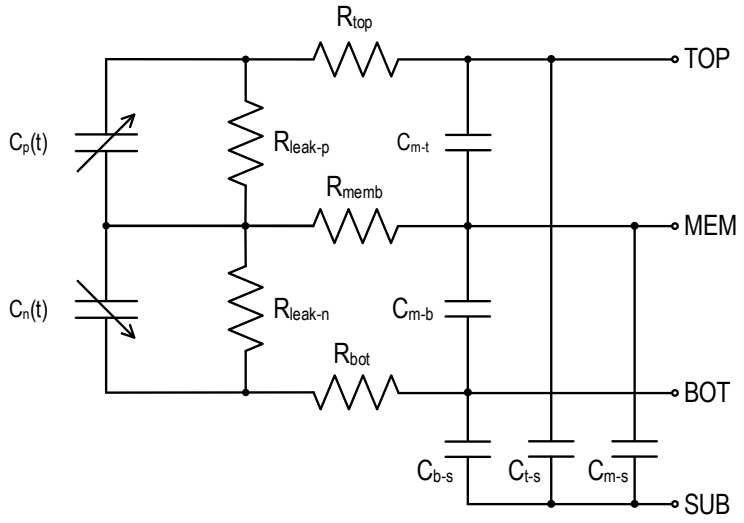


Figure 2.4: Simplified electrical model of the dual backplate MEMS.

Table 2.3: Example of DBP MEMS parasitics values.

Parameter	Value	Parameter	Value
$R_{leak\text{-}p}$	> 1 GΩ	$C_{m\text{-}t}$	200 fF
$R_{leak\text{-}n}$	> 1 GΩ	$C_{m\text{-}b}$	200 fF
R_{memb}	600 Ω	$C_{b\text{-}s}$	> 200 fF
R_{top}	400 Ω	$C_{t\text{-}s}$	200 fF
R_{bot}	400 Ω	$C_{m\text{-}s}$	> 3 pF

2.2.3 Bonding wires

These MEMS microphones require fabrication processes that are not compatible with the standard processes employed to manufacture the transistors of the readout circuit. Therefore, the MEMS and the circuit are hosted in two different silicon dies, and they are connected together through bonding wires, as illustrated in Figure 2.5.

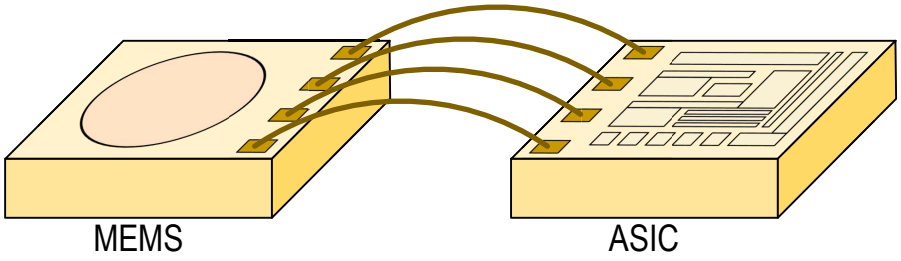


Figure 2.5: Connection between the MEMS and the readout ASIC.

Figure 2.6 shows a simplified electrical model of the bonding. R_{wire} and L_{wire} are respectively the resistance and the inductance of the bonding wire. $C_{pad\text{-}MEMS}$ is the parasitic capacitor formed between the MEMS pad and the MEMS substrate. Similarly, $C_{pad\text{-}ASIC}$ is the parasitic capacitor of the pad on the readout circuit silicon die.

Table 2.4 shows an example of the value of these parasitics, although these values may be completely different depending on fabrication and packaging details.

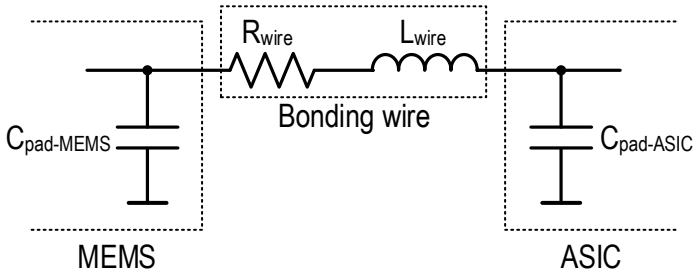


Figure 2.6: Bonding parasitics model.

Table 2.4: Example of bonding parasitics.

Parameter	Value
$C_{\text{pad-MEMS}}$	500 fF
$C_{\text{pad-ASIC}}$	500 fF
R_{wire}	0.1 Ω
L_{wire}	1 nH

2.3 System architecture

In this section we describe the architecture of an oscillator-based readout circuit low-cost MEMS microphones. Table 2.5 summarizes the specifications considered as the reference for the system-level design. More information about the meaning of these parameters can be found in appendix A.

Equation (1.12) can be rewritten as follows:

$$SQNR_{max} \approx 20\log_{10}\left(\frac{\Delta f_{max}}{f_s}\right) + \tag{2.2}$$

$$+ 1.76 - 5.17 + 30\log_{10}\left(\frac{f_s}{2 \cdot BW}\right), \tag{2.3}$$

where Δf_{max} represents the full-scale oscillation frequency variation. Although this expression is not accurate due to the non-white phase quantization noise (see Section 3.2.2 for more details), it is valid to estimate the order of magnitude of different system level parameters required to meet the specifications. For example, taking as target 96 dB of SQNR_{max} (for simplicity we do not consider A-weighting for this estimation), from

equation (2.2) we derive

$$\Delta f_{max} \cdot \sqrt{f_s} > 7.5 \cdot 10^{11} Hz^{3/2}. \tag{2.4}$$

Table 2.5: Target specifications for the target low-cost MEMS microphone.

Parameter	Value
$\text{SNDR}_{\text{peak}}$	$>$ 68 dB-A
SNDR @ 94 dB_{SPL}	$>$ 68 dB-A
SNDR @ AOP	40 dB-A
AOP	120 dB_{SPL}
DR	96 dB-A
BW	20 kHz
Sampling frequency	2.54 MHz
Digital word length	1 bit
Power	$<$ 1 mW
Supply voltage	$\leq$ 1.8 V

Given the small full-scale capacitance variation that MEMS microphones show (see Table 2.1), the frequency variation of the capacitance-controlled oscillator is considerably smaller than its nominal oscillation frequency. Using the target sampling frequency of 2.54 MHz is not an option because it would require an oscillation frequency of several GHz, which is not feasible. Therefore, both the center oscillation frequency and the sampling frequency should be in the order of hundreds of MHz in order to satisfy (2.4). Furthermore, if the sampling frequency is higher than twice the maximum oscillation frequency, the readout circuit can be implemented using the F2D converter shown in Figure 2.8, which has been widely used in the past due to its simplicity and efficiency [21,26,27].

In order to meet the interface specifications listed in Table 2.5 (i.e., single-bit output and 2.54 Mbps), the F2D output must be connected to a digital signal processing (DSP) block formed by a decimator and a noise shaper, as shown in Figure 2.8.

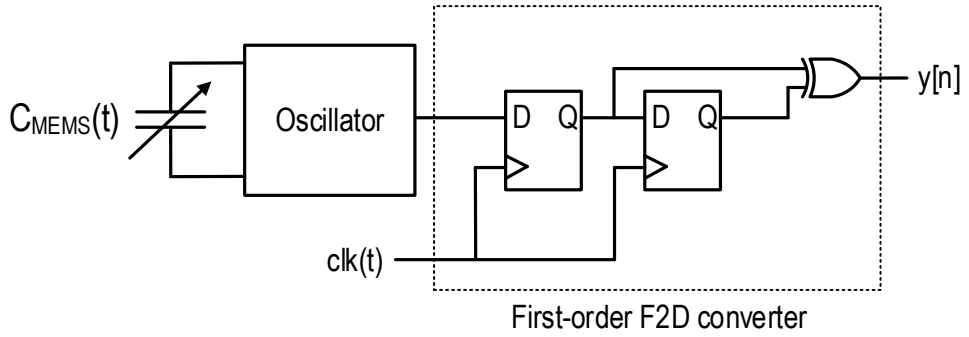


Figure 2.7: Proposed oscillator-based readout circuit with XOR-based F2D converter.

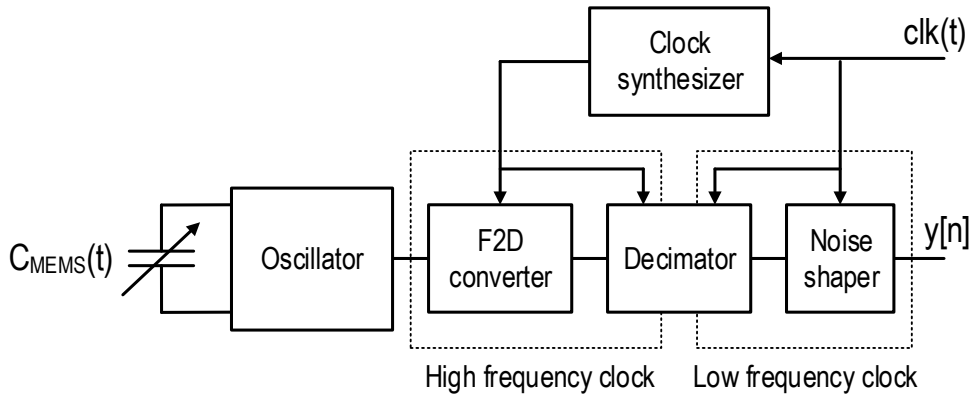


Figure 2.8: Architecture of the system with high effective sampling frequency.

Alternatively, a high-order oscillator-based $\Sigma\Delta$ modulator can be built connecting the capacitance-controlled oscillator to a more complex F2D converter, which may be composed of several oscillators or analog integrators, as will be discussed in Chapter 4. This approach would reduce the minimum center oscillation frequency and sampling frequency and eventually would eliminate the need for the DSP subsystem.

Regardless of the modulator order and the architecture of the F2D converter used, the accuracy of the capacitance-to-frequency conversion process may limit the performance of the oscillator-based MEMS sensor readout circuit. Chapter 5 provides more details about the origins and the consequences of phase noise and distortion.

2.4 Oscillator topology

This section discusses the suitability of four oscillator topologies to be used in capacitance-controlled oscillators for sensor readout circuits. We describe three inductor-less oscillators: ring oscillators, I-C relaxation oscillators, and source-coupled multivibrators. These topologies are interesting because they do not require integrated inductors, which are costly in terms of area. In contrast, LC oscillators need an integrated coil, but they show much lower phase noise [28].

2.4.1 Inductor-less oscillators

Ring oscillator

Ring oscillators are commonly used in several applications such as frequency synthesizers [29], wafer testing [30], data conversion [27], and sensor applications [31–33]. A ring oscillator consists of an odd number of inverting stages (and optionally some non-inverting stages, although we will not consider this option for simplicity) connected on a ring configuration. The oscillation period is proportional to the number of stages and the delay introduced by each stage. These delays depend on the capacitive loads connected between stages and other circuit parameters. Although some guidelines to achieve the target oscillation frequency and phase noise can be found in the literature [34, 35], the design process is typically empirical. Figure 2.9 shows two examples of delay stage architectures: single-ended and differential. The single-ended delay (Figure 2.9(a)) is typically better in terms of power consumption and phase noise, whereas the differential implementation (Figure 2.9(b)) is less sensitive to interferences and supply noise [36].

A capacitance-controlled oscillator can be built using an SBP MEMS as the load of some stages of the ring oscillator. In absence of parasitics, both architectures would be suitable for connecting the MEMS as a capacitive load at the output of one stage: in the differential implementation the MEMS would be connected between both sides of the differential output, whereas in the single ended topology the MEMS

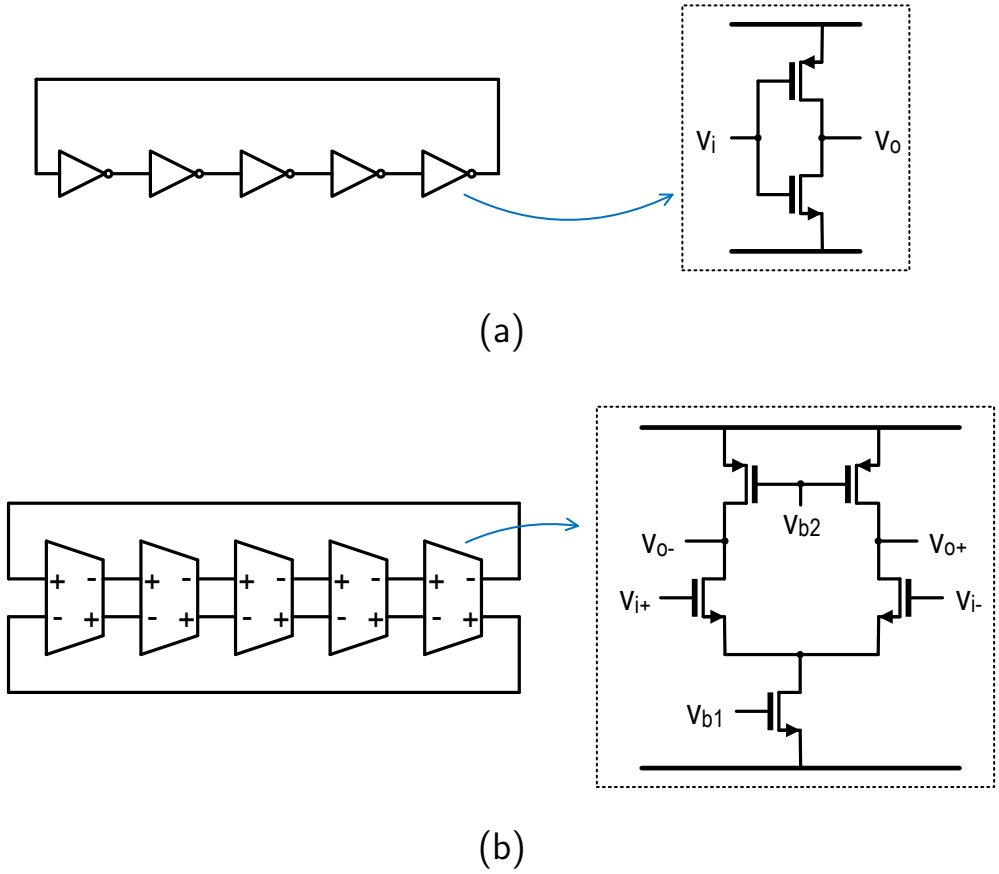


Figure 2.9: Ring oscillator schematic. (a) Single-ended delay stages. (b) Differential delay stages.

would be connected between the output and a reference node (typically ground). In practice, however, one of the terminals of the MEMS is associated with a large parasitic capacitor connected to the substrate (see Figure 2.3) which would destroy the symmetry required for the differential operation. Therefore, single ended ring oscillators are more suitable for the MEMS readout circuit.

Figure 2.10 illustrates three ways to control the three-stage oscillation frequency of a ring oscillator using a capacitive MEMS. The oscillation period is equal to the sum of delays introduced by each stage, i.e., $T_{osc} = t_{d1}+t_{d2}+t_{d3}$. In the approach shown in Figure 2.10(a), the MEMS in connected to the first stage, so only t_{d1} is modulated by the capacitance change. This combination of varying and non-varying delay stages introduces distortion for large t_{d1} variations. Assuming that the load of the first stage is considerably larger than the load of the second and the

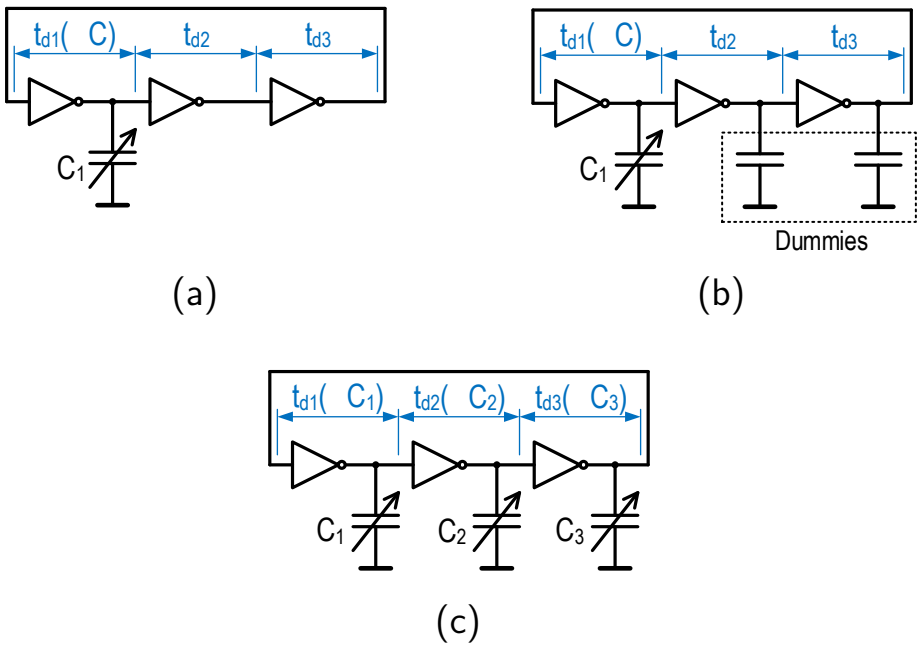


Figure 2.10: Different ways to connect a MEMS to a 3-stage ring oscillator to build a capacitance-controlled oscillator. (a) Single-capacitor MEMS without dummies. (b) Single-capacitor MEMS with dummies. (c) Multi-capacitor MEMS.

third stages, the delay is not equally distributed ($t_{d1}(\Delta C_1) \gg t_{d2} + t_{d3}$), which may be not desirable in terms of phase noise and interference sensitivity [36]. Alternatively, dummy capacitors can be connected to the rest of stages in order to match all the delays, as shown in Figure 2.10(b). However, this approach still suffers from additional distortion because only one of the delays is modulated by the MEMS variation. Moreover, given that $t_{d1}(\Delta C_1) \approx t_{d2} = t_{d3}$, the sensitivity of the oscillator is lower because only one third of the total capacitance depends on the measurand. An interesting alternative is connecting every stage to an acoustic responsive capacitive sensor [18], as shown in Figure 2.10(c). This approach combines good sensitivity and reasonable phase noise and interference immunity. The main drawback of this implementation is that it requires a more complex MEMS with several isolated (or at least partially isolated) capacitors. Figure 2.11 shows two examples of possible multi-capacitor MEMS microphones suitable for implementing the cir-

cuit of Figure 2.10(c). Figure 2.11(a) describes a MEMS on which at least one of the plates (potentially the backplate, because the membrane is a mobile part and may be more difficult to fabricate) is split in three equal parts. Alternatively, three cavities could be fabricated separately as shown in Figure 2.11(b).

(a) (b)

Figure 2.11: Different options to build a multi-capacitor MEMS. (a) One-cavity MEMS with isolated membrane of backplate. (b) Multi-cavity MEMS.

I-C relaxation oscillator

Figure 2.12 shows an example of a relaxation oscillator on which the MEMS is charged an discharged between two thresholds, V_{lo} and V_{hi}, by a current DAC whose output current oscillates between two values, $-I$ and $+I$, controlled by an hysteresis comparator. In this case, the oscillation period is the amount of time required to charge and discharge the capacitor between the two threshold, which is ideally

$$T(t) = \frac{2(V_{hi} - V_{lo}) \cdot C_{MEMS}(t)}{I}. \tag{2.5}$$

From this equation it is clear that the oscillation frequency is linearly proportional to the distance between the MEMS plates. Therefore, this topology is specially good in terms of linearity and sensitivity. However, there are two noise sources that degrade the performance of this oscillator. On one hand, the noise generated inside the hysteresis comparator can be modeled as a variation in the threshold voltages, which modulates the oscillation frequency. On the other hand, the noise generated by the

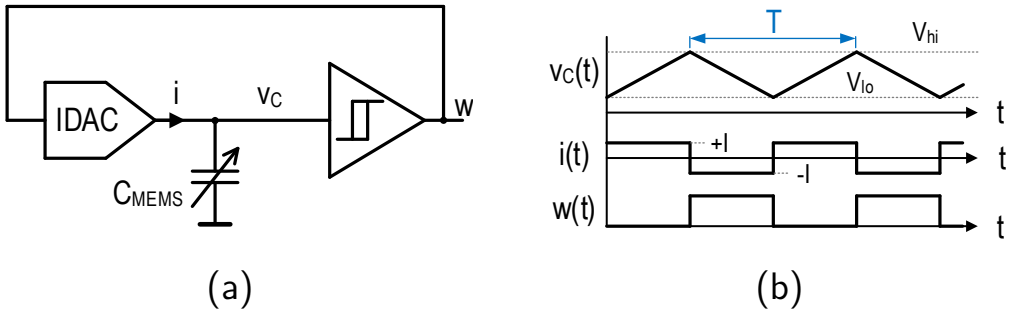


Figure 2.12: Capacitance-controlled I-C relaxation oscillator. (a) Schematic. (b) Circuit operation.

current DAC causes variations in the charging and discharging rates of the capacitor that are indistinguishable from variations in the MEMS capacitance.

Source-coupled multivibrator

Source-coupled multivibrators like the one shown in Figure 2.13 have been intensively studied during the last decades [37–43].

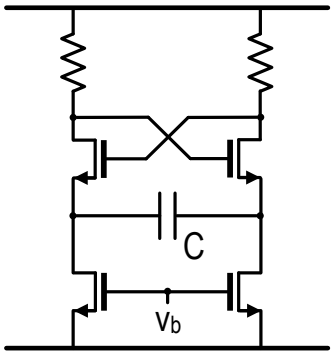


Figure 2.13: Source-coupled multivibrator schematic.

As stated in [40], this oscillator topology can operate both as a sinusoidal oscillator and as a relaxation oscillator, depending on circuit parameters. According to [40], the oscillation frequency in the sinusoidal mode is approximately:

$$f(t) = \sqrt{\frac{g_{m0}}{8\pi^2 RC(C_{gs} + 4C_{gd})}}, \tag{2.6}$$

where g_{m0} is the transconductance of the cross-couple pair, and C_{gs} and C_{gd} are respectively the gate-source and gate-drain parasitic capacitances of the source-couple MOS pair. Therefore, one of the main drawbacks of this topology is that the relationship between the oscillation frequency and the MEMS capacitance involves a square root, which decreases the sensitivity and introduces distortion components for large input signals.

In addition to this problem, it can be observed that the capacitor that sets the oscillation frequency is connected between two twin branches. As stated before, one of the MEMS terminals has a large parasitic capacitance that would destroy the symmetrical operation of the oscillator, which is not recommended for the sack of low phase noise and interference immunity. Alternative topologies are proposed in Figure 2.14, which are based on splitting the main capacitor C into two capacitors with one of the terminals connected to ground. If both capacitors are replaced by MEMS, as shown in Figure 2.14(a), both branches are loaded with identical capacitive loads that are responsive to sound pressure variations, what is optimum in terms of sensitivity and phase noise.

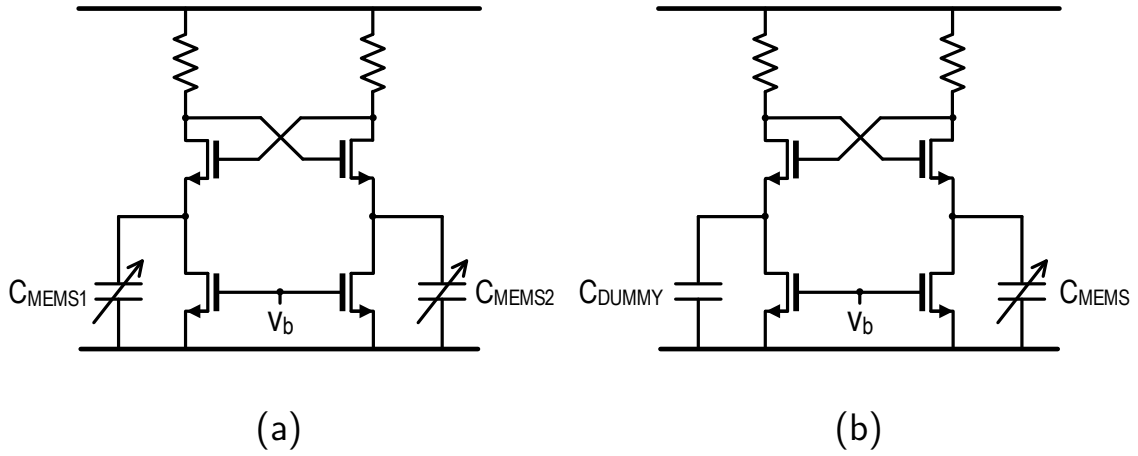


Figure 2.14: Capacitance-controlled source-coupled multivibrator. (a) Two-capacitor MEMS without dummies. (b) One-capacitor MEMS and one dummy.

However, this implementation requires two MEMS (i.e., a multi-cavity MEMS), which may be a problem for low-cost applications. Alternatively, one of the capacitors can be replaced by a dummy capacitor as shown in Figure 2.14(b), but this implies that only half of the capacitive load is responsive to audio, what decreases the sensitivity and introduces distortion. Moreover, since the load is not symmetrical, phase noise may be higher.

2.4.2 LC oscillator

LC oscillators are the most popular choice for generating on-chip high-quality clock signals due to their low phase noise and good frequency stability. Nevertheless, this kind of oscillators can also be used also as a sensor [44]. An LC oscillator consists of an LC tank and an active element, as shown in Figure 2.15. During the startup of the circuit the active element injects energy into the LC tank, which starts to oscillate at a frequency:

$$f(t) = \frac{1}{2\pi\sqrt{L \cdot C(t)}}. \tag{2.7}$$

where L and $C(t)$ are respectively the inductance and the capacitance of the LC tank. The oscillation amplitude increases over time up to an equilibrium point determined by the amplitude control mechanism of the active element. Ideally, the LC tank would maintain this oscillation indefinitely. However, any practical implementation of an LC tank involves parasitics that dissipates energy on each oscillation. Therefore, the active element must inject energy into the tank periodically in order

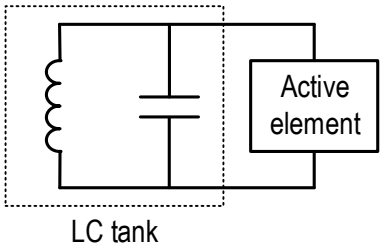


Figure 2.15: Simplified diagram of a generic LC oscillator.

to maintain the oscillation amplitude. Figure 2.16 shows an example of a cross-coupled LC oscillator on which four transistors act as a negative resistance that compensates the losses of the LC tank.

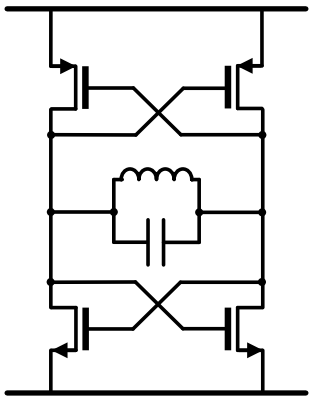


Figure 2.16: Cross-coupled LC oscillator.

Phase noise appears in LC oscillators due to the noise injected by the active element into the tank. Indeed, phase noise is inversely proportional to the quality factor Q [36,45], which among other definitions [37] can be expressed as

$$Q = 2\pi \frac{Energy\ stored}{Energy\ dissipated\ per\ cycle}. \tag{2.8}$$

LC oscillators are specially suitable for frequencies in the range of several GHz which, according to (2.7), can be synthesized using small capacitors and inductors. However, a capacitance-controlled oscillator running at GHz may not be suitable for low power sensor readout circuits because both the oscillator and the F2D converter would consume too much power. Moreover, given that the MEMS capacitance is approximately 2.5 pF (it is actually slightly larger due to parasitics), a frequency oscillation of hundreds of MHz requires an inductor in the order of tens of nH.

One of the main challenges in the implementation of LC oscillators is the integration of the inductor in the chip. Inductors are typically built using metal tracks to draw a coil, as shown in Figure 2.17, which requires a large amount of area. In the technology on which we are trying to develop our capacitance-controlled oscillator (0.13 μm CMOS), an

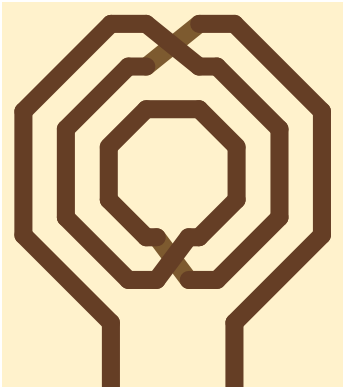


Figure 2.17: Typical implementation of an integrated coil.

inductor larger than 10 nH is nearly unfeasible because it would occupy an area in the range of 0.1 mm^2.

Figure 2.18 shows two proposals for building a large coil taking advantage of the area available on the MEMS. Figure 2.18(a) illustrates an implementation on which the coil is made using metal tracks routed around the MEMS membrane. Alternatively, the inductor could be build using bonding wires to surround the MEMS, as shown in Figure 2.18(b). The advantage of the bonding wire based inductor is that parasitics are potentially smaller than in the metal track coil. However, bonding wires are costly and its length may considerably change from sample to sample. The dimension of metal tracks, in contrast, can be accurately controlled and repeated. Nevertheless, both option are interesting alternatives to implement large coils without consuming hundreds of thousands of square microns of ASIC area.

In addition to the parasitics introduced by the inductor, MEMS parasitics also play an important role in the performance of the readout circuit. On one hand, parasitic capacitors associated with bonding pads and with the MEMS structure add a capacitance to the LC tank, which reduces the oscillator sensitivity and causes distortion for large acoustic input signals. Furthermore, the parasitic resistances due to the membrane and backplates resistivity worsens phase noise and decreases the oscillator sensitivity. As stated before, phase noise is proportional to the LC tank energy losses, which are proportional to the resistive elements present in the tank. The relationship between parasitic resistors and the loss of sensitivity is illustrated in Figure 2.19. Figure 2.19(a) shows the

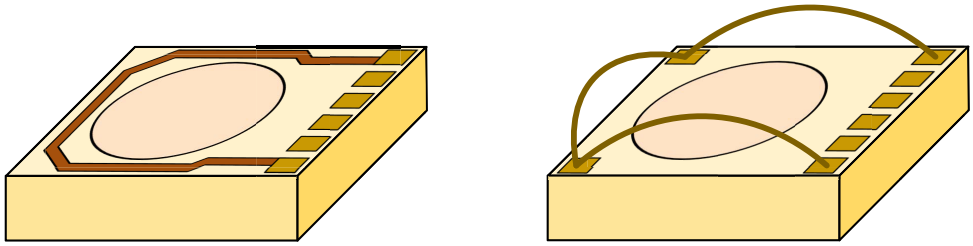


Figure 2.18: The coil can be built using the empty space available on top of the MEMS. (a) Coil build routing metal tracks around the membrane. (b) Coil based on bonding wires.

schematic of a cross-coupled LC oscillator on which the LC tank includes some of the parasitics mentioned in Section 2.2. Figure 2.19(b) shows three curves that represent the oscillation frequency versus R_{MEMS} for three different values of C_{MEMS}: 2 pF (blue), 2.17 pF (red), and 1.85 pF (green). The rest of the parameters are summarized in Table 2.6.

Table 2.6: Values used in the simulation shown in Figure 2.19.

Parameter	Value	Parameter	Value
L_{coil}	25 nH	R_{coil}	10 Ω
C_{pad}	500 fF	$R_{leakage}$	1 TΩ
$L_{bonding}$	2 nH	$R_{bonding}$	20 Ω
W_P/L_P	100 μm / 400 nm	W_N/L_N	50 μm / 400 nm

It can be observed that for low resistances, the oscillation frequency depends on the MEMS capacitance (the sensitivity is approximately -100 MHz/pF, which is only slightly lower than the ideal -150 MHz/pF that can be derived from equation (2.7)). However, as R_{MEMS} is increased, the oscillation frequency increases up to 1.04 GHz and no longer depends on the MEMS capacitance. This happens because the capacitance C_{MEMS} becomes partially isolated from the oscillator, and the effective capacitance of the LC tank is determined by the parasitic capacitors, which are fixed and lower than C_{MEMS}. Table 2.7 shows the simulated relationship between the series resistance and the oscillator

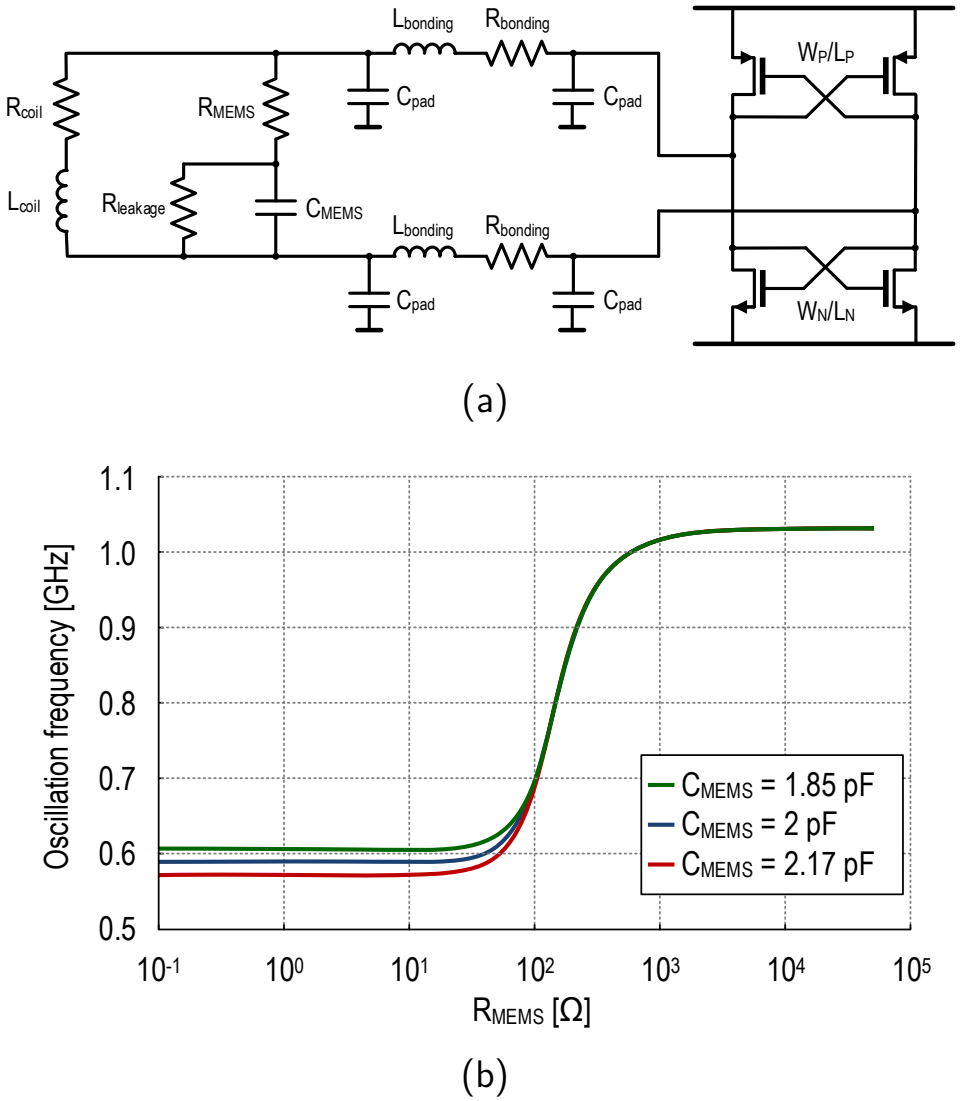


Figure 2.19: (a) Simulated LC oscillator with parasitics. (b) Simulated oscillation frequency versus R_{MEMS} for three different values of C_{MEMS}.

SNR, which is in line with the phenomena described in the last paragraphs.

As stated in Section 2.2, the series resistance of the MEMS microphones considered for building a capacitance-controlled oscillator are in the range of 1 kΩ. According to Figure 2.19 and Table 2.7, the resistance must be well below 100 Ω to target the target performance. Therefore, the MEMS sensors currently available are not suitable for this kind of approach.

Table 2.7: Simulated SNR for different values of R_{MEMS}.

R_{MEMS} [Ω]	SNR [dB]
1	83.3
10	81
50	73
90	51.1

2.5 Conclusion

This chapter we have discussed the feasibility of connecting a capacitive MEMS microphone as the load of an oscillator to build a capacitance-controlled oscillator based readout circuit. The main advantage of this approach is that it does not require a biasing circuitry to charge the MEMS and generate an analog voltage, as is frequently done in available readout circuits (see Section 1.2.3).

However, we have found that the proposed approach is not efficient for several reasons. The first problem is the oscillator sensitivity, which is degraded by several factors. On one hand, the relative capacitance variation due to sound pressure is reduced by the parallel parasitic capacitance of the MEMS, which is a fixed value added to the total MEMS capacitance. Moreover, most of the oscillators considered cannot operate using the MEMS as their only capacitive load due to MEMS parasitics or due to oscillator topology. In consequence, dummy capacitors must be connected to other nodes of the oscillator, increasing the overall load capacitance and therefore decreasing the relative capacitance variation. The resulting sensitivity loss tightens the oscillator specifications in terms of phase noise, making this approach inefficient in power for most of the oscillator topologies. LC oscillators are a popular alternative to implement very low phase noise oscillators. In this chapter we have shown two potential approaches for the implementation of a Q-enhanced inductor integrated with the MEMS, which is one of the main challenges of this topology. Unfortunately we have found that the parasitic resistances of the MEMS membrane and backplates are a limiting factor, given that they isolate the MEMS capacitance from the LC tank,

which implies a drastic sensitivity reduction.

For these reasons, we conclude that using the classical biasing circuitry is more efficient than connecting the MEMS microphone directly to the oscillator. In consequence, we decided to use the biasing circuitry and focus our efforts on the development of efficient oscillator-based data converters. Nevertheless, the idea of integrating a capacitive sensor into the oscillator may be a option to consider for other kind of sensors with lower parasitics.

Part II

High-order VCO-based $\Sigma\Delta$ modulators

CHAPTER 3

Fundamentals of frequency-encoding based $\Sigma\Delta$ modulators

3.1 Introduction

This chapter provides an in-depth look to frequency-encoding based $\Sigma\Delta$ modulators. As introduced in Section 1.3.2, oscillators can be used to build $\Sigma\Delta$ modulators on which one or several intermediate signals are encoded using frequency modulation. These systems can be implemented using mostly-digital circuitry, which benefit from CMOS technology scaling. Therefore, frequency-encoding is potentially advantageous for the implementation of compact analog-to-digital converters for audio applications. As an alternative to embedding the MEMS capacitance into the oscillator, we will deal here with replacing the ADC in a conventional MEMS microphone by a high-order frequency-encoded modulator, as described in Figure 3.1. This will be the analog interface with the MEMS considered for the rest of the thesis.

As mentioned in Section 2.3, digital MEMS microphones must typically provide a single-bit output sampled at several MHz. Under these

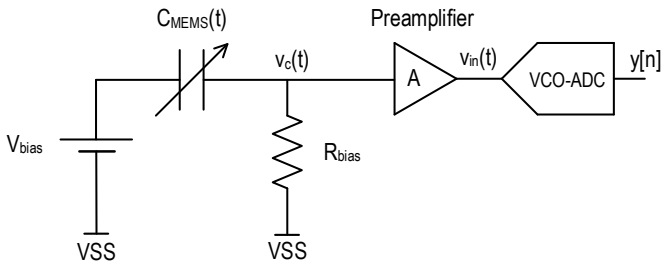


Figure 3.1: Interconnection between a VCO-based ADC and a MEMS microphone using a biasing circuitry.

conditions, first-order ΣΔ modulators require complex auxiliary circuitry (see Fig. 2.8) to reach the target specifications. In contrast, high-order ΣΔ converters can generate a digital output compatible with standard MEMS microphone interfaces without the need for additional signal processing circuitry. In consequence, this part of the dissertation is focused on the development of high-order oscillator-based ΣΔ converters for audio applications.

Oscillator-based ADCs can be divided in two categories: open-loop and closed-loop architectures. Open-loop modulators do not use any feedback loop. Instead, an oscillator is used to encode the input signal into a frequency modulated signal, which is digitized and digitally post-processed. First-order oscillator-based ΣΔ modulators are frequently implemented using open-loop approaches, like [20, 21] or in the converter proposed in Chapter 2. Nevertheless, open-loop configurations can be used to achieve high-order noise shaping, such as the coarse-fine concept presented in [46]. In contrast, closed-loop modulators are implemented with feedback loops. For example, the converter proposed in [27] uses a VCO-based integrator and quantizer as part of a fourth-order ΣΔ modulator. Oscillators can be used to implement also the other stages of high-order closed-loop ΣΔ modulators [22, 47, 48].

In this chapter we explain the concept of phase referenced integrator, on which an oscillator can be used to perform the integration of a signal in combination with digital circuitry. Then, we describe different alternatives to build first-order ΣΔ modulators using phase referenced integrators, including a brief analysis of the loop filter state variables

and the main differences between classical ΣΔ modulators and their oscillator-based counterparts. Finally, we describe some of the oscillator-based modulators reported during the last years, including first-order and high-order modulators in open-loop and closed-loop configurations. This chapter is the basis for the development of high-order oscillator-based ΣΔ modulators presented in Chapter 4.

3.2 Phase referenced integration

One of the key building blocks of frequency-encoding based data converters is the combination of a variable-frequency oscillator and a counter shown in Fig. 3.2(a). The frequency of an oscillator can be controlled by several different magnitudes (e.g., voltage, current, capacitance, resistance...). We use voltage-controlled oscillators as case study, but all the explanations here exposed are still applicable when oscillators are controlled by other magnitude.

The signal produced by a VCO-Counter combination is a staircase whose climbing rate is proportional to the input voltage. Fig. 3.2(b) shows the waveforms of the different signals of a VCO-Counter for a step input signal. This behavior resembles the operation of a classical integrator (properly scaled), whose output for the same input would be the ramp shown in the lower graph of Fig. 3.2(b) in dotted lines. Therefore, we call phase referenced integrator (PRI) the combination of varying-frequency oscillators and digital circuitry (which is typically based on counters) that can substitute a classical integrator in a system. Note that as the oscillation frequency of a VCO can not be negative, the output of the associated counter tends to increase infinitely. Therefore, a PRI must typically include a mechanism to counterbalance this effect and avoid saturation. More details about this will be provided in Section 3.2.1. Furthermore, as show in Fig. 3.2(b), the output of the PRI is quantized in level. The impact of this quantization noise is discussed in Section 3.2.2.

In this section we describe two different ways to model the VCO-Counter pair. The first option is based on modeling the oscillator as a

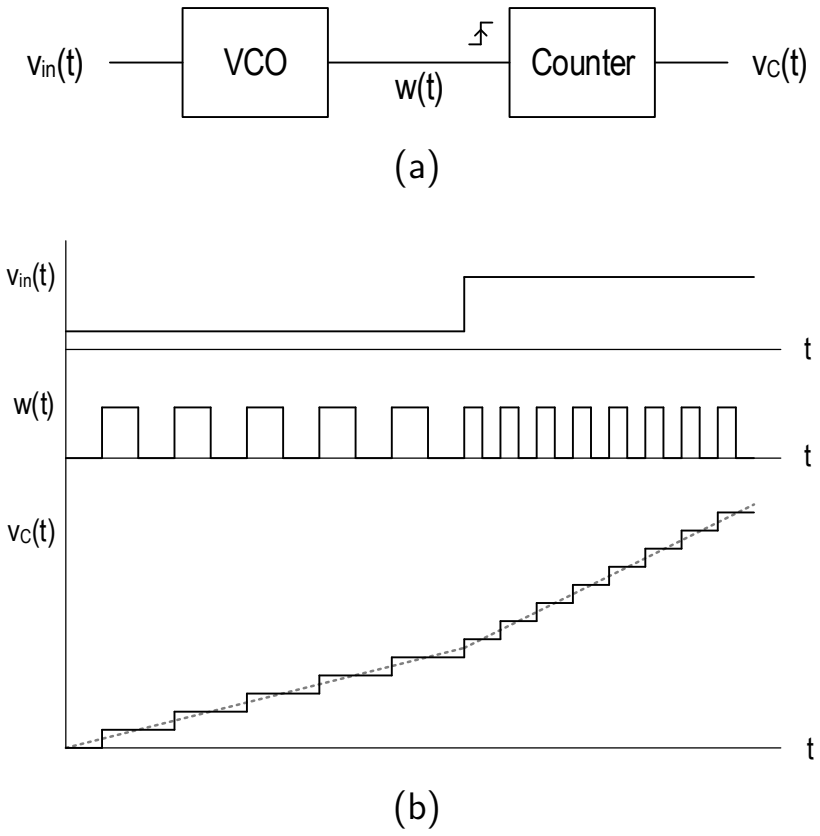


Figure 3.2: (a) VCO-Counter structure used to perform the phase referenced integration. (b) Input signal, VCO oscillation, and output signal of a VCO-Counter

phase integrator followed by a phase wrapper, whereas the counter acts as phase unwrapper. On the other hand, a VCO can be modeled as an encoder which generates a train of impulses that are lately integrated by the counter.

3.2.1 Oscillator as a phase integrator model

Voltage-controlled oscillator model

An ideal oscillator with fixed oscillation frequency f_0 can be represented as shown in Fig. 3.3(a). The oscillator phase ($\varphi(t)$, in radians) is the integral of the frequency ($\omega(t) = 2\pi \cdot f(t) = 2\pi \cdot f_0$, in rad/s) over time:

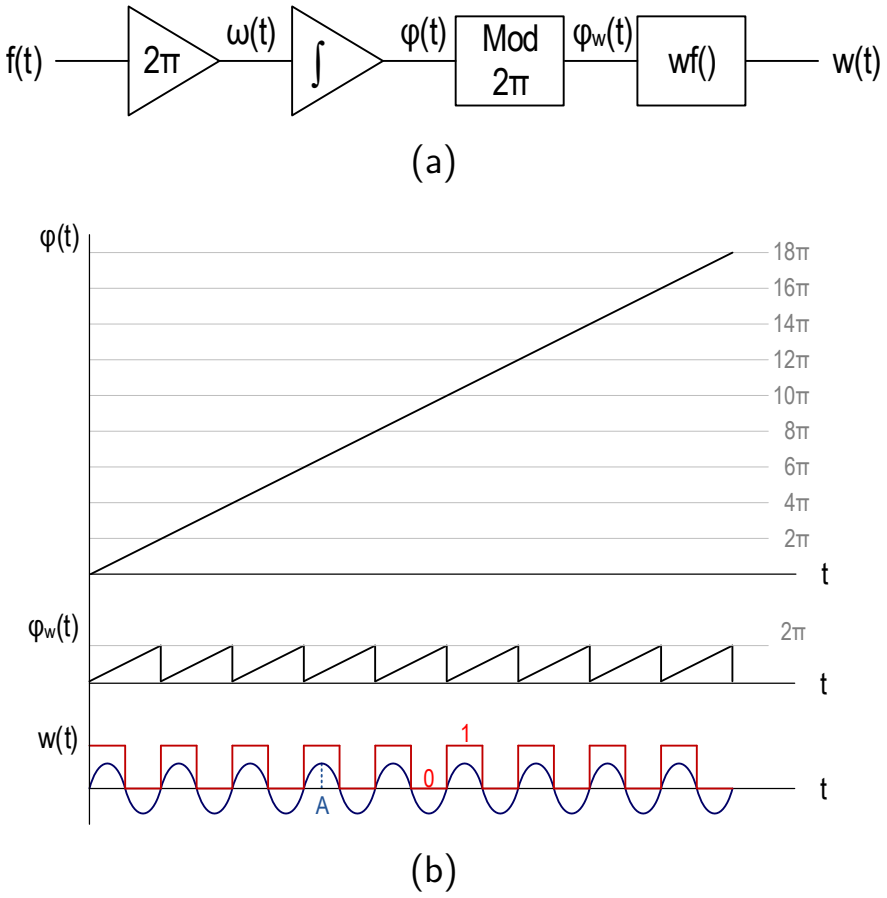


Figure 3.3: Description of fixed-frequency oscillator. (a) Block diagram. (b) Non-wrapped phase, wrapped phase, and output oscillation for two different waveform functions: sinusoidal (blue) and square (red).

$$\varphi(t) = \int 2\pi f_0 dt. \tag{3.1}$$

The oscillation frequency is real and positive, which implies that $\varphi(t)$ grows indefinitely over time. The block "Mod 2π" (or "phase wrapper") of Fig. 3.3(a) calculates the wrapped equivalent of $\varphi(t)$, $\varphi_w(t)$, whose value belongs to the interval $[0, 2\pi)$ and differs from $\varphi(t)$ in a entire multiple of 2π, as shown in Fig. 3.3(b). The output voltage is related to the wrapped phase through the waveform function $wf(\varphi_w)$. For the case of a sinusoidal oscillator,the waveform function is

$$wf(\varphi_w) = A \cdot sin(\varphi_w). \tag{3.2}$$

However, given that our intention is to connect the oscillator to a digital circuit, a square oscillation is preferred over any other waveform. Most of waveforms can be turned into a square wave by passing it through a comparator, whose output is compatible with digital circuits. The waveform function of a 50% duty cycle square oscillation is

$$wf(\varphi_w) = \begin{cases} 1 & \text{if} \quad 0 \leq \varphi_w < \pi, \\ 0 & \text{if} \quad \pi \leq \varphi_w < 2\pi. \end{cases} \tag{3.3}$$

This way of modeling an oscillator can be extended to a VCO, as shown in Fig. 3.4. In a VCO, the oscillation frequency is modulated by the input voltage following

$$f(t) = f_0 + K_{VCO} \cdot v_{in}(t) = f_0 \cdot (1 + k_d \cdot v_{in}(t)), \tag{3.4}$$

where f_0 is the center frequency (the oscillation frequency when zero input is applied), $v_{in}(t)$ is the input signal, K_{VCO} is the absolute sensitivity (which is typically expressed in Hz/V), and k_d is the relative sensitivity (typically in V^{-1}). Hence, in an ideal VCO the input signal is encoded without loss of information in the slope of $\varphi(t)$. The output oscillation ($w(t)$), however, provides limited information about the instantaneous phase, depending on the waveform function implemented. In the case of the square wave of equation (3.3), from the instantaneous value of $w(t)$ we can only know whether the wrapped phase is lower of higher than π radians.

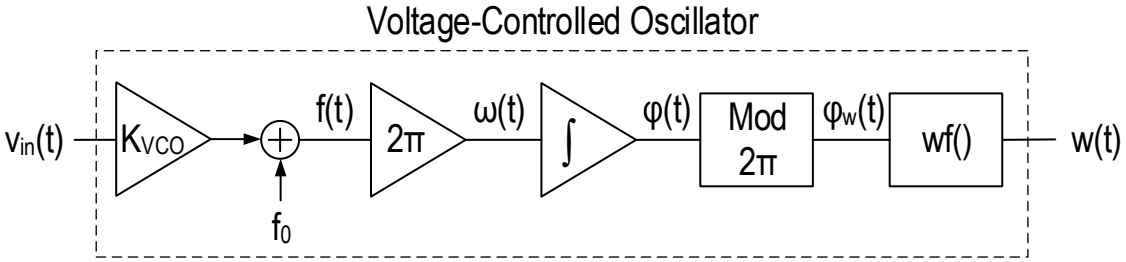


Figure 3.4: Model of a voltage-controlled oscillator.

Counters and phase unwrapping

Although a VCO already performs the integration, as stated in the previous subsection, phase wrapping makes impossible to use a VCO directly as integrator in most of the cases. A simple argument to support this assertion is that, generally speaking, we can not know how much phase has been integrated during a given time interval by only looking at the output of the VCO at the beginning and at the end of this interval, unless we keep track of the number of cycles occurred. This can be done with a digital counter, as long as the output of the oscillator is a square signal capable of driving digital circuits. A counter can be designed to increment its value by rising, falling, or by both edges.

Fig. 3.5 illustrates the operation of a PRI with a counter responsive to both edges. Assuming that the wave function of the VCO is the one described by equation (3.3) (i.e., the oscillation is an square wave with 50% of duty cycle), the output of the counter represents the unwrapped phase quantized in steps of π radians and divided by π. Fig. 3.5(b) shows the equivalent model of the PRI described. In contrast, if the counter only responds to the rising (or falling) edge of the oscillation, the output signal represents the unwrapped phase quantized in steps of 2π radians and divided by 2π, as shown in Fig. 3.6.

It can be observed that using a counter responsive to both edges results in a more accurate representation of the phase at the output of the counter, because the quantization step is smaller (one half). However, this implementation may present two disadvantages in certain cases. On one hand, designing a counter which value is increased in both rising and falling edges of a signal is slightly more complex, and may require larger silicon area and higher power consumption. But more importantly, the waveform function of an oscillator has not necessarily a 50% of duty cycle. Therefore, the distance between rising and falling edges is not π radians, which introduces irregular quantization steps as shown in Fig. 3.7. For these reasons, we will focus on counters only responsive to one of the edges (arbitrarily, rising edges). Therefore, unless otherwise stated, we will restrict the use of the term PRI to refer to subsystems based on the structure of Fig. 3.6(b), which can be simplified as shown

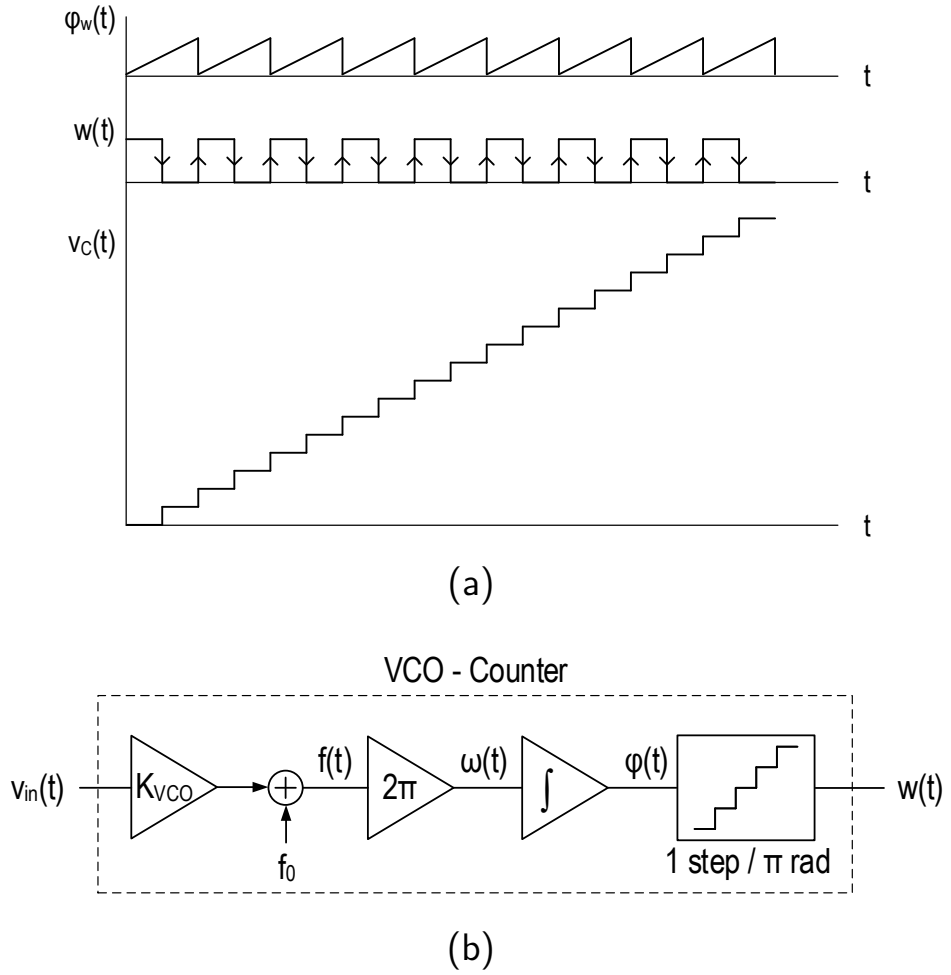


Figure 3.5: (a) Operation of a VCO connected to a both-edges responsive counter. (b) Equivalent model of the resulting VCO-Counter.

in Fig. 3.8

In summary, a counter can be connected to the output of an varying-frequency oscillator to compensate its inherent phase wrapping. The resulting structure is called PRI and works similar to a classical integrator, with two important differences. The first difference is that whereas a classical integrator can integrate both positive and negative (and typically integrates a zero-mean signal to avoid saturation), the frequency of an oscillator cannot be negative. For a zero-mean input signal, the PRI integrates the offset frequency f_0, as shown in Fig. 3.8. This DC value can not be compensated by any input signal, because negative oscillation frequencies are not easily implementable in real circuits. Therefore, the output of the counter tends to grow infinitely, unless periodic subtrac-

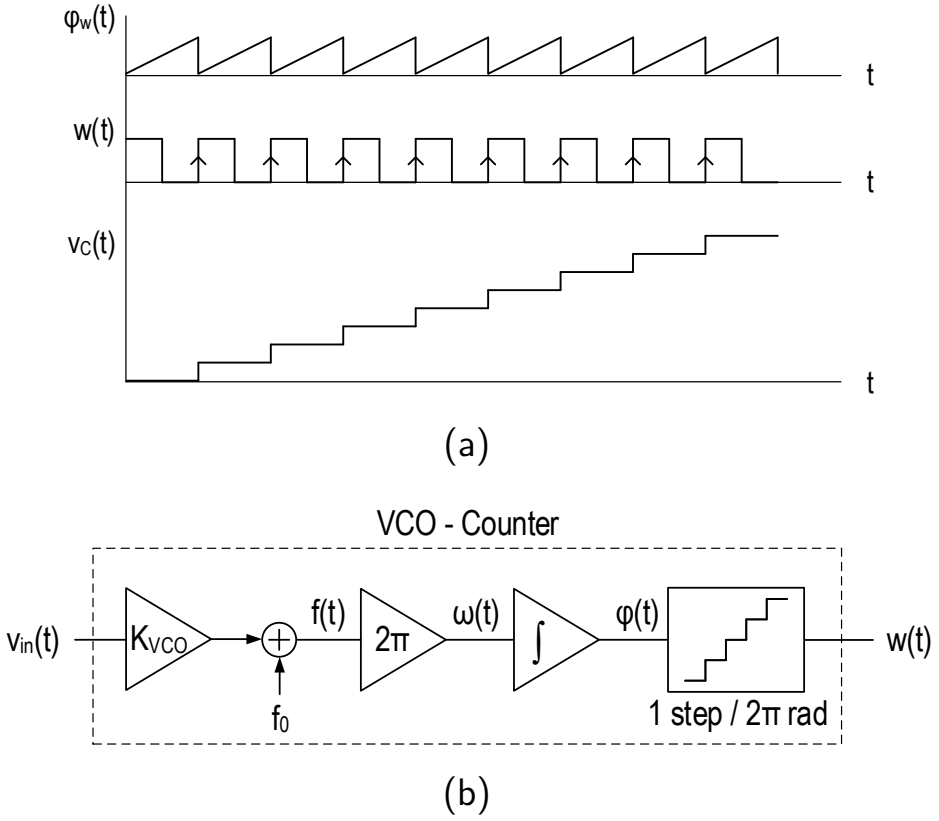


Figure 3.6: (a) Operation of a VCO connected to a rising-edge responsive counter. (b) Equivalent model of the resulting VCO-Counter.

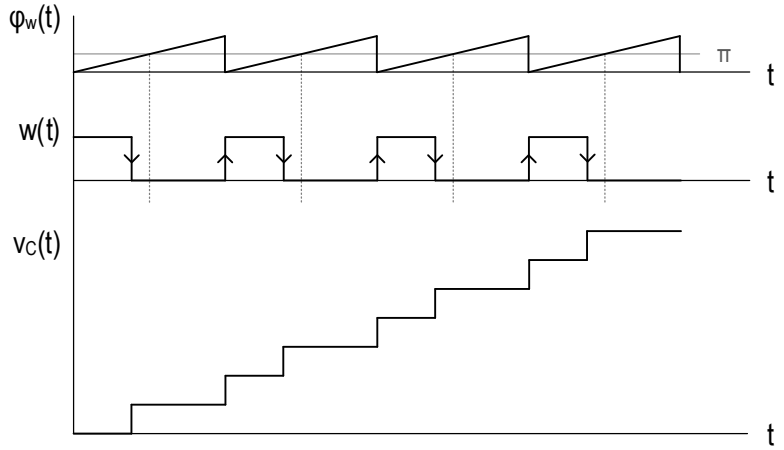


Figure 3.7: Using both edges of the oscillation results in irregular quantization steps if the duty cycle is other than 50%.

tions are performed as explained in Section 3.2.1. The other difference between the proposed PRI and a classical integrator is "phase quanti-

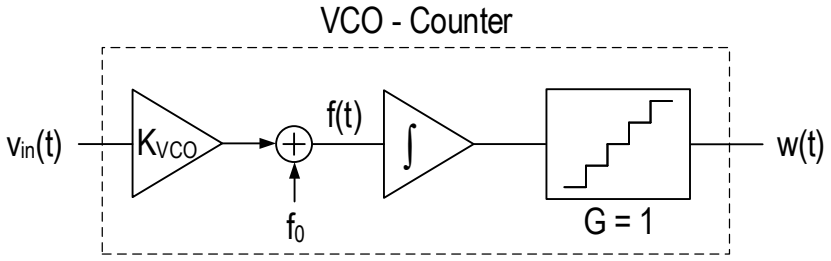


Figure 3.8: Equivalent model of a VCO-Counter when only rising edges are taken into account.

zation noise", which is the error introduced by the quantizer shown in Fig. 3.8. The influence of phase quantization noise in phase referenced integrators will be discussed in Section 3.2.2.

DC integration compensation

As stated in the previous section, the oscillation frequency $f(t)$ must be positive (or zero), since negative frequencies are not physically implementable. Therefore, for a zero-mean input there is positive constant value (f_0) that is continuously integrated, with the potential risk of saturating the digital counter connected at the output of the oscillator. This distances the behavior of the proposed PRI from the operation of a classical integrator, on which zero-mean inputs generate finite output signals.

Therefore, a PRI must include a mechanism to compensate the integration of the mean oscillation frequency (f_0 for a zero-mean input voltage). Figure 3.9(a) shows a theoretical DC compensation method based on counterbalancing the continued growth of the counter with the analog integration of a constant value, as shown in Figure 3.9(b). This figure also illustrates the spectrum of the output signal. On one hand, the integral of the input tone is visible at f_{in}, represented in black. In addition, phase quantization error (whose spectral properties are described in Section 3.2.2) can be observed at the oscillation frequency and its harmonics plotted in red. However, this compensation mechanism is not practical because it requires an analog integrator, and the subtraction of an analog voltage to a digital value is not obvious.

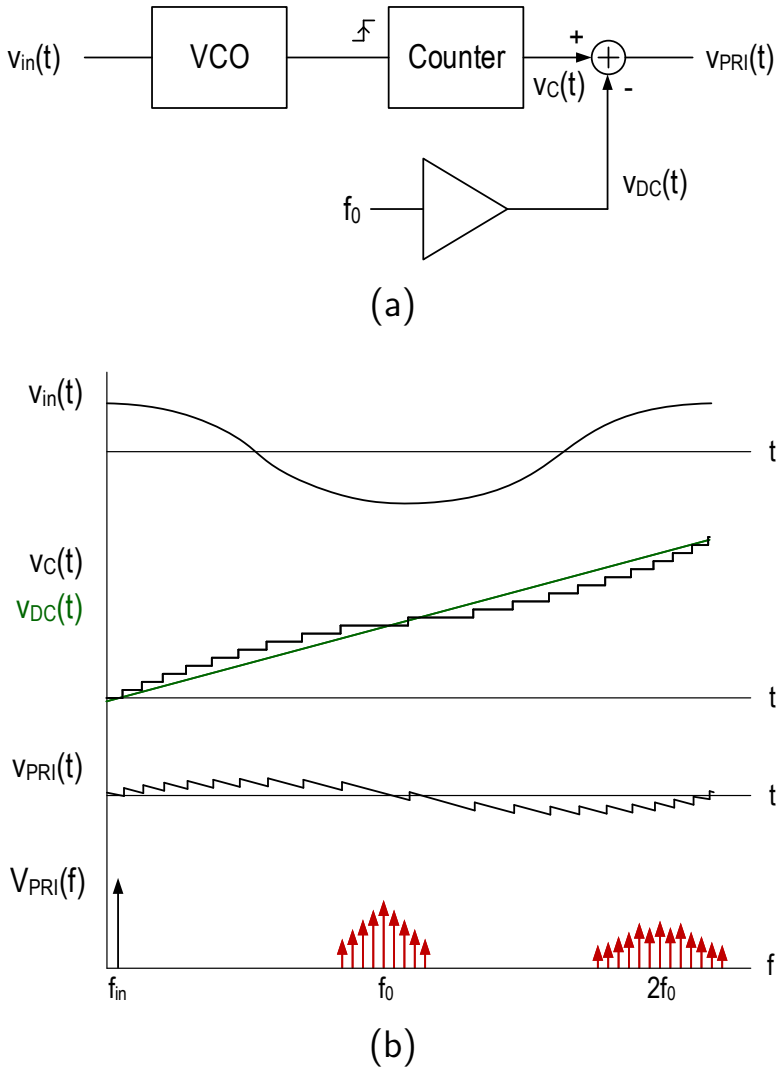


Figure 3.9: Ideal DC compensation based on an analog integrator. (a) Block diagram. (b) Input signal, output of the counter and DC compensation ramp, PRI output, and spectrum of the PRI output.

Fig. 3.10(a) illustrates a possible way to implement an alternative DC compensation mechanism by means of two identical VCO-Counter units. The unit at the bottom of Fig. 3.10(a) performs the phase referenced integration of the mean oscillation frequency, which is digitally subtracted to the main unit which integrates the input signal. An alternative implementation of this system for differential input signals is shown in Fig. 3.10(b), on which each VCO-Counter unit integrates one of the sides of the input signal. Note that the use of two independent counters is not advised in neither the single-ended nor the differential

configuration because both counters would tend to increase infinitely up to saturation. The subtraction of two counters is equivalent to an up-down Counter (UDC) whose value increments and decrements in response to rising edges on its respective inputs.

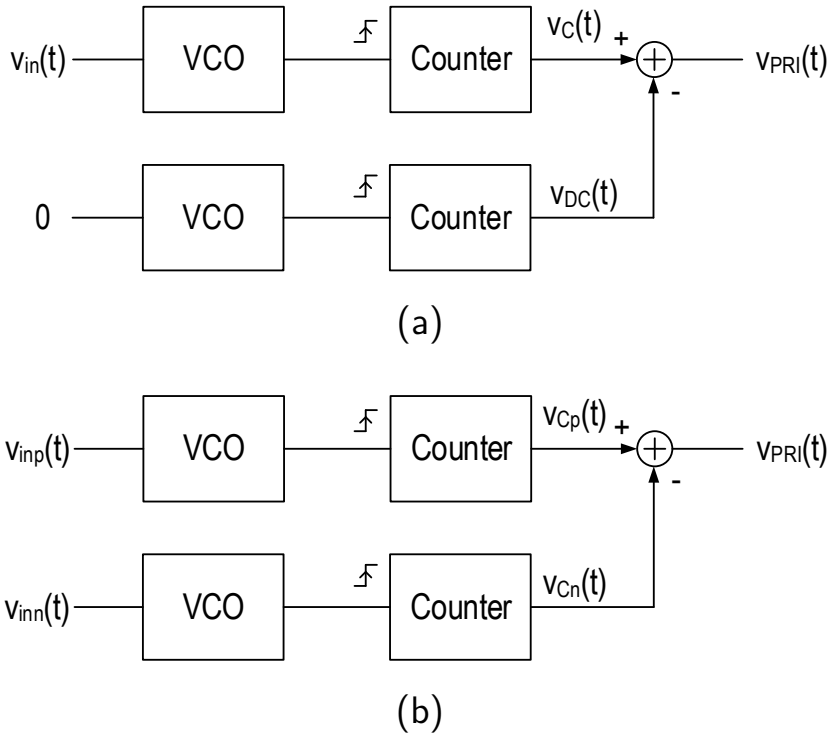


Figure 3.10: DC compensation based on a twin VCO-Counter unit. (a) Single-ended input. (b) Differential input.

However, the compensation of the mean oscillation frequency using a twin oscillator is typically not efficient, as it requires an additional oscillator which doubles the power consumption and silicon area. Another alternative implementation is to replace the second VCO-Counter unit with a discrete-time digital integrator, as shown in 3.11. This implementation is more efficient because it does not need to generate an additional oscillator, but it reuses an fixed-frequency oscillation (f_{ref}) already present in the system, such as the sampling clock. If the frequency of this auxiliary oscillation is not equal to the mean oscillation frequency of the main oscillator, a gain f_0/f_{ref} must be introduced to achieve the desired compensation. Figure 3.11(b) shows an example of the operation of this DC compensation method for $f_{ref} = f_0/4$. It can be observed that the output spectrum is composed by three groups of signals. Firstly, the

integral of the input tone can be found at f_{in} (black). Secondly, phase quantization errors appear around the oscillation frequency and its harmonics (red). Finally, the difference between the ideal DC compensation ramp and the staircase is a sawtooth signal whose spectral components are located at f_{ref} and its harmonics.

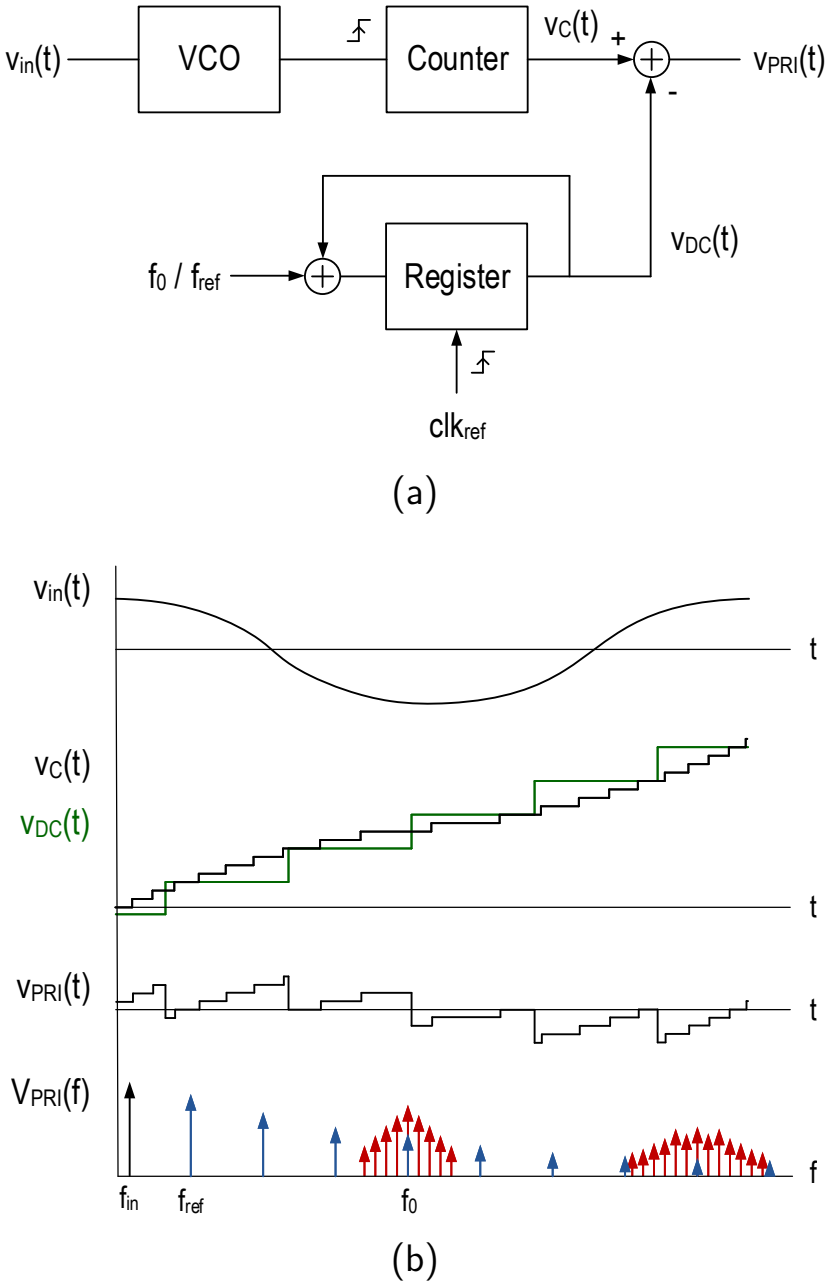


Figure 3.11: DC compensation based on digital integration. (a) Block diagram. (b) Input signal, output of the counter and DC compensation staircase, PRI output, and spectrum of the PRI output.

Any of these PRIs including a VCO-Counter structure and a DC compensation method can be modeled as shown in Figure 3.12, where signals (e_{DC}) and (e_{φ}) are respectively the deviation from the chosen DC compensation mechanism and an ideal integrator, and the phase quantization error.

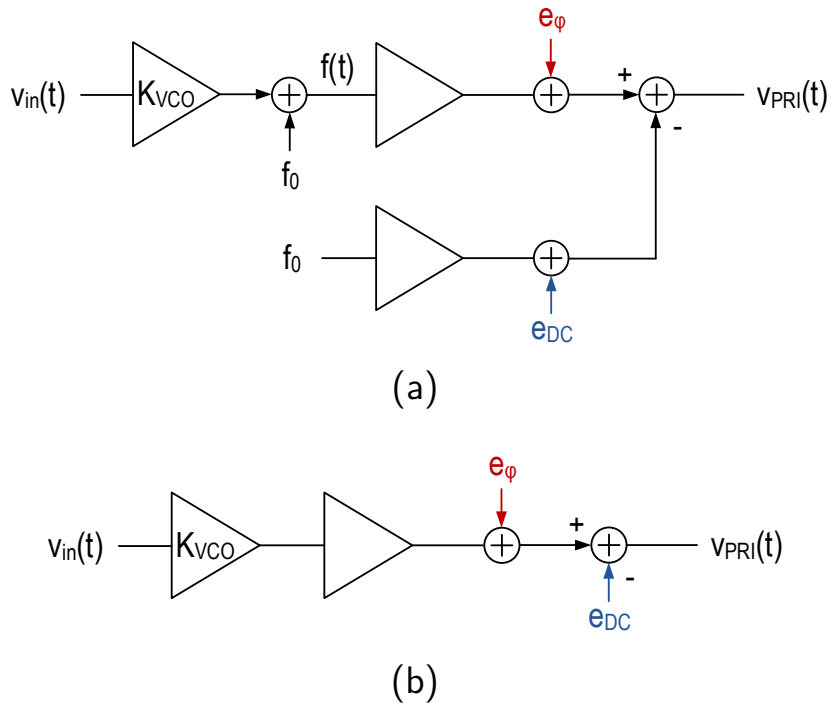


Figure 3.12: Phase quantization error (e_{φ}) and DC compensation error (e_{DC}) modeled as signals added to ideal integrators.

3.2.2 Phase quantization noise and the PFM-based model

Phase quantization noise is the other major difference between phase referenced integrators (as we have defined them in this work) and traditional integrators. The quantization process has been widely studied in the literature [10, 21, 49–51]. Quantization can be modeled as the addition of a quantization error to the input signal to obtain the quantized signal, as shown in Figure 3.12.

In classical ΣΔ modulators, quantization noise is typically studied assuming that the input of the quantizer is very active (almost random),

and this causes that the error introduced by the quantizer is a random signal. Under this assumption, quantization noise spectral density can be considered constant over frequency, which simplifies the analysis of SNR degradation. However, as can be observed in Figure 3.8, the input of the quantizer is not close to a random signal because it is dominated by the integral of the mean frequency, except for very large input signals. Conversely, the power of the phase quantization error is concentrated close to the oscillation frequency and its harmonics, as shown in Figure 3.11(b) in red. The spectral distribution of this error depends on several system parameters, such as the oscillation frequency, the VCO sensitivity, and the power and shape of the input signal. A more in-depth analysis of phase quantization noise in phase referenced integrators can be performed using the pulse frequency modulation (PFM) model presented in [51–54].

PFM-based model

The system displayed in Figure 3.9(a) can be modeled as shown in Figure 3.13 [51]. In this alternative representation, a counter is described as an edge detector connected to an analog integrator. The edge detector generates a Dirac delta on each rising edge of the VCO, producing a train of impulses whose frequency is the VCO frequency, which is integrated to obtain an staircase at the output of the counter. Figure 3.14 shows the different signals of this system, both in the time-domain and in the frequency-domain, assuming the following cosine input signal:

$$v_{in}(t) = A \cdot \cos(2\pi f_{in} t). \tag{3.5}$$

Therefore, the oscillation frequency of the VCO is

$$f(t) = f_0 + K_{VCO} A \cdot \cos(2\pi f_{in} t). \tag{3.6}$$

The oscillation is a square wave whose spectrum consists of FM modulation components around the oscillation frequency and its odd harmonics, in addition its DC value. The edge detector transforms this FM signal into a PFM signal, which can be expressed in the frequency domain as follows:

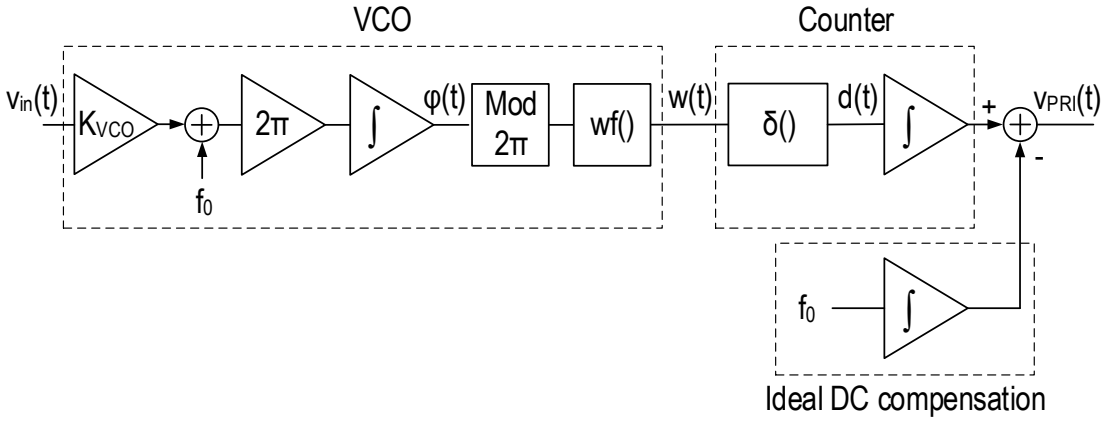


Figure 3.13: Alternative model of a PRI based on Pulse-Frequency Modulation

$$d(t) = f_0 + K_{VCO} v_{in}(t) + m(t), \tag{3.7}$$

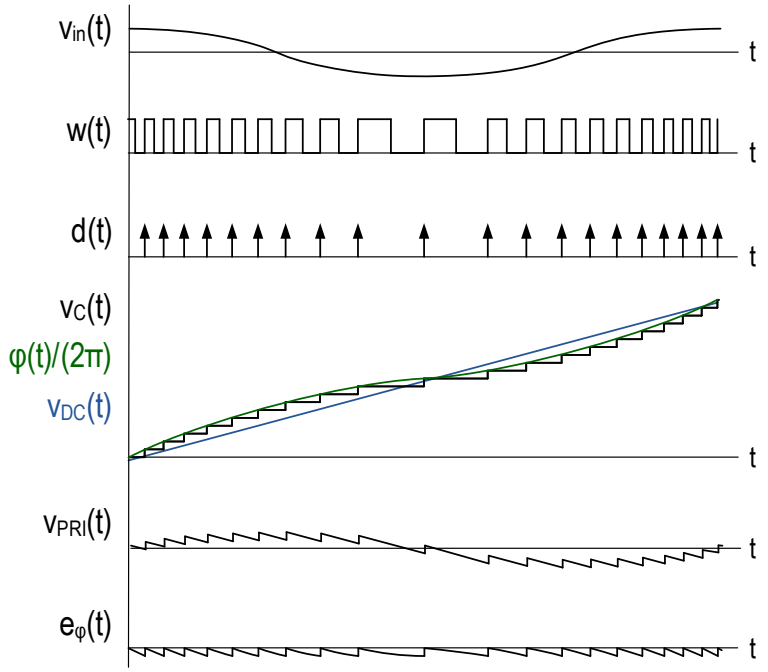
$$m(t) = 2f_0 \sum_{q=1}^{\infty} \sum_{r=-\infty}^{\infty} J_r\left(q\frac{AK_{VCO}}{f_{in}}\right)\left(1+\frac{rf_{in}}{qf_0}\right)\cos\left(2\pi(qf_0+rf_{in})t\right), \tag{3.8}$$

where J_r is the r-th order Bessel function of the first kind [51, 55].

The spectrum of this signal, $D(f)$, consists of a DC component (f_0), the modulating tone at low frequencies ($K_{VCO} \cdot v_{in}(t)$), and PFM modulation components around the oscillation frequency and its harmonics ($m(t)$). The power and the spectral distribution of these components depend on the input tone, the oscillation frequency, and the VCO sensitivity. The DC value of d(t) is counterbalanced by the DC compensation mechanism, and thus this term can be canceled. Therefore, the output of this phase referenced integrator is composed by the integral of the input signal plus the integral of the high frequency PFM components. This is equivalent to the system depicted in Figure 3.12(b), where the phase quantization error is the integral of the high frequency PFM components:

$$e_\varphi(t) = \int_0^t m(\tau)d\tau. \tag{3.9}$$

This expression can be used to calculate the spectral distribution of the phase quantization error for a VCO-counter unit with a single-tone



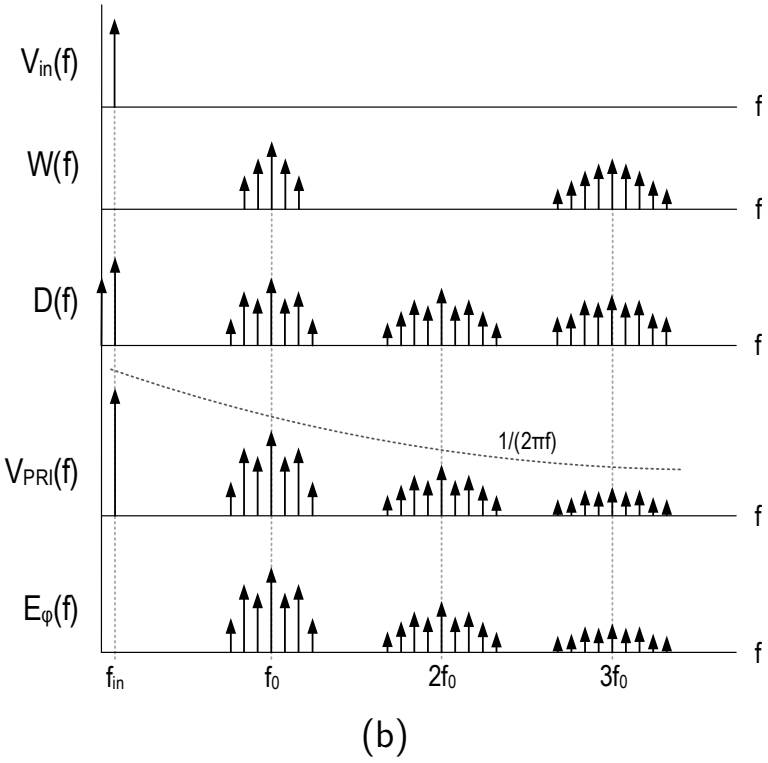


Figure 3.14: Signals of the PFM-based model of the PRI shown in Fig. 3.13. (a) Time domain. (b) Frequency domain.

sinusoidal input. The spectral shape of the PFM modulation components depends on the parameters such as the VCO sensitivity and the amplitude of the input tone. Furthermore, if f_0 and K_{VCO} are properly chosen, phase quantization noise can be almost entirely out of the band of interest before sampling. However, sampling and the associated aliasing may cause that part of this noise appears inside the band.

3.3 VCO-based first-order ΣΔ modulators

This section provides examples of how VCOs and VCO-Counter units can be used to build first-order ΣΔ modulators, including single-phase and multi-phase implementations.

3.3.1 System concept

Figure 3.15 illustrates how a first-order continuous-time ΣΔ modulator can be transformed into a VCO-based ADC using a VCO-Counter unit and digital circuitry, based on the equivalence explained in previous sections.

Figure 3.15(a) shows a classical first-order ΣΔ modulator, on which the output $y[n]$ is subtracted from the input v_{in} through a non-return-to-zero (NRZ) DAC modeled by a gain a. Let's assume that gain of the quantizer is 1, and that its output is always an integer value (i.e, the quantization step is also 1). This system can be transformed in the modulator displayed in Figure 3.15(b) after three modifications: firstly, the integration of the input signal has been split from the integration of the feedback; secondly, a constant c has been added to the input of both integrations; finally, the continuous-time integrator of the feedback is replace by its discrete-time counterpart. This modulator is equivalent to the system of Figure 3.15(c) if $b = K_{VCO}$, $c = f_0$, and if $(y[n] \cdot a + f_0)/f_s$ is an integer number (so it is not affected by the quantization process) for any possible value of $y[n]$. Note that the resulting system can be implemented with a VCO-Counter unit to perform the signal integration, whereas feedback integration and the DC compensation can be done by means of a digital filter. If $a = f_s$, the output of the modulator can be

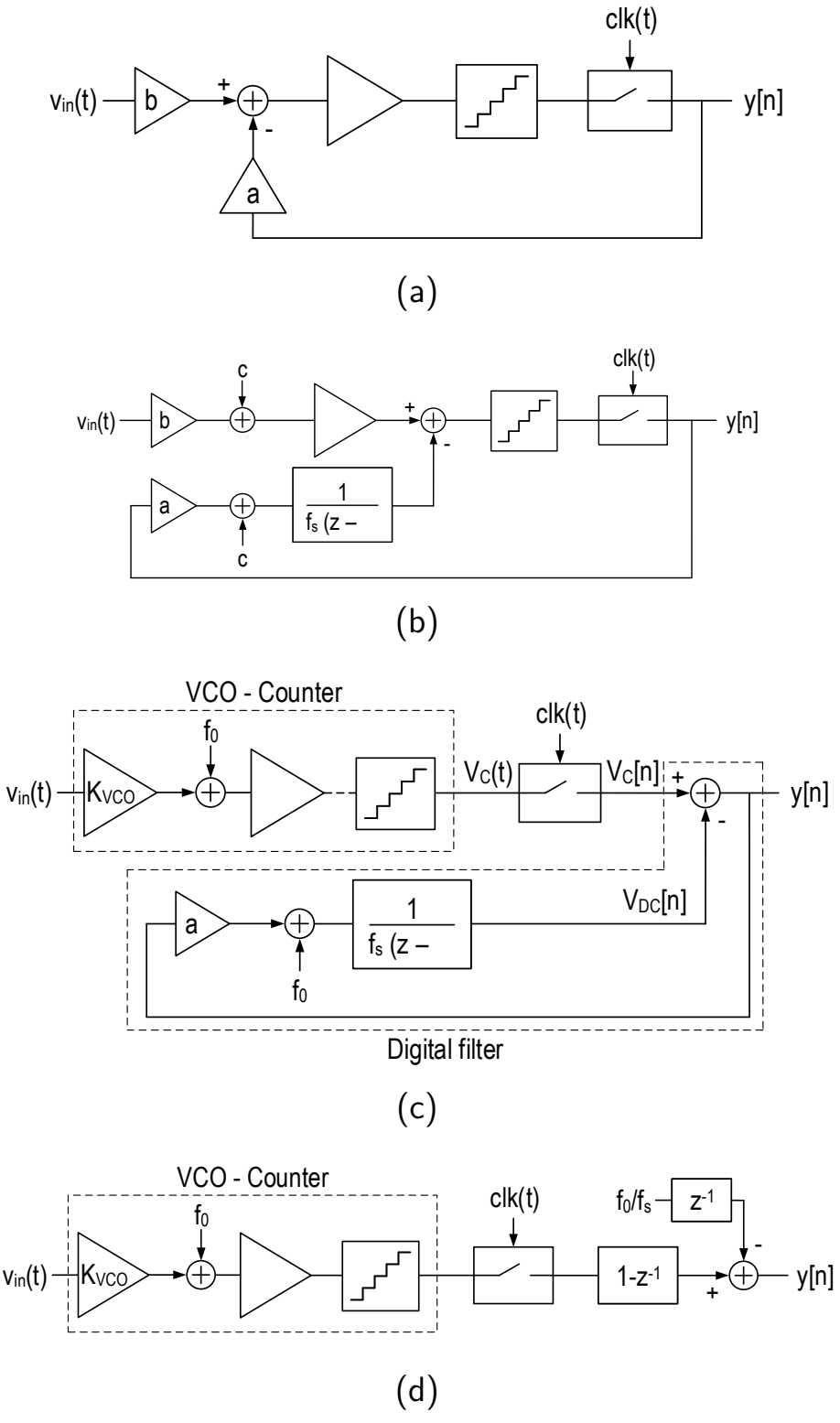


Figure 3.15: Transformation of a classical first-order ΣΔ modulator (a) into a VCO-based modulator (d).

expressed as

$$Y(z) = V_C(z) \cdot (1 - z^{-1}) - \frac{f_0}{f_s} \cdot z^{-1}, \tag{3.10}$$

which is equivalent to the system shown in 3.15(d). In this implementation, the input signal is integrated by a VCO-Counter unit, whose output is sampled and differenced (i.e, high-pass filtered). Therefore, the transfer function of the signal (STF) is almost flat, whereas the transfer function of the phase quantization noise corresponds to a high-pass filter. Figure 3.16 illustrates the behavior of phase quantization noise assuming a sinusoidal input at frequency f_{in} and an arbitrary sampling frequency. In this example, phase quantization error consist of a series of progressively wider modulation sidebands centered on the oscillation frequency and its multiples [54]. After sampling (and the subsequent aliasing) quantization phase noise power is distributed over the full discrete band, resulting in the combination of white noise with some of the PFM sidebands protruding from it. These protrusions are also visible in the output spectrum, which shows first-order noise shaping due to the high-pass filtering performed by the differentiator.

3.3.2 Practical single-phase implementations

Implementing the VCO-based modulator as described in Figure 3.15(d), where a VCO is connected to a counter whose value is sampled and filtered, is not practical because the value of the counter that follows the VCO would increase infinitely. In contrast, in the implementation shown in Figure 3.17 the first difference is performed by reseting the counter immediately after registering it, so the value sampled is the amount of rising edges occurred during the sampling period. Therefore, the average value of the output sequence is f_0/f_s, which could be compensated if needed by subtracting a constant value after the register, as shown in Figure 3.15(d). Alternatively, instead of reseting the counter, it could be preset to $-f_0/f_s$ in order to compensate the DC component without requiring an additional digital adder.

The number of bits required in the counter depends on the relation-

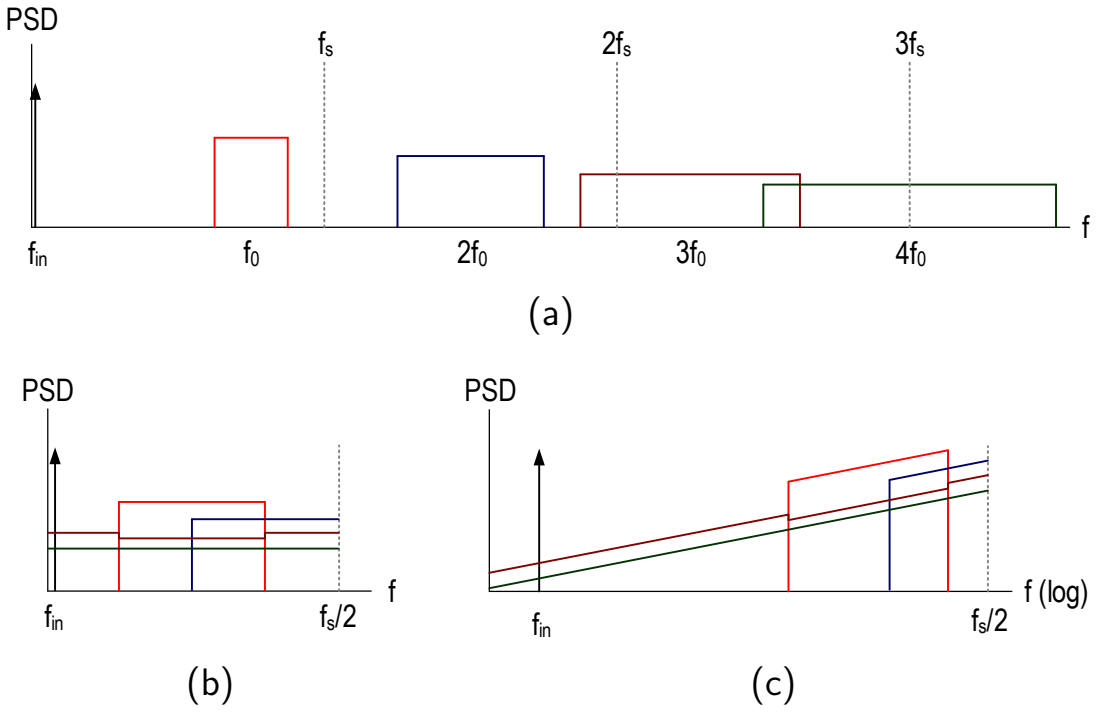


Figure 3.16: Power spectral density (PSD) of the input tone and phase quantization noise in different nodes of the system of Fig. 3.15(d). (a) $v_C(t)$. (b) $v_C[n]$. (c) $y[n]$.

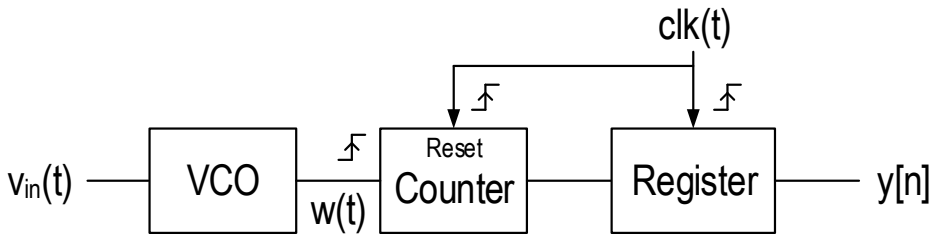


Figure 3.17: Practical implementation of a multi-bit first-order VCO-based ΣΔ modulator.

ship between the maximum oscillation frequency of the VCO and the sampling frequency. There are particular cases on which the modulator does not even require a classical counter, but it can be implemented using a simplified logic. For example, Figure 3.18 shows an alternative implementation that can be used when the sampling frequency is higher than twice the maximum oscillation frequency of the VCO. The modulator consists of a VCO whose oscillation is sampled by a flip-flop, which is connected to a AND-gate based rising-edge detector. Figure 3.18(b)

illustrates the operation of this circuit for $f(t) = f_s/4$, where the output $y[n]$ is '1' only when $Q_1[n] = \overline{Q_2[n]} = 1$, which occurs immediately after a rising edge of the VCO.

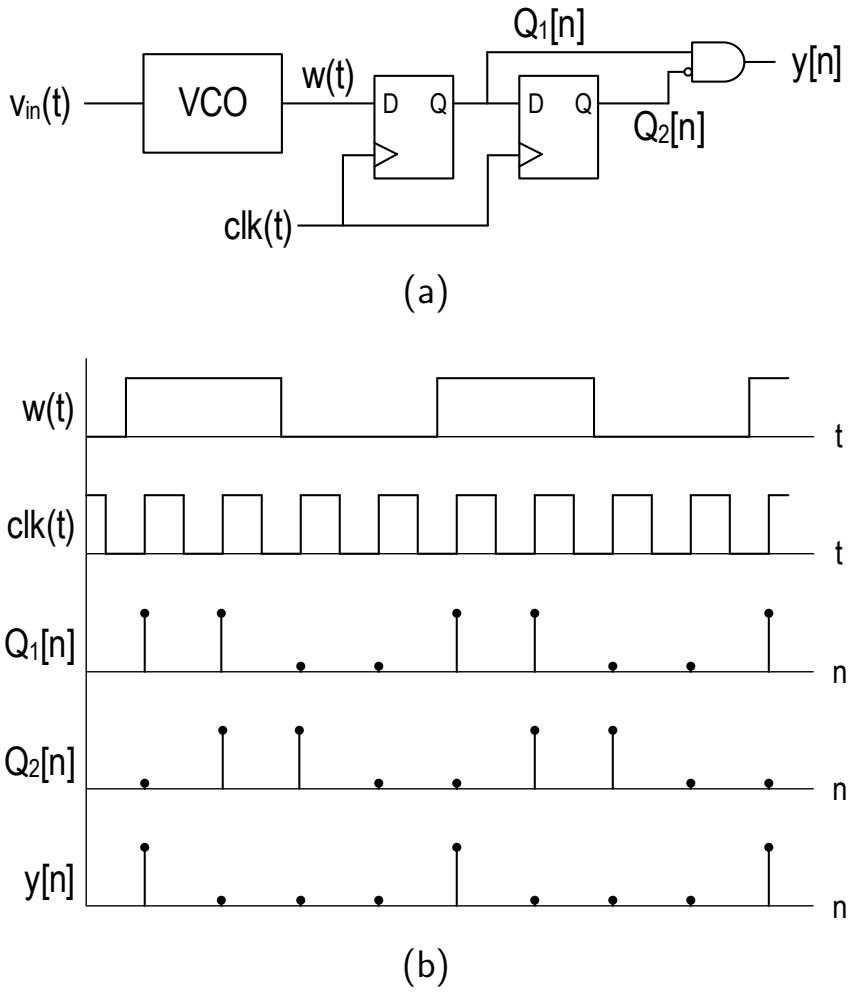


Figure 3.18: VCO-based first-order ΣΔ modulator based on an AND-based counter.

3.3.3 Multi-phase implementation

As mentioned in Section 3.2.1, using only the rising edges of the oscillation implies that phase is quantized in step of 2π radians. However, alternative implementations allow reducing the quantization step. For example, in the system of Figure 3.19(a), both edges of the oscillation are taken into account so, if the duty cycle of the oscillation is 50 %, the quantization is performed in steps of π radians, which reduces the noise

power and shifts its spectral distribution to higher frequencies [54]. The XOR-based modulator of Figure 3.19(b) detects both rising and falling edges, operating as shown in Figure 3.19(c).

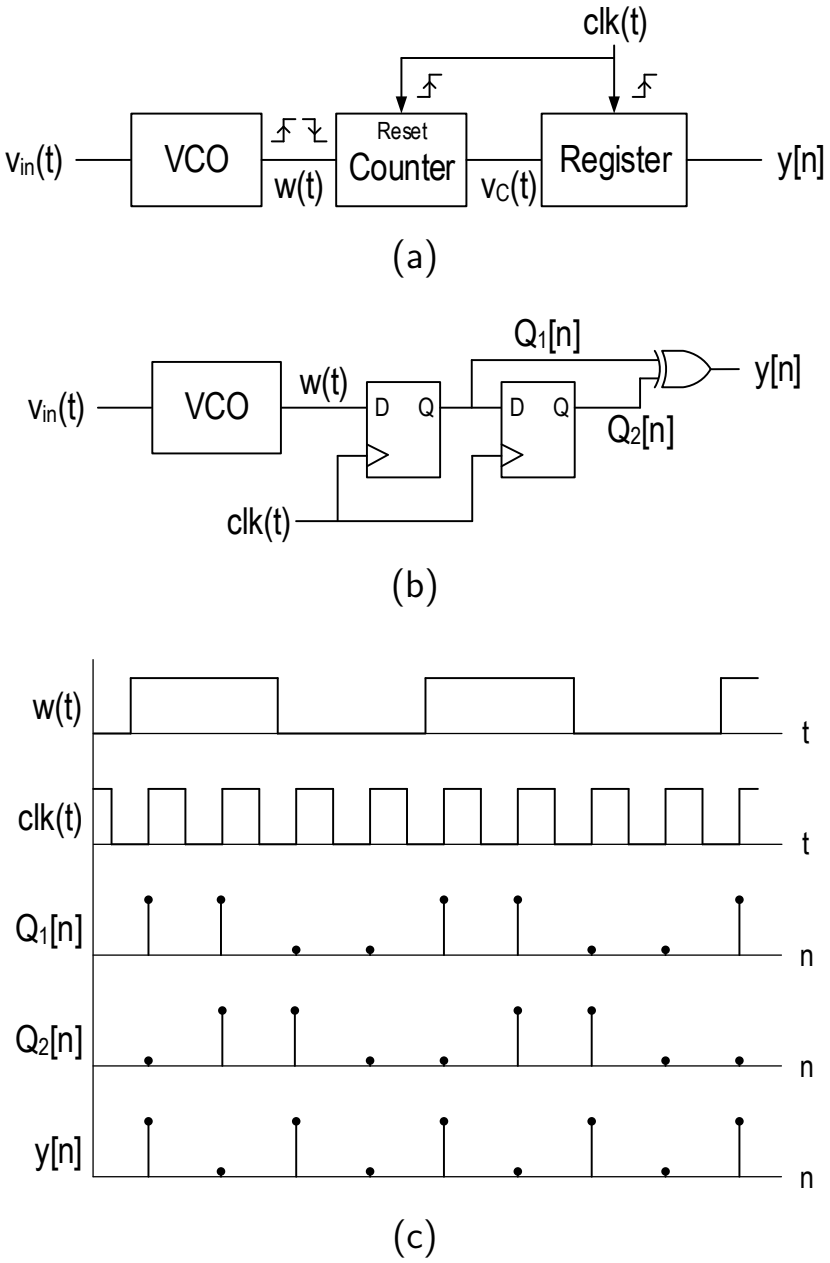


Figure 3.19: VCO-based first-order ΣΔ modulators using both-edges detectors. (a) Practical multi-bit implementation. (b) Single-bit XOR-based detector. (c) Operation of the XOR-based detector.

Nevertheless, phase resolution can be improved using multi-phase oscillators, whose output provide more information about its phase than

whether it is lower or higher than π radians. For example, a ring oscillator (RO) can have several square output from which the phase can be inferred with better precision. A voltage-controlled ring oscillator (VCRO) is composed of an odd number of inverting stages connected on a ring configuration, where the delay of each stage is controlled by the input voltage. Figure 3.20(a) depicts a 5-stage VCRO whose operation is illustrated in Figure 3.20(b). In this case, the phase quantization step is $2\pi/5$ radians if only on of the two edges are considered, and $\pi/5$ radians if both edges are taken into account (assuming a duty cycle of 50%). Figure 3.21 shows a generic multi-phase VCO-based ΣΔ, on which each of output (or "phase") of the oscillator is connected to a multi-phase frequency-to-digital converter. This F2D converter may consist of several single-phase counters or edge detectors whose outputs are added together.

3.4 High-order VCO-based ΣΔ modulators

High-order single-loop ΣΔ modulators typically consist of a series of integrators combined with a set of gains, feedback and forward branches, a sampler and a quantizer. These structures allow the reduction of quantization noise in the band of interest at the expense of complexity, power consumption, and silicon area. This section describes how VCOs and phase referenced integrators can be used to build part of high-order ΣΔ modulators.

3.4.1 VCO-based quantizers

As mentioned in Section 3.3, a VCO-Counter unit followed by a digital differentiator (or any of the practical implementations of this concept) digitalizes an analog signal with first-order noise shaping. This system can be used as a standalone converter, or can used as the quantizer of a higher-order modulator, as shown in Figure 3.22. In this subsection we enumerate three examples of the many high-order ΣΔ modulators with VCO-based quantizers reported in the last years.

Figure 3.23 shows the system proposed in [56], on which quantization

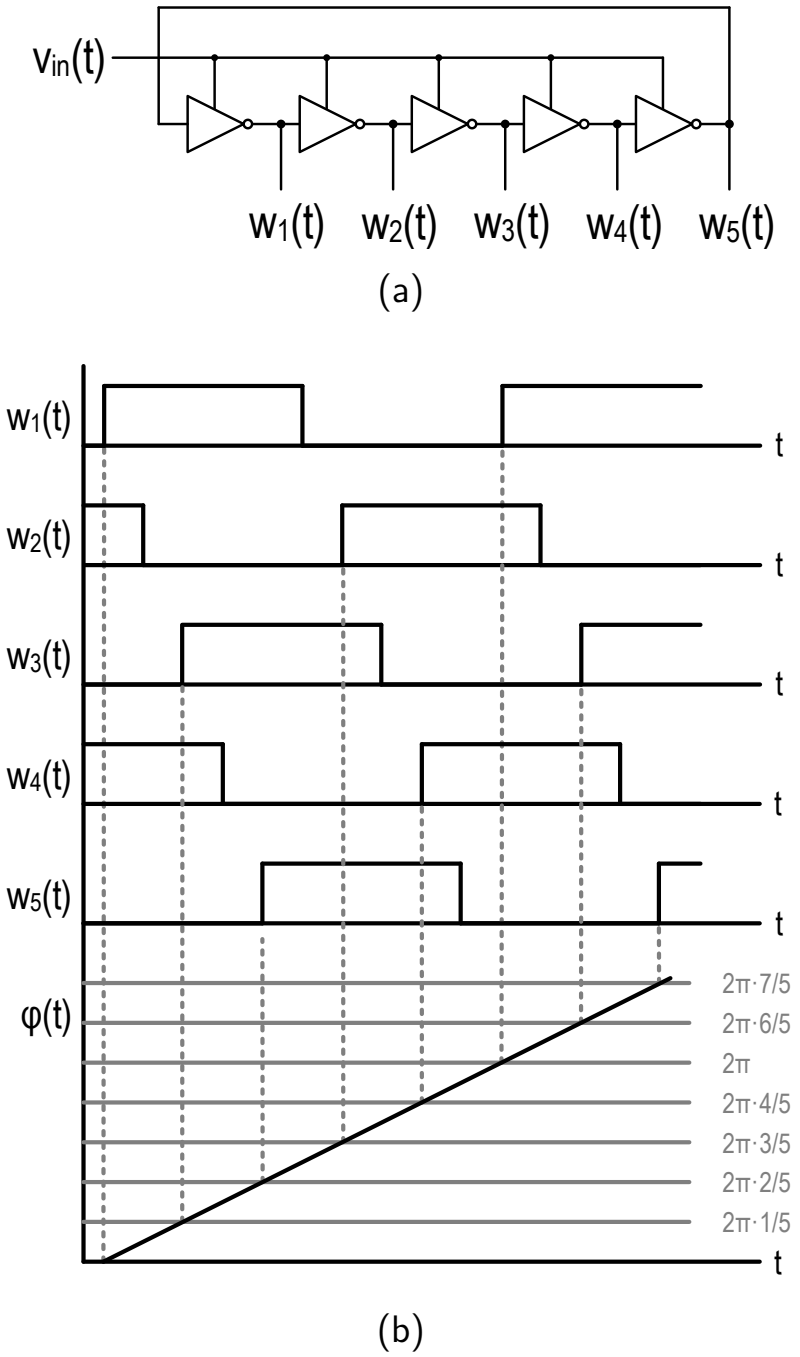


Figure 3.20: Circuit (a) and behavior description (b) of a 5-stage ring oscillator.

is performed by means of a VCO follows by a counter reseted by the sampling clock, like in Figure 3.17. An analog integrator is also part of the loop filter, which achieves second-order noise shaping.

The modulator proposed in [57] also shows second-order noise-shaper,

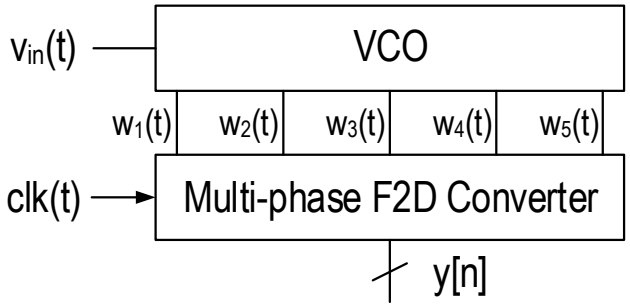


Figure 3.21: Generic multi-phase VCO-based modulator.

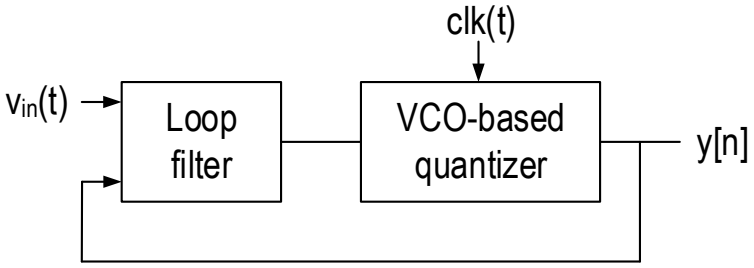


Figure 3.22: ΣΔ modulator with VCO-based quantizer.

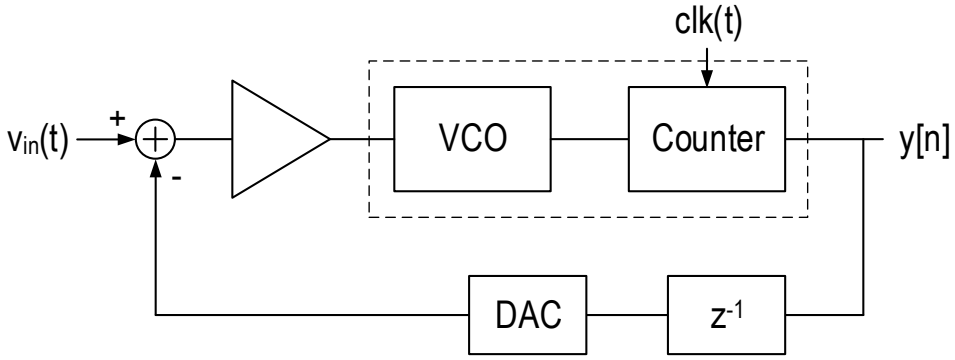


Figure 3.23: Second-order ΣΔ modulator with VCO-based quantizer [56].

but the VCO-based quantizer is not used as one of the integrators. Therefore, two classical integrators are required to obtained the desired order in the loop filter, as shown in Figure 3.24. An interesting feature of this implementation is that the feedback signal is not obtained from the output of the counter but from the oscillation frequency of the VCO, which is converted into a voltage by means of a frequency detector and a low-pass filter. This design decision was taken to avoid the need for static and dynamic element matching in the feedback DAC.

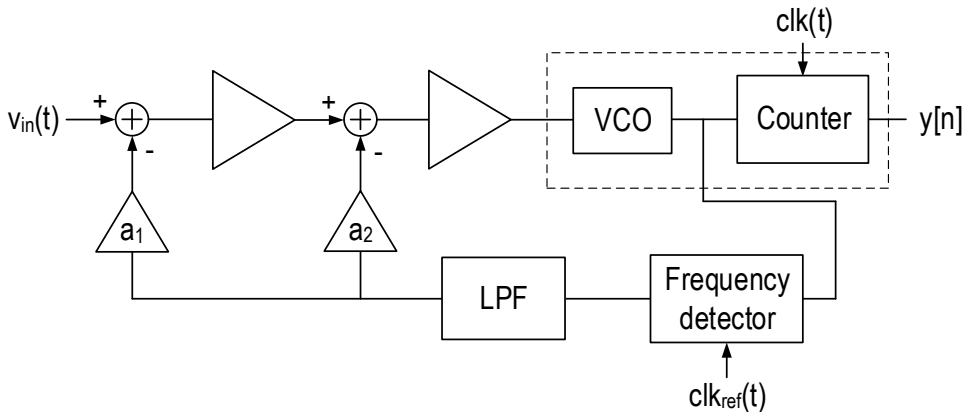


Figure 3.24: Second-order ΣΔ modulator with VCO-based quantizer and FM-based feedback [57].

Finally, [27] proposes a third-order VCO-based ΣΔ on which the three zeros of the NTF are provided by the front-end passive filter, the active integrator, and by the VCO-based quantizer. This quantizer is implemented using a 31-stage ring oscillator connected to multi-phase F2D converter, which is composed of 31 XOR-based edge detectors similar to the structures shown in Fig. 3.19(b). Moreover, the phase rotation of the ring oscillator is used to implement an implicit barrel-shift dynamic element matching (DEM) for the feedback DAC elements.

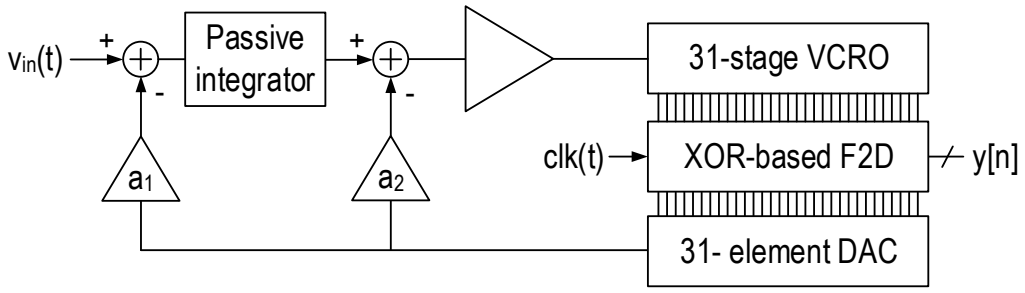


Figure 3.25: Third-order VCO-based ΣΔ modulator with implicit DEM implementation [27].

3.4.2 VCO-based loop filters

Classical integrators based on operational amplifiers have drawbacks such as elevated power consumption and silicon area occupation. Time-

encoding implementations are, in contrast, a promising alternative better suited for modern low-voltage and low-power applications. Consequently, in the last years, ΣΔ modulators on which VCOs are used also as main integrators of the loop filter have been reported [22, 47, 48, 58].

Figure 3.26 shows the architecture of a VCO-based ΣΔ modulator without analog integrators proposed in [47]. This architecture is one of the main contributions of this thesis, and is the basis for modulators proposed in chapters 4, 7 and 8. In this implementation, every analog integrator is replaced by a phase referenced integrator composed of an oscillator (VCO if it is driven in voltage and DCO if it is digitally-controlled) and a generic digital accumulator.

Later, in the prototype reported in [48], a similar architecture has been used to implement a third-order VCO-based ΣΔ modulator in 65 nm CMOS technology. Figure 3.27 shows system-level diagram, which is almost identical to the one of Fig. 3.26 except for the feedback coefficient g_{fb}. The practical implementation of this system is based on three 9-stage differential ring oscillators and three 9-element up-down counters, as shown in Figure 3.27(b). The first oscillator is controlled by the input voltage, whereas the other two oscillators are driven by current DACs controlled by the output of the digital counters.

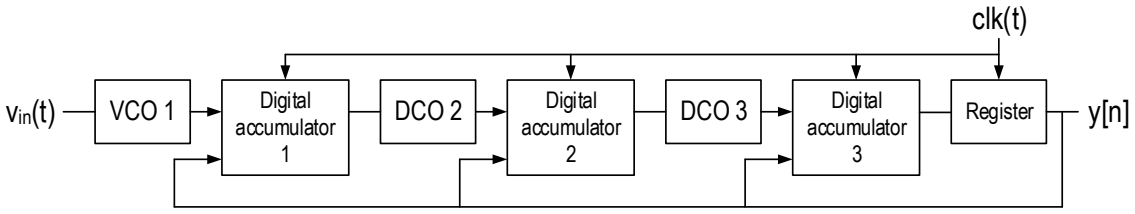


Figure 3.26: Architecture of a high-order VCO-based ΣΔ modulator proposed in [47].

Figure 3.28 depicts a different third-order VCO-based ΣΔ modulator, proposed in [22]. In this case, only two of the three integrators are based on oscillators, and the last stage consists of a classical integrator followed by a 4-bit flash ADC that performs the quantization. Each VCO-based integrator consists of two CCOs connected in a differential configuration, whose output is used in combination with a phase comparator to produce a pulse width modulated signal. Figure 3.28(b) shows the schematic of

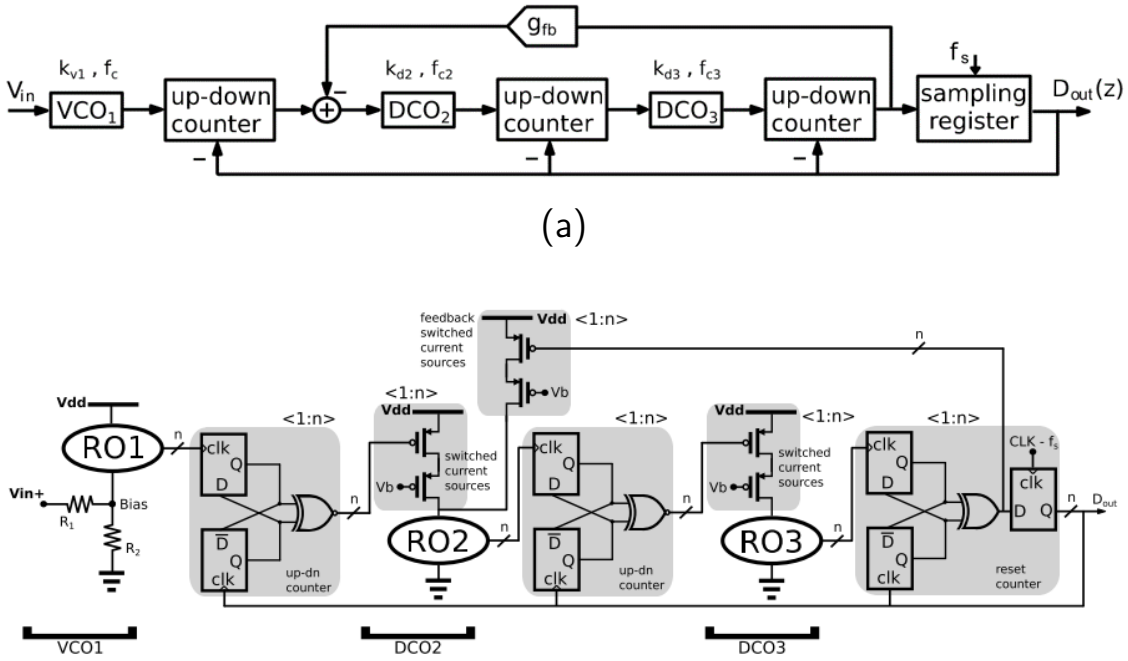


Figure 3.27: Third-order VCO-based ΣΔ converter reported in [48] (©2017 IEEE). (a) System-level diagram. (b) Schematic.

VCO1, on which both CCOs are interfaced using a transconductor stage.

3.5 Conclusion

The operation of ΣΔ modulators is based on integration, which is typically performed using classical analog integrators. Unfortunately, this kind of integrators do not benefit from technology scaling, and their implementation in modern CMOS technologies is not fully efficient. This chapter focuses on a different integrator topology based on frequency-encoding. A phase referenced integrator can be implemented combining a VCO (or any other oscillator) with digital circuitry. This alternative is scalable, and it is potentially more efficient than classical integrators in terms of power consumption and area.

The two main difference between classical integrators and PRIs are phase quantization noise and DC integration. Ideally, an analog integrator can provide an analog output without any kind of quantization.

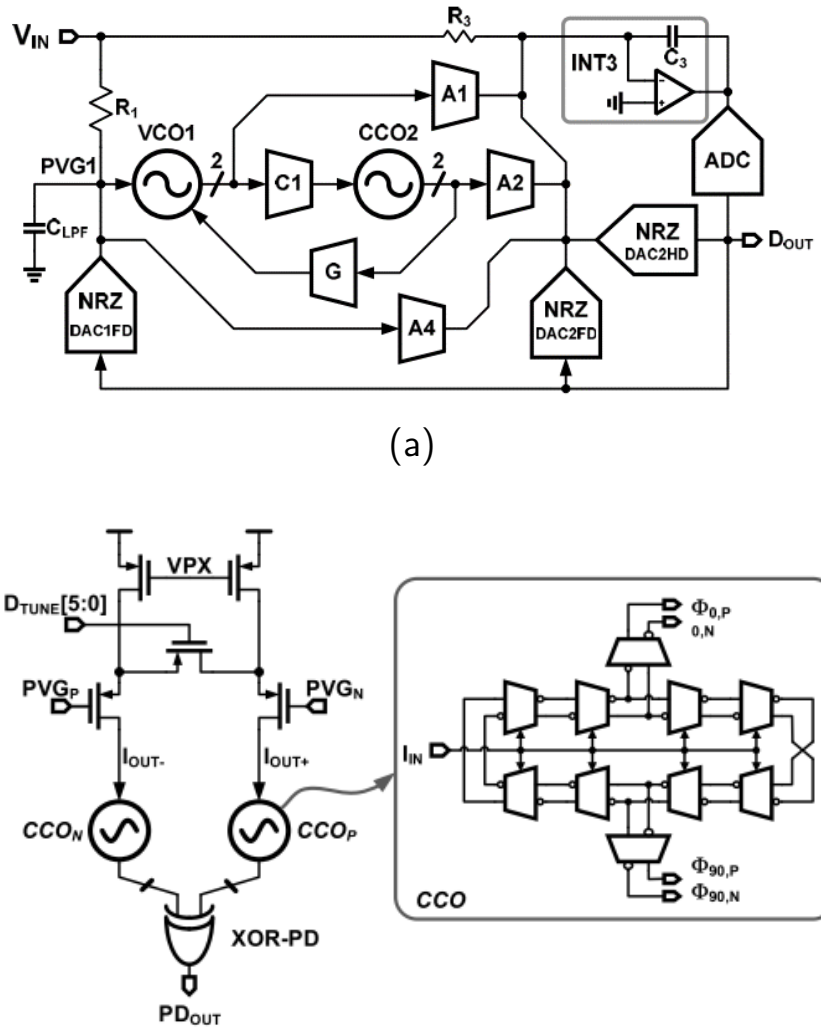


Figure 3.28: Third-order ΣΔ modulator using two VCO-based integrators presented in [22] (©2014 IEEE). (a) System-level diagram. (b) Schematic of VCO1.

In contrast, a phase referenced integrator typically add a certain phase quantization noise power given that the output of a PRI only provides limited information about the oscillator phase. On the other hand, a conventional integrator can integrate both positive and negative signals. However, given that the frequency of an oscillator cannot be negative, the output of a PRI would tend to increase indefinitely. Therefore, PRIs must include a mechanism to compensate the DC integration.

In this chapter we have studied the operation of phase referenced inte-

grators, including different practical implementations of ΣΔ modulators using PRIs. The studies presented in this chapter set the basis for the development of high-order oscillator-based ΣΔ modulators presented in Chapter 4.

CHAPTER 4

Design of high-order oscillator-based ΣΔ modulators

4.1 Introduction

In this chapter we focus on the development of high-order single-loop ΣΔ modulators using phase referenced integrators which, as described in Chapter 3, can be build combining oscillators and digital circuitry. This kind of implementations presents some advantages over classical analog integrators, specially in modern CMOS technologies. The work presented in this chapter is partially based on the material published in [47].

Firstly we take a generic n^{th}-order CT-ΣΔM as reference, and we replace the classical integrator of the first stage by a phase referenced integrator. In addition, we study how feedback DACs are not required in this approach, given that feedback integration can be performed in the digital domain. Different alternatives to implement the digital circuitry involved in phase referenced integration are analyzed. Then, we show the system level design of a second-order ΣΔ modulator implemented using only oscillator-based integrators, which is the basis for the two chips presented in chapters 7 and 8. Finally, we describe some of the circuit impairments that must be considered during the design of this

kind of systems, such as phase noise, clock jitter, or metastability.

4.2 Continuous-time and discrete-time feedback

Figure 4.1 shows the incomplete diagram of a generic n$^{\text{th}}$-order single-loop continuous-time ΣΔ modulator. The discontinuous line represents the additional $n-2$ stages required to build the converter. The feedback of this kind of modulators can be implemented using different types of DAC pulses such as NRZ DACs, return-to-zero (RZ) DACs, and switched-capacitor (SC) based DACs [3, 46, 59]. We have taken as a case study a modulator with NRZ DACs, which implies the use of a zero-order hold (ZOH) in the feedback path.

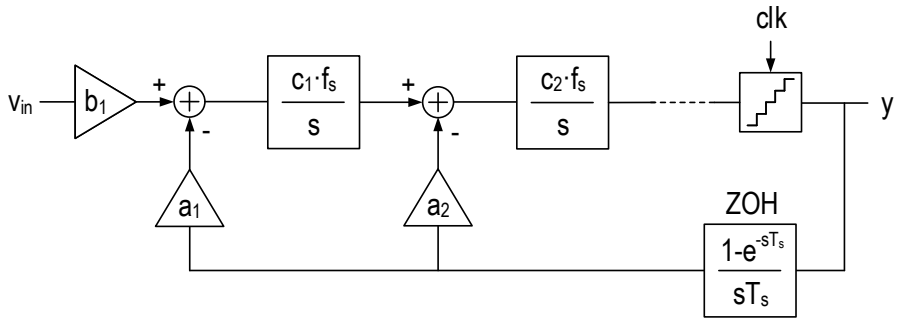


Figure 4.1: Diagram of a generic n$^{\text{th}}$-order continuous-time ΣΔ modulator with NRZ feedback DACs

As explained in Chapter 3, a continuous-time integrator can be replaced by a phase referenced integrator. Figure 4.2 illustrates how a system almost equivalent to the modulator of Figure 4.1 can be built using the PRI described in Figure 3.11, on which the DC compensation is performed using the sampling clock as the reference clock (i.e., $f_{ref} = f_s$). For the sack of completeness we have added a ZOH after the DC Compensation discrete-time integrator. In addition, g_{DAC_1} represents the gain of the DAC that should be connected after the PRI to generate a voltage (or a current) from the PRI digital code. Note that the resulting system is only equivalent to the reference modulator shown

in Figure 4.1 if the PRI-DAC gain is equal to the classical integrator gain, which implies:

$$K_{VCO} \cdot g_{DAC_1} = c_1 \cdot f_s. \tag{4.1}$$

Nevertheless, even if this condition is met, the PRI differs from the classical integrator in the addition of two error signals (the DC compensation error e_{DC} and and the phase quantization error e_φ), as explained in Section 3.2.1.

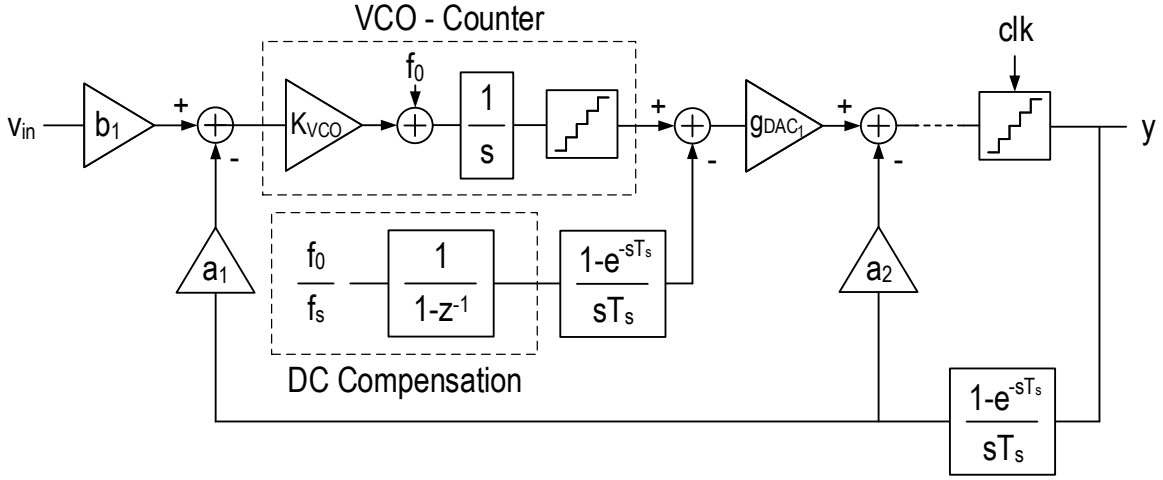


Figure 4.2: N$^{\text{th}}$-order continuous-time ΣΔ modulator with the first integrator implemented using a PRI.

This architecture may be more difficult to design if the first stage is implemented using a capacitance-controlled oscillators such as the ones described in Chapter 2. The challenge relies on designing an oscillator whose frequency can be controlled by both a capacitance and an electrical signal. This device could be implemented using a capacitance-controlled LC oscillator whose load is the combination of the capacitive sensor and a voltage-controlled capacitance [60]. Another alternative would be controlling both the capacitance and the charging and discharging current of a relaxation oscillator. An implementation suitable for resistive sensors have been published in [61].

Even if the first oscillator is not a sensor-controlled oscillator but a classical VCO, this architecture has a potential weakness due to the continuous-time feedback, specially in the first stage. Given that the

first DAC subtracts a signal at the input of the modulator, any error injected at this point is not filtered by the loop filter. Therefore, this DAC is very demanding in terms of noise and distortion, which implies more power consumption and silicon area. Moreover, given that the modulator chosen as example is implemented using NRZ DACs, any variation in the sampling period (i.e., jitter) injects additional noise at the input of the modulator.

Figure 4.3 shows an alternative implementation of the modulator shown in Figure 4.2 on which the feedback integration is performed in discrete-time, taking advantage of the discrete-time integrator used for the DC compensation. Note that the input coefficient b_1 has been integrated into the PRI for simplicity. Therefore, it must be true that

$$K_{VCO} \cdot g_{DAC_1} = b_1 \cdot c_1 \cdot f_s. \tag{4.2}$$

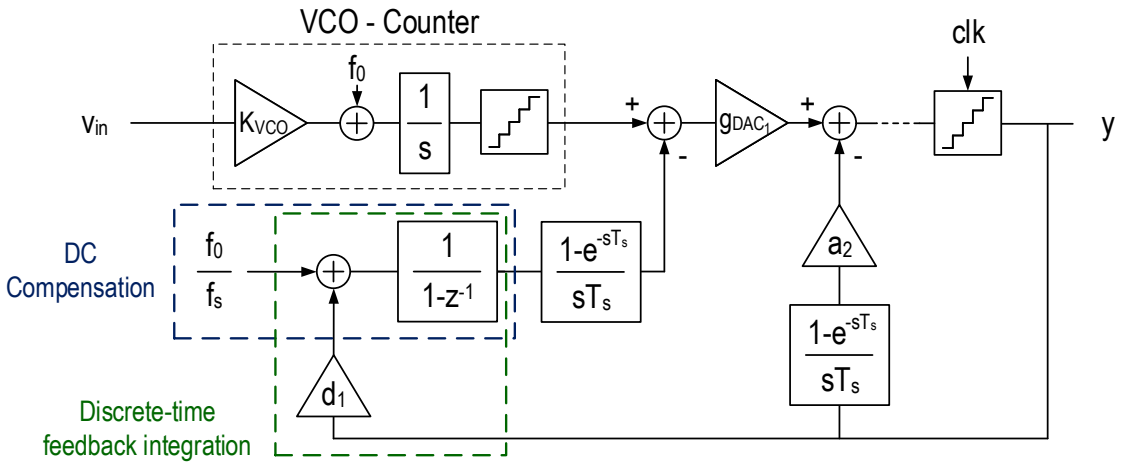


Figure 4.3: Alternative implementation of the system shown in Figure 4.2 using discrete-time feedback integration.

Moreover, in order to preserve the feedback gain and obtain a system equivalent to the reference modulator of Figure 4.1, the following condition must be accomplished:

$$d_1 \cdot f_s \cdot g_{DAC_1} = a_1 \cdot c_1 \cdot f_s. \tag{4.3}$$

This implementation has several advantages respect to the converter shown in Figure 4.2. On one hand, the feedback is subtracted in the

digital domain, without classical DACs that may require large silicon area and high power consumption. Moreover, since the feedback is not subtracted at the input of the oscillator, this architecture can be easily implemented using sensor-controlled oscillators like the ones described in Chapter 2. In addition, given that the feedback integration is performed in discrete-time, this topology is less sensitive to clock jitter. Nevertheless, this variant also shows some disadvantages respect to the continuous-time feedback integration of Figure 4.2. For example, given that in Figure 4.3 the oscillator is out of the feedback loop, the VCO distortion is not corrected by the loop and therefore it is visible in the output spectrum. Furthermore, the digital up-down counter becomes more complicated since the value that must be subtracted depends on the feedback signal. Indeed, given that the feedback value changes in the sampling instants, it is sometimes required to drive the discrete-time integrator using a delayed clock.

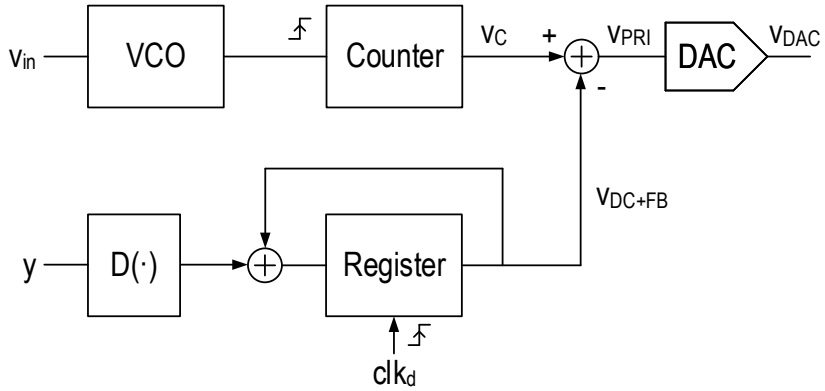


Figure 4.4: Phase referenced integrator including the feedback input and the output DAC.

Figure 4.4 shows an example of a PRI on which the register of the digital integrator is driven by signal a delayed clock clk_d. The function $D(\cdot)$ determines the relationship between the value subtracted to the PRI on the next clk_d rising edge and the output signal y. According to the feedback gain defined in Figure 4.3 (d_1), the feedback function of the first stage can be expressed as follows:

$$D_1(y) = D_1(0) + d_1 \cdot y. \tag{4.4}$$

As stated before, d_1 must satisfy equation (4.4). On the other hand, $D_1(0)$ should be equal to f_0/f_s in order to completely compensate the DC integration in the VCO. Nevertheless, $D_1(0)$ could differ from this value without degrading the performance of the system, as will be explained in Section 4.4. In any case, the selection of the parameters $D_1(0)$ and d_1 is restricted to values that produce integer numbers for any possible value of the output y, in order to obtain numbers compatible with the digital integrator. Indeed, for some of the PRI implementations that will be described in Section 4.3 we will restrict $D_1(y)$ to only positive integers and zero.

4.3 PRI-counter design alternatives

One of the main challenges during the implementation of phase referenced integrators is the design of the up-down counters. These counters generally have three input: the main oscillation, the clock, and the feedback. As explained before, its output is increased a constant value on each oscillation rising edge (w), and decreased a variable value on each clock rising edge (clk). The value subtract to the counter depends on the value of the feedback signal (y). Figure 4.5 depicts a theoretical up-down counter composed of two discrete-time integrators, three adders, and a the logic function $D(\cdot)$ that has been described in Section 4.2. This structure models the desired operation of the up-down counter as has been described before. However, it can not be used in a practical circuit given that both integrators grow indefinitely, so this circuit can not be implemented with a finite number of digital devices.

Figure 4.6 shows a potential workaround for this problem. In this implementation, both integrators are reset periodically, so signals v_C and v_{DC+FB} do not grow indefinitely. However, the integrators must be reset only when both output values are similar in order not to alter the PRI output. The register bus-width required to implement this structure must be estimated from extensive simulations of the complete system, given that the frequency on which both registers are reset depend on the ratio between the VCO frequency, the sampling frequency, and on several characteristics of the output signal y.

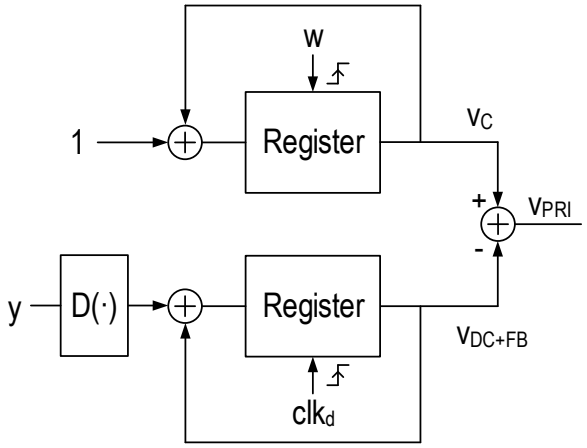


Figure 4.5: Theoretical up-down counter with variable decreasing value.

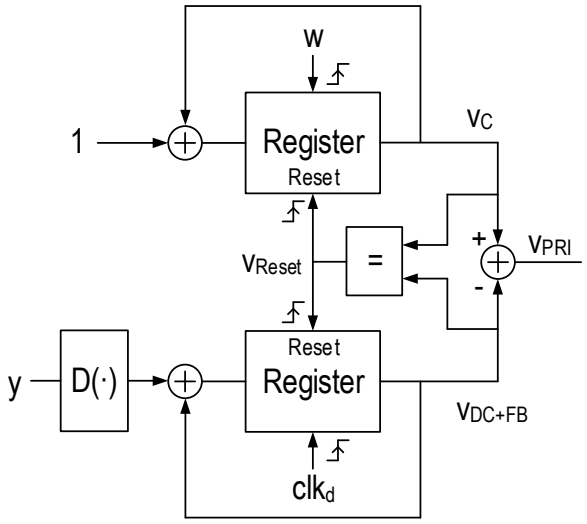


Figure 4.6: Up-down counter with reset logic to prevent saturation.

As shown in Figure 4.4, the up-down counter is sometimes connected to a DAC which generates the analog signal that drives the next stage. One of the most extended ways to implement a DAC is using an array of identical current sources (which can be individually switched on and off) connected in parallel. Therefore, the output current is ideally proportional to the number of elements switched on. However, the implementation of this structure in silicon suffers from element mismatch, what means that different elements provide different currents. This impairment degrades the performance of the system given that it affects the linearity of the DAC. Dynamic element matching is an effective technique to reduce the influence of element mismatch. A DEM algorithm

dynamically changes which elements are used to generate the output current for a certain input code. Data weighted averaging (DWA) is an example of a DEM implementation on which the current elements are cyclically used [62]. Figure 4.7 illustrates the operation of a DWA algorithm, where each square represents whether a current element is switched on (blue) or off (white). Each row corresponds to a different current element, and each column determines which current elements are enabled at a certain time instant. Figure 4.7(a) shows the operation of the DAC when DWA is not enabled, and the active elements are chosen using a thermometric code. In this case, a certain input code always switches on the same current elements, whose output current is constantly affected by mismatch. In contrast, Figure 4.7(b) illustrates the behavior of the DAC when DWA is active. In this case, the elements used chosen according to an algorithm that rotates which current sources are enabled, so a certain mismatch of one of the elements does not always affect the same input code. This results in the modulation of mismatch errors, reducing the impact of this impairment on the system performance.

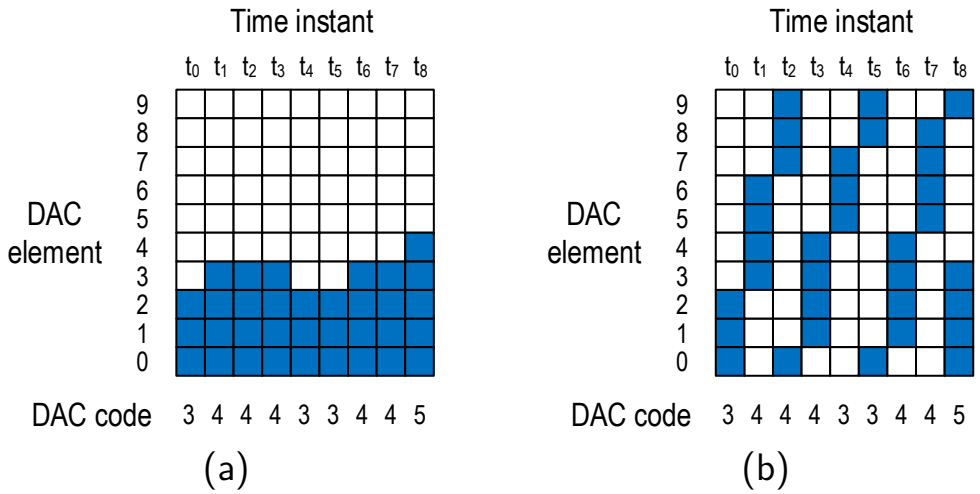


Figure 4.7: Active DAC elements for two different DAC approaches. (a) Without DWA, based on thermometric code. (b) Using a DWA algorithm.

This matching technique is inherently applied in the up-down counter depicted in Figure 4.8, which has been presented in [47]. This architec-

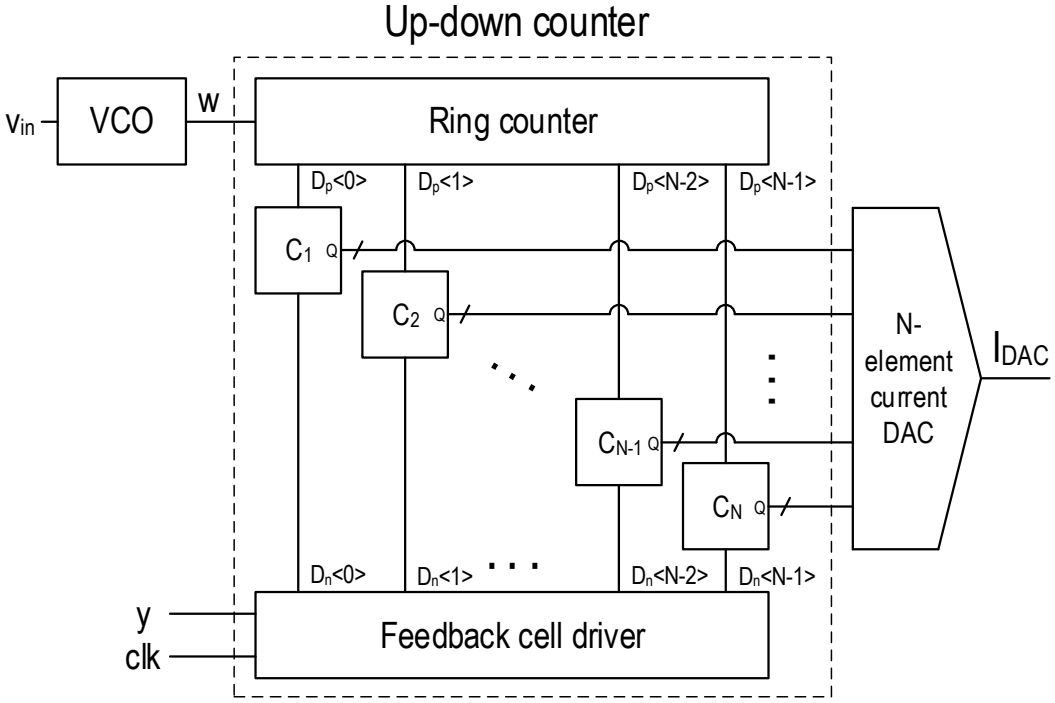


Figure 4.8: PRI wnith inherent DWA presented in [47].

ture consists of an N-stage ring counter, a feedback cell driver, and N element control cells.

The ring counter is driven by the PRI oscillator that integrates the input signal, and can be implemented as shown in Figure 4.9. If the circuit is properly initialized (e.g., reset during the system power-on), one half of the N outputs is '1' and the other half is '0'. Every time that the VCO generates a rising edge in w, one of the flip-flops changes from '1' to '0' (generating a falling edge) and another flip-flop commutates from '0' to '1' (i.e., it produces a rising edge). The position of these two edges moves forward along the ring on each VCO pulse.

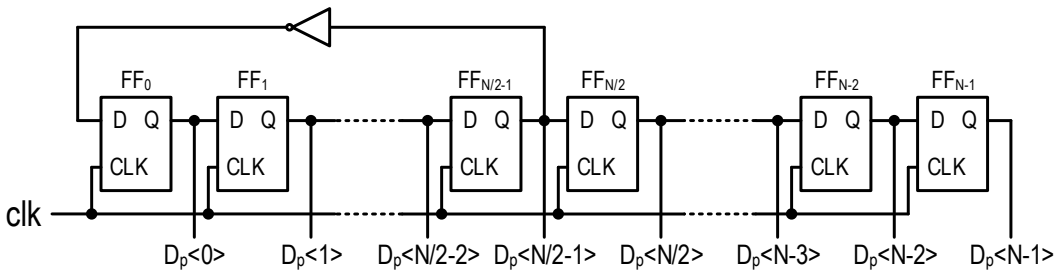


Figure 4.9: N-th stage ring counter.

Every rising edge produced by the ring counter triggers the positive input (D_p) of an element control cell. As shown in Figure 4.10(a), these cells have two inputs (D_p and D_n) and two outputs (Q_p and Q_n). A rising edge in any of the inputs sets to '1' a D-type flip-flop, who drives the correspondent output. However, when both outputs are high, both flip-flops are reset and the cell returns to its resting levels, as can be observed in Figure 4.10(b). Note that this structure is similar to the phase-frequency detectors frequently used in phase-locked loop (PLL) applications [63]. The operation of this kind of cells can be also described as a 2-bit up-down counter whose output is $Q_p - Q_n$. An analog output can be generated from this structure connecting in parallel several current elements like the one depicted in Figure 4.11 driven by the same amount of element control cells. Therefore, the total current provided by the DAC would be:

$$I_{DAC} = \sum_{j=0}^{N} i \cdot (Q_p\langle j\rangle - Q_n\langle j\rangle)\,. \tag{4.5}$$

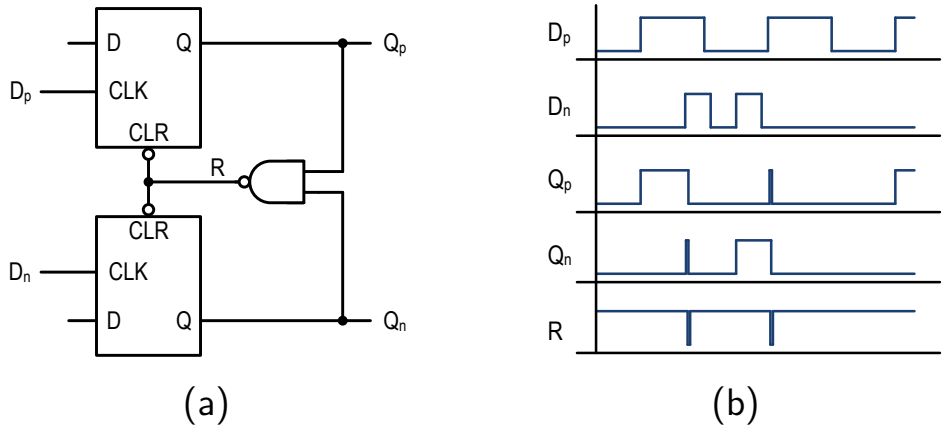


Figure 4.10: Element control cell with differential digital output. (a) Schematic. (b) Example of operation.

Concerning the feedback cell driver, we propose two different approaches. The first approach consists of a modulus counter whose value is incremented on $D(y)$ units each sampling edge. As shown in Figure 4.12, the counter output (p_k) is registered to also obtain the previous value of the counter (p_{k-1}). These two digital words are used as pointers to

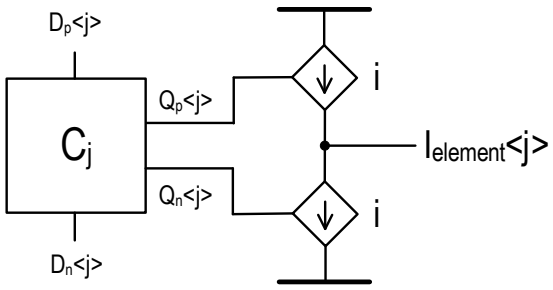


Figure 4.11: Connection between a DAC element and the control cell.

indicate which elements must be triggered each sampling instant. When the current pointer is higher than the previous pointer, only the cells whose position is between the two pointers are triggered. In contrast, when the previous pointer is higher than the current pointer it means that the modulus counter has overflowed, what implies that only the cells higher than previous pointer or lower than the current pointer must be triggered. Figure 4.13 illustrates the operation of the DAC including the value that pointers would take. This structure is very easy to implement since it can be synthesized using the available computer aided digital design tools.

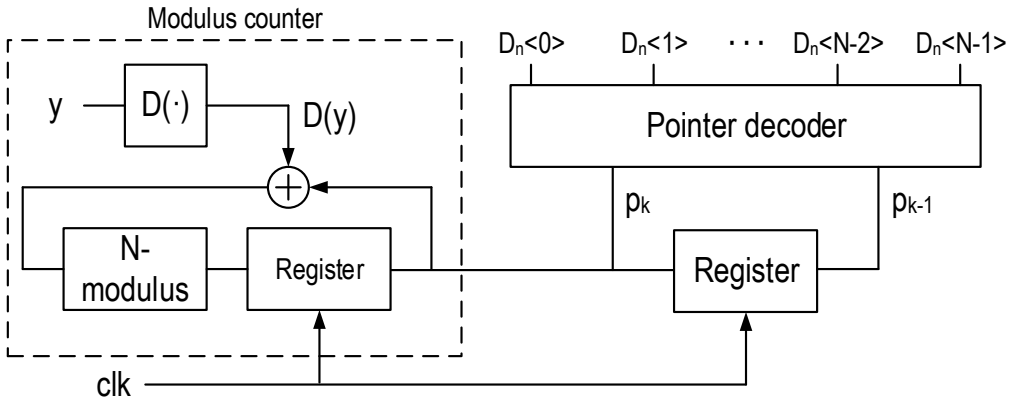


Figure 4.12: Feedback cell driver schematic.

However, the alternative approach depicted in Figure 4.14 may be more efficient in terms of area an power due to its simplicity and limited gate count. The proposed circuit is a modification of the classical ring counter shown in Figure 4.9. The main difference is that the data input of the D-type flip-flops comprising the counter are not by default connected to the previous flip-flop. Instead, multiplexers controlled by the

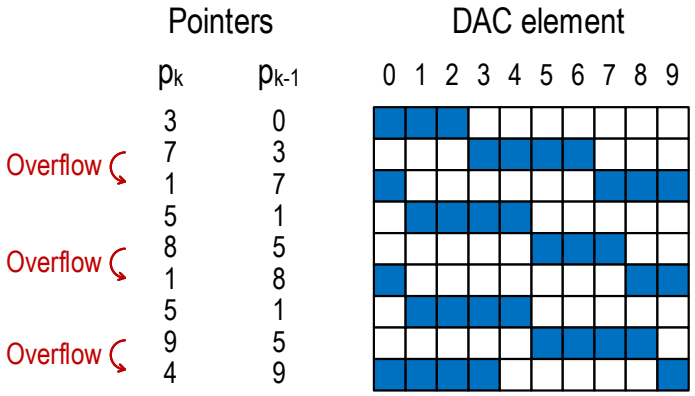


Figure 4.13: Feedback cell driver example of operation assuming N = 10.

feedback signal (y) determine to which point of the ring each flip-flop input is connected. In the example of Figure 4.14, when y equals '0' the multiplexer connects each flip-flop to the previous one, so counter operates as the original ring counter depicted. In contrast, when y equals '1', the input of each flip-flop is connected to the output of a flip-flop two positions back. Therefore, each sampling clock edge makes advance the ring counter value two positions instead of one.

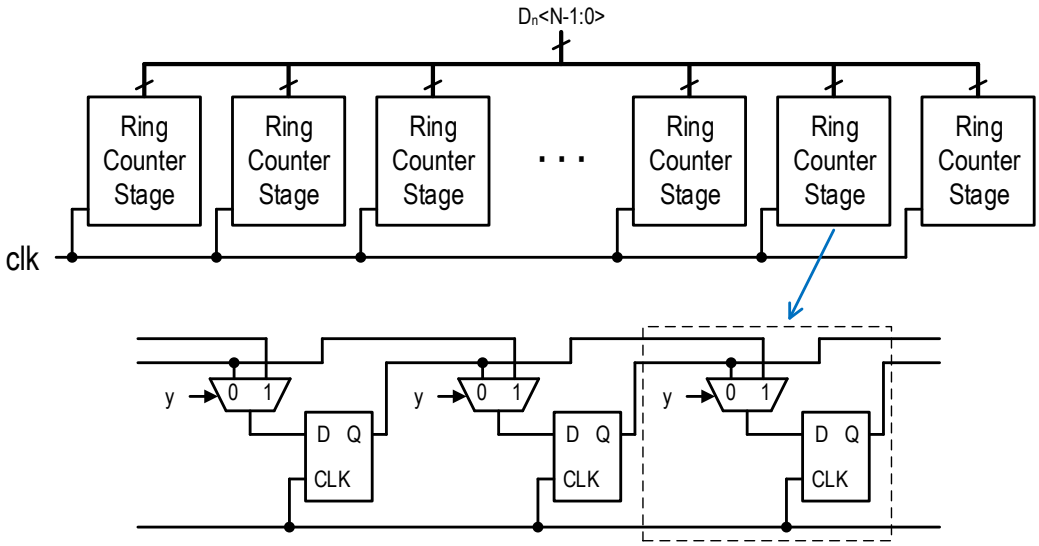


Figure 4.14: Alternative feedback cell driver based on a modified ring counter.

4.4 Oscillator-based second-order ΣΔ modulators

In this section we illustrate how a second-order ΣΔ modulators can be implemented using phase referenced integrators. Figure 4.15 depicts the block diagram of a classical second-order ΣΔ modulator with multi-bit quantizer. This system consist of two continuous-time integrators, a multi-bit quantizer whose gain is g_{Q1}, and two feedback loops. The feedback is performed through a zero order hold which models the operation of NRZ DACs. A delay of T_d has been included to model the potential synchronization delay of the DACs. The gains a_1, a_2, b_1, c_1, c_2, and g_{Q1} determine the shape and the gain of the system transfer functions. The STF is the transfer function from the input to the output of the modulator (which in this case must be flat or low-pass), whereas NTF is the transfer function from the noise injected in the quantizer to the output (which should be high-pass in order to minimize quantization noise within the band of interest).

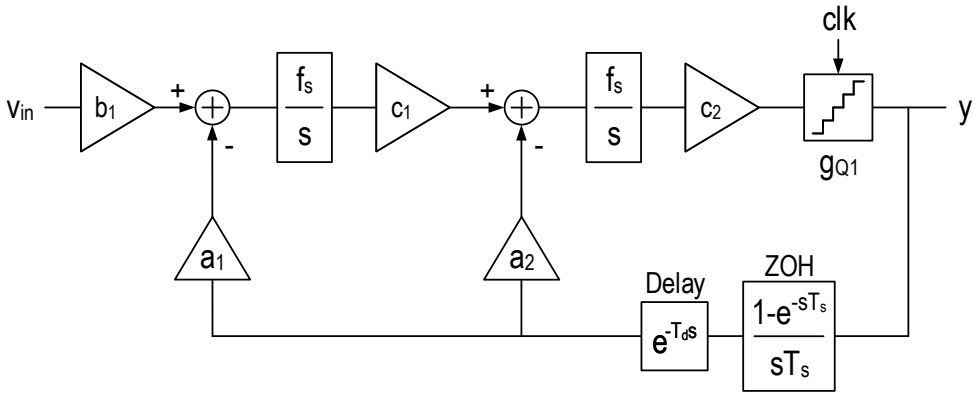


Figure 4.15: Classical second-order ΣΔ modulator with multi-bit quantizer taken as reference for this section.

An oscillator-based equivalent implementation of this system is shown in Figure 4.16. In this case, the continuous-time integration is performed using two phase referenced integrators, which are built around VCO1 and VCO2. The second oscillator can be considered as a digitally controlled oscillator (DCO), given that its driven by a DAC controlled by the digital

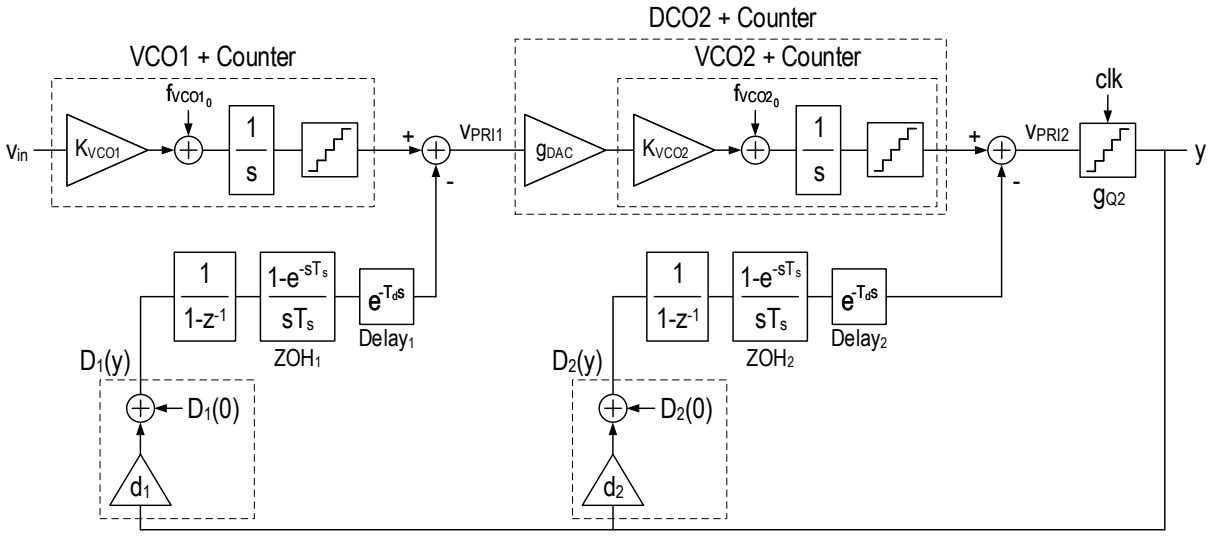


Figure 4.16: Oscillator-based second-order ΣΔ modulator.

output of PRI1 (V_{PRI1}). The DCO center frequency is $f_{DCO2_0} = f_{VCO2_0}$, and the DCO gain is $K_{DCO2} = g_{DAC} \cdot K_{VCO2}$.

Feedback integration has been implemented using discrete-time integrators as described in Sections 4.2 and 4.3. Note that the ZOH and the delay connected after the quantizer in Figure 4.15 have been replaced by two ZOH-delay pairs connected at the output of the discrete-time feedback integrator.

The resulting oscillator-based system is equivalent to the modulator of Fig. 4.15 only if the transfer function of every path is matched between both modulators. Firstly, the transfer function from the input port to the output of the modulator is match between modulators if

$$b_1 \cdot \left(\frac{f_s}{s}\right)^2 \cdot c_1 \cdot c_2 \cdot g_{Q1} = \frac{K_{VCO1} \cdot K_{DCO2}}{s^2} \cdot g_{Q2}, \tag{4.6}$$

where the first part of the equation is the signal path of the modulator shown in Fig. 4.15, and the second part is the corresponding transfer function of the oscillator-based converter of Fig. 4.16. Secondly, the transfer function of the outer feedback loop are matched if

$$-a_1 \cdot \left(\frac{f_s}{s}\right)^2 \cdot c_1 \cdot c_2 \cdot g_{Q1} = -d_1 \cdot \frac{f_s \cdot K_{DCO2}}{s^2} \cdot g_{Q2}, \tag{4.7}$$

assuming that the discrete-time integration is nearly equivalent to its

continuous-time counterpart. Under the same assumption, the matching of the inner feedback loop is conditioned to:

$$-a_2 \cdot \frac{f_s}{s} \cdot c_2 \cdot g_{Q1} = -d_2 \cdot \frac{f_s}{s} \cdot g_{Q2}. \tag{4.8}$$

In order to allow the implementation of the oscillator-based equivalent of Fig. 4.16 using any of the design alternatives proposed in Section 4.3, $D_1(y)$ and $D_2(y)$ must be integer values for any possible $y[n]$. Therefore, if $y[n]$ can only take integer values, d_1 and d_2 must also be restricted to integers. From equations (4.6), (4.7), and (4.8) we can derive the following expressions:

$$d_1 = \frac{a_1 \cdot c_1 \cdot c_2 \cdot f_s \cdot g_{Q1}}{K_{DCO2} \cdot g_{Q2}} = \frac{K_{VCO1} \cdot a_1}{f_s \cdot b_1}, \tag{4.9}$$

$$d_2 = \frac{a_2 \cdot c_2 \cdot g_{Q1}}{g_{Q2}}. \tag{4.10}$$

Moreover, assuming that $y[n]$ can be equal to zero, $D_1(0)$ and $D_(0)$ must also be an integer. If these conditions are met, $D_2(y)$ is always integer, and therefore $V_{PRI2}(t)$ can only take integer values. In consequence, the output quantizer can be replaced by a digital function that generates $y[n]$ depending on the value of V_{PRI2} sampled. Note that if $g_{Q2} = 1$, the output of the system is the result of sampling the output of PRI2, which is the simplest implementation possible.

Note that some of the implementations described in Section 4.3 are not compatible with negative feedback values. In these cases, $D_1(y)$ and $D_2(y)$ must be positive (or zero) for any possible value of $y[n]$. This condition can be achieved setting $D_1(0)$ and $D_2(0)$ as follows:

$$D_1(0) \geq max(y) \cdot d_1, \tag{4.11}$$

$$D_2(0) \geq max(y) \cdot d_2, \tag{4.12}$$

where $max(y)$ represents the maximum possible value of $y[n]$. However, these expressions may conflict with the description of the ideal DC compensation values provided in Section 3.2.1 (i.e., $D_1(0) = f_{VCO1_0}/f_s$ and

$D_2(0) = f_{VCO2_0}/f_s$). In consequence, the integration of the center frequency would not be completely counterbalanced by design, and the average value of some nodes of the system may be non-zero. On one hand, the center frequency of VCO1 is compensated through the outer feedback loop. In order to avoid the unrestrained growth of v_{PRI1}, the average value integrated by the oscillator must be equal to the average of the signal integrated by the discrete-time feedback integrator:

$$\overline{v_{in}} \cdot K_{VCO1} + f_{VCO1_0} = (\overline{y} \cdot d_1 + D_1(0)) \cdot f_s. \tag{4.13}$$

From this equation we can calculate the average value of the output sequence assuming that the average of the input signal is zero:

$$\overline{y} = \frac{f_{VCO1_0} - D_1(0) \cdot f_s}{d_1 \cdot f_s}. \tag{4.14}$$

On the other hand, the following expression describes the equilibrium condition for the second stage of the modulator:

$$\overline{v_{PRI1}} \cdot K_{DCO2} + f_{DCO2_0} = (\overline{y} \cdot d_2 + D_2(0)) \cdot f_s. \tag{4.15}$$

Given that the average of the output sequence is fixed by equation (4.14), the DC compensation of DCO2 is achieved through the adjustment of the average of v_{PRI1}:

$$\overline{v_{PRI1}} = \frac{(\overline{y} \cdot d_2 + D_2(0)) \cdot f_s - f_{DCO2_0}}{K_{DCO2}}. \tag{4.16}$$

In other words, the average oscillation frequency of DCO2 is

$$\overline{f_{DCO2}} = \overline{v_{PRI1}} \cdot K_{DCO2} + f_{DCO2_0} = (\overline{y} \cdot d_2 + D_2(0)) \cdot f_s. \tag{4.17}$$

Design example

A multi-bit second-order oscillator-based ΣΔ modulator has been designed following the procedures described in this chapter. We have taken as a reference the modulator depicted in Fig. 4.15, with the parameters specified in Table 4.1. Figure 4.17 shows the output spectrum obtained

from a behavioral simulation of the system applying a full-scale sinusoidal input signal at 1 kHz. The SNR calculated in the audio band (20 kHz) is 94.89 dB (100.78 dB-A).

Table 4.1: Parameters of the reference modulator used for the simulation of Fig. 4.17.

Parameter	Value	Parameter	Value	Parameter	Value
a_1	1	a_2	1	f_s	5 MHz
c_1	2/3	c_2	1	Quantization step	1 V
b_1	1	g_Q	1	Input full-scale	±0.9 V

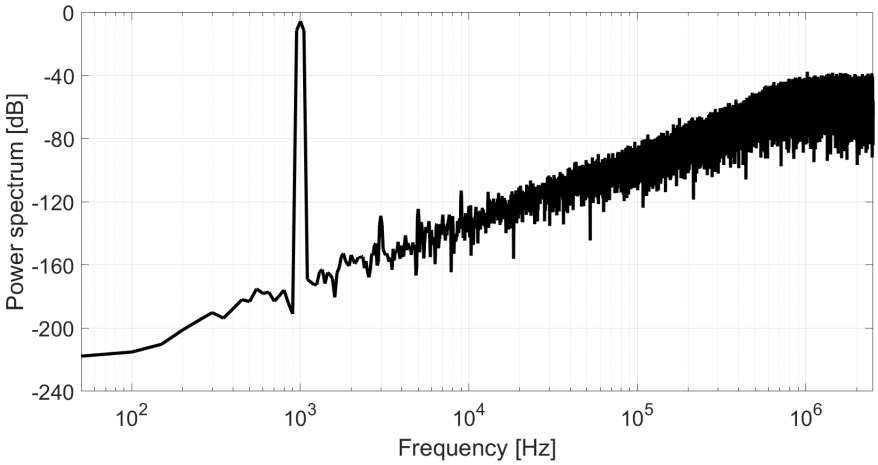


Figure 4.17: Simulated spectrum of the reference second-order CT-ΣΔ modulator.

From the parameters specified in Table 4.1 we can derive an oscillator-based equivalent using the equations presented in this chapter. Figure 4.18 depicts the resulting system, whose main parameters are summarized in Table 4.2. Note that the system of Fig. 4.18 does not require any kind of quantizer because the output of Up-down Counter 2 is a signal already quantized, given that it can only take integer values. Therefore, both the quantization step and the quantizer gain are equal to 1, i.e., similar to the same parameters of the reference modulator (see Table 4.1).

The gain d_2 has been calculated using equation (4.10). Note that the coefficients that influence d_2 have been properly chosen to obtain $d_2 = 1$

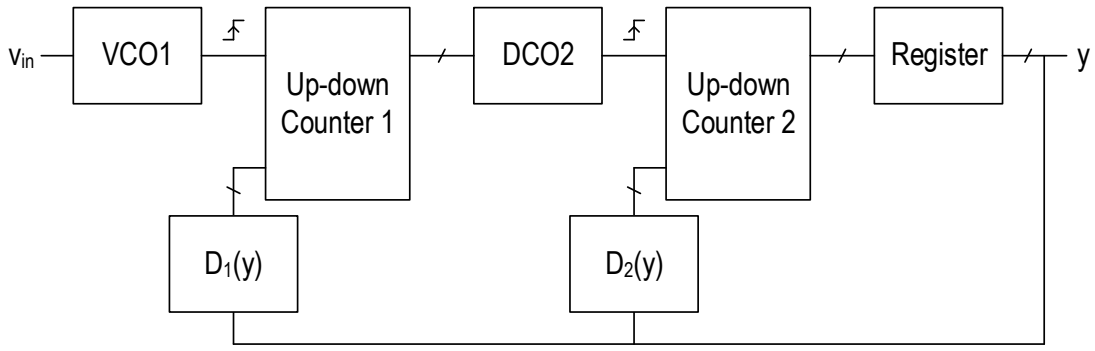


Figure 4.18: Simplified block diagram of the proposed second-order VCO-based ΣΔ modulator.

Table 4.2: Parameters of the proposed second-order VCO-based ΣΔ modulator.

Parameter	Value	Parameter	Value
K_{VCO1}	5 MHz/V	K_{DCO2}	3.33 MHz/code
f_{VCO1_0}	10 MHz	f_{DCO2_0}	6.66 MHz
$D_1(0)$	2	$D_2(0)$	2
d_1	1	d_2	1
f_s	5 MHz	g_{Q2}	1

what, as stated above, simplifies the implementation of the system. On the other hand, equation (4.9) describes the relationship between d_1, K_{VCO1}, and K_{DCO2}. Setting $d_1 = 1$ is a necessary condition to allow the implementation of the feedback integration using simple digital circuitry, which requires $D_1(y)$ to be an integer value for any possible y. Moreover, the resulting values for K_{VCO1} and K_{DCO2} are easily implementable with oscillators in the range of several MHz. The selection of f_{VCO1_0}, f_{DCO2_0}, $D_1(0)$, and $D_2(0)$, is an iterative process based on behavioral simulations. The parameters summarized in Table 4.2 avoid negative oscillation frequencies and negative feedback values, which would significantly complicate the implementation.

Figures 4.19 and 4.20 show the output of both PRIs obtained through a behavioral simulation, applying the same input tone as in Fig. 4.17 (i.e., a full-scale amplitude sinusoidal tone at 1 kHz). Figures 4.19(b) and

4.20(b) show the details of these waveforms, which consist of a combination of unitary rising steps and varying-sized falling steps. The size of the falling steps depend on the feedback signals, which can be described as follows:

$$D_1(y) = D_2(y) = y + 2. \tag{4.18}$$

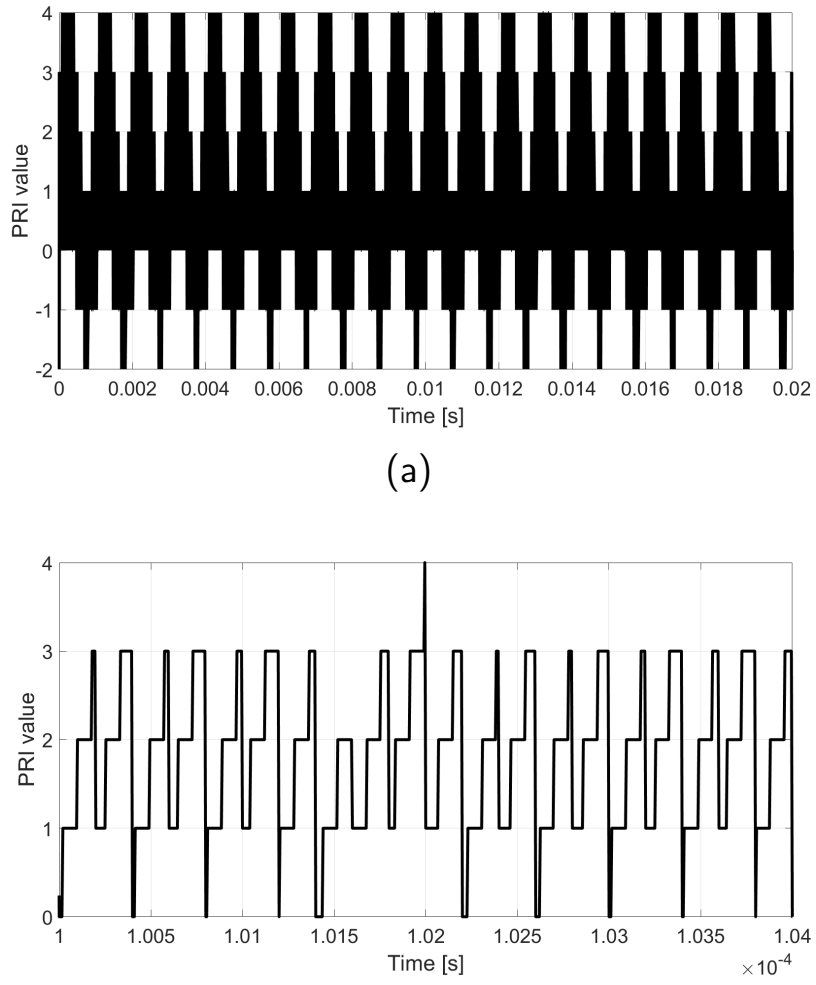
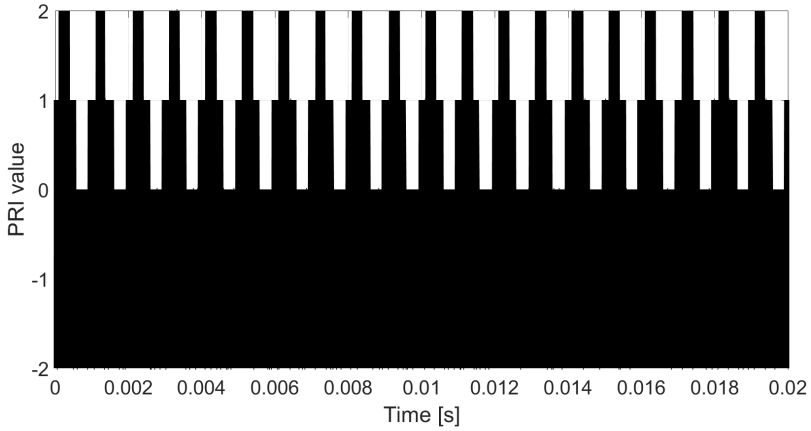
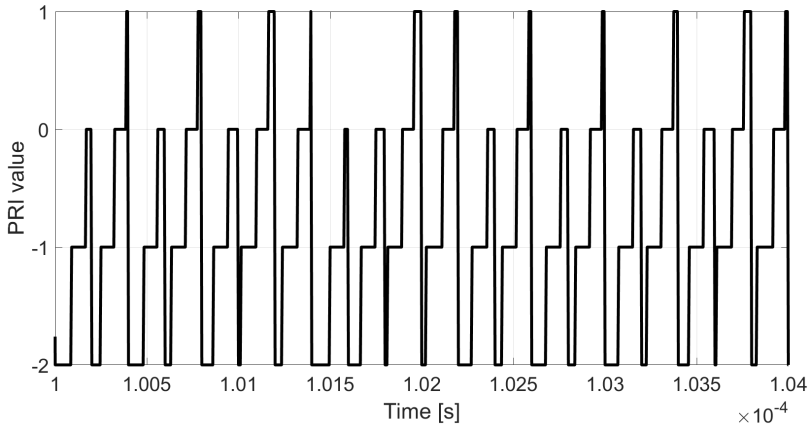


Figure 4.19: Simulated output of PRI1. (a) Full simulation. (b) Detailed view.

Figure 4.21 depicts the simulated oscillation frequencies of both oscillators over time. According to equation (4.14), the average of the output sequence is zero because the center frequency of VCO1 is perfectly counterbalanced by $D_1(0)$ (i.e., $f_{VCO1_0} = D_1(0) \cdot f_s$). In contrast, given that



(a)



(b)

Figure 4.20: Simulated output of PRI2. (a) Full simulation. (b) Detailed view.

$f_{DCO2_0} \neq D_2(0) \cdot f_s$), the average of v_{PRI1} is nonzero. According to equations (4.16) and (4.17), $\overline{v_{PRI1}} = 1$ and $\overline{f_{DCO2}} = 10$ MHz. These values match with simulation results.

Finally, Figure 4.22 shows a comparison between the output spectrum of the oscillator-based modulator and the spectrum of the reference modulator presented in Fig. 4.22. The SNR calculated from the spectrum of the oscillator-based equivalent is 95.52 dB (101.84 dB-A), which implies a deviation of approximately 1 dB respect to the SNR of the reference modulator.

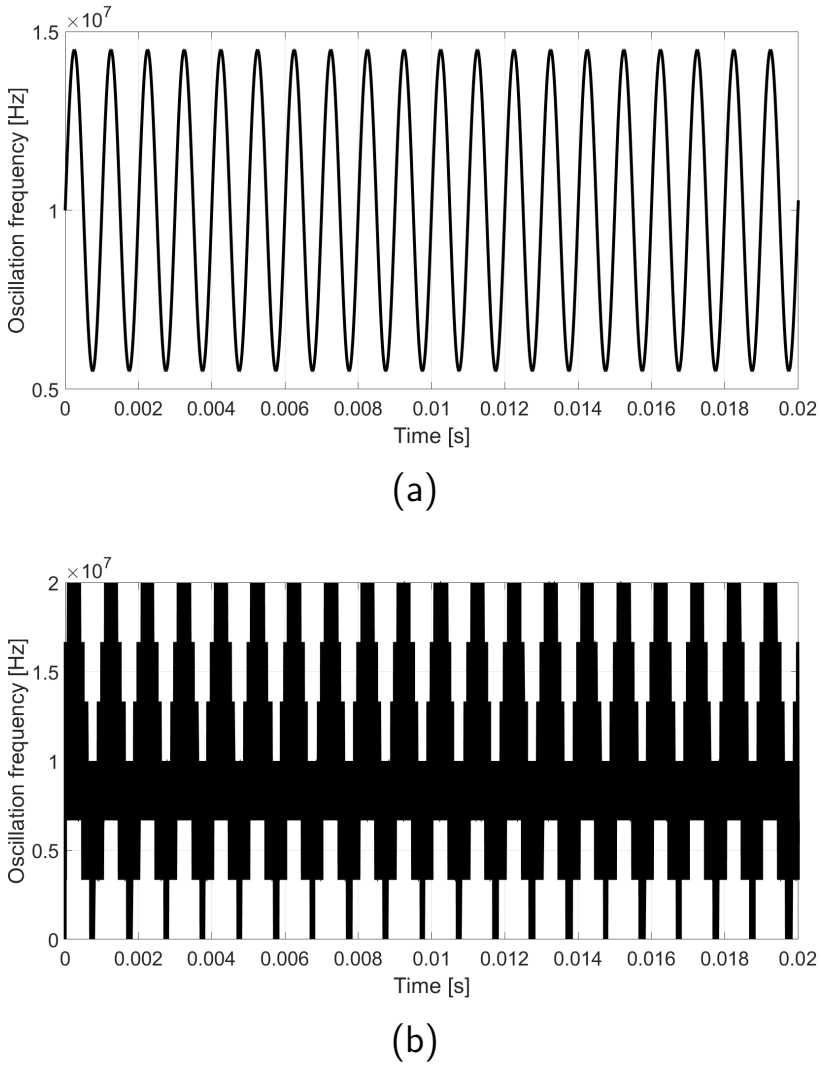


Figure 4.21: Simulated oscillation frequencies. (a) VCO1. (b) DCO2.

4.5 Design considerations for VCO-based modulators

As in the case of classical ΣΔ converters, any practical implementation of a VCO-based modulator involves the emergence of certain kind of problems that degrade the performance of the system. This section discusses some of the common issues that must be taken into account during the design of VCO-based converters.

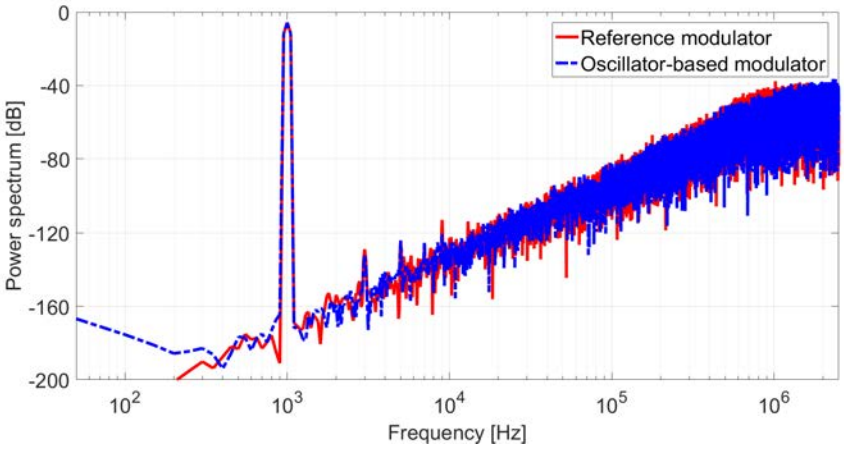


Figure 4.22: Simulated spectrum of the oscillator-based ΣΔ modulator compared to the output of the reference modulator.

4.5.1 VCO phase noise and distortion

The operation of VCO-ADCs is based on the voltage-to-frequency conversion performed by VCOs. Ideally, the relationship between voltage and frequency should be linear and deterministic, as stated in equation (3.4). However, the oscillation frequency of a real VCO is perturbed by two undesirable effects: phase noise and distortion [21]. The instantaneous phase of the oscillator can be defined as:

$$\varphi(t) = \int 2\pi\big(g(v_{in}(t)) + f_0\big)dt + \phi(t). \tag{4.19}$$

where function $g(\cdot)$ represents the nonlinear relationship between voltage and oscillation frequency, and $\phi(t)$ is the random phase fluctuation caused by electrical noise (i.e, phase noise). Therefore, a practical implementation of the first-order VCO-ADC of Fig. 3.15(d) can be modeled as shown in Figure 4.23(a). Figure 4.23(b) displays the output spectrum of the converter, which in addition to the components explained in Fig. 3.16 presents harmonic distortion (depicted in blue), and demodulated phase noise (depicted in green). Chapter 5 will present an in-depth discussion of the origins and influence of phase noise and distortion.

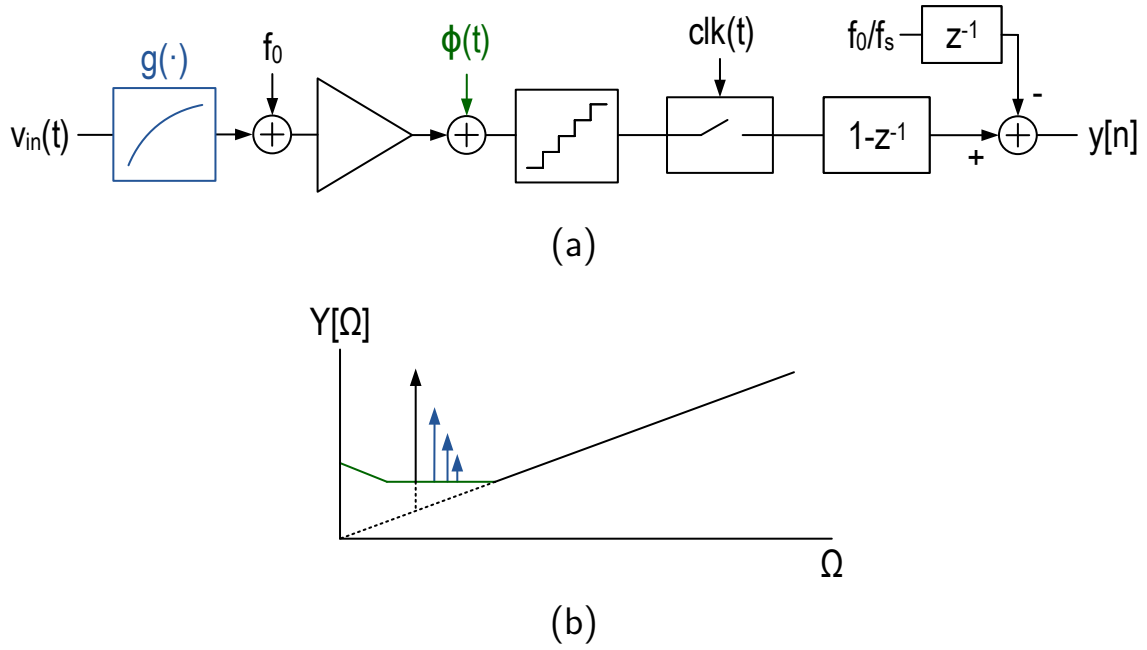


Figure 4.23: Influence of VCO phase noise (green) and distortion (blue) in the first-order VCO-ADC of Fig. 3.15(d). (a) System-level model. (b) Output spectrum.

4.5.2 Sampling clock jitter

The clock generator that synthesizes the oscillation that triggers the sampling of the system can be based on different oscillator topologies. This clock generator can be based on a free-running oscillator, or it can be synchronized with a reference oscillator, typically by means of a PLL. In any case, the oscillation is perturbed by electrical noise which randomly shifts the time instants on which clock edges are produced. Therefore, sampling period is not constant over time. This phenomenon is known as clock jitter and may degrade the performance of the system under certain circumstances.

Discrete-time ΣΔ modulators are typically implemented using SC circuits, on which charge exchanges between capacitors are performed abruptly, and the amount of charge transfered does not depend on the duration of the sampling period. In contrast, continuous-time ΣΔ converters implemented with classical integrators are very sensitive to jitter because the amount of charge integrated on one sampling cycle is directly

proportional to the duration of the period. Several works published in the last years have shown that the main contributor to SNR degradation due to clock jitter is typically the error injected in the feedback DAC of the first stage of the modulator [64–70].

In the case of VCO-based ADCs, jitter sensitivity is determined by the structure of the loop filter. For example, the system of Fig. 3.28 is similar to a continuous-time modulator because feedback is performed in continuous-time using NRZ DACs, whose pulse width depend on the sampling period. In contrast, the system proposed in Fig. 3.15(d) may show better tolerance to clock jitter because feedback is performed in discrete-time integration, as the equivalent model of Fig. 3.15(d) shows. Chapter 6 will provide more details about the influence of clock jitter in different modulator topologies.

4.5.3 Digital circuitry metastability and synchronization

Another typical source of problems in VCO-ADCs is related to the no synchronization of the different oscillating signals, such as the sampling clock and the output of VCOs.

On one hand, this situation may lead to metastability issues in the digital circuitry. A typical flip-flop is only stable when its output is in one of the two digital levels, '0' or '1', and any intermediate value is unstable and ends up converted into one of this two levels. However, a flip-flop only operates properly when certain timing conditions are met, and it can show a metastable behavior if any of these conditions are violated. Generally speaking, in the D-type flip-flop of Figure 4.24(a), the voltage level of the input D must be stable during a certain time interval prior and subsequent to each rising edge received through the clock input. Figure 4.24(b) illustrates possible reactions of a flip-flop to different time separations between the clock edge and a D-input variation. Note that some of these scenarios may be conflictive or not depending on the function of the output signal, which is typically sampled by others registers or directly used to control other devices (such as DACs).

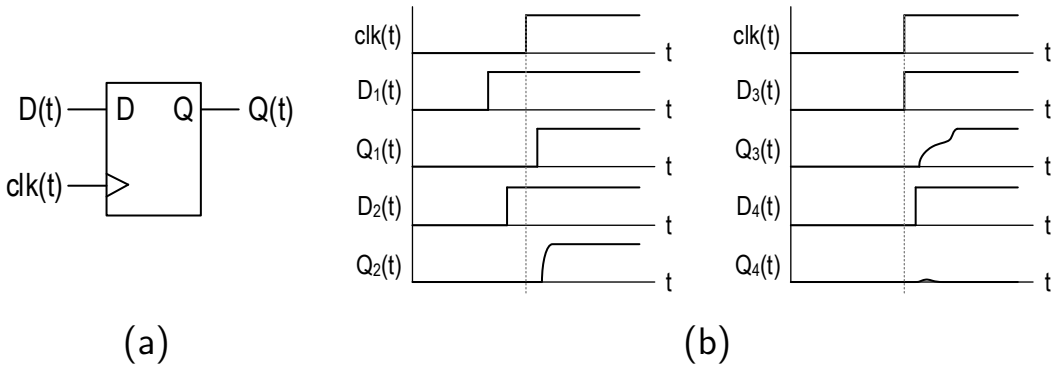


Figure 4.24: Example of metastability problems of a D-type flip-flop. (a) D-type flip-flop. (b) Possible outputs of this flip-flop in four different situations.

On the other hand, even if flip-flops do not suffer from metastability, synchronization can be a source of errors. For example, Figure 4.25(a) shows a section of a first-order VCO-based ADC similar to the one described in [19, 20]. This converter is based on a voltage-controlled ring oscillator the generates several oscillations, one of them (considered the "main phase") triggers a counter, and the rest of the phases are just sampled. Therefore, the output of the counter provides the number of full cycles occurred during the sampling period (i.e., the phase increment in steps of 2π radians), whereas the status of the other phases relative to the main phase can be used to improve the resolution of the phase increment, as explained in Section 3.3.3 (see Fig 3.20). However, the operation of this system may not be robust under certain conditions related to the synchronization between the sampling clock and the ring oscillator edges. Figure 4.25(b) shows different signals of this implementation, assuming a 5-stage ring oscillator. The rising edge of the main phase occurred at t_1 is followed by an increment on the value of the digital counter, which happens at t_2. This delay introduced by the counter $(t_2 - t_1)$ depends on the counter architecture, number of bits, and technology node. The problem arises when a sampling edge occurs during this time window, because the values received by the processing logic would lead to an error of -2π radians in the output of the converter. Note that compensating this delay introducing an intentional delay in

the path of the phase sampler is risky because temperature and process variations may difficult the proper matching between both delays.

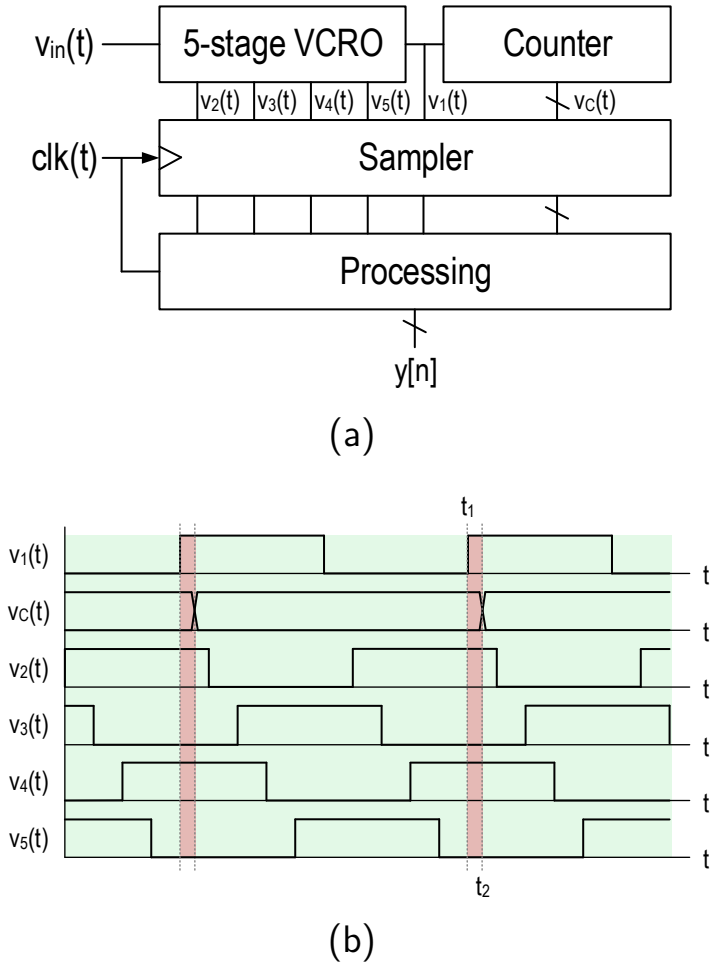


Figure 4.25: Example of a system sensitive to synchronization problems. (a) VCO-based converter. (b) Signal description with conflictive time-intervals highlighted in red.

These are just two examples among the wide variety of scenarios on which the asynchronous nature of VCOs oscillations may result in the injection of errors. In summary, metastability and synchronization errors are relevant sources of errors that must be considered in the design process. Most of these errors are unavoidable, and the designer can only minimize its probability and ensure that it is low enough to achieve the target performance.

4.5.4 Interferences and injection locking

In addition to the noise generated by the components that build up the oscillator, external signals can interfere with the normal operation of the oscillator and shift its phase or frequency. These interference signals can be originated in any other point of the same silicon die, or in any other system of the external world. Although these undesired signals can disturb the oscillator by other means (such as the bulk, air, or vacuum), the main mean of interferences is the electrical connection between the oscillator and the other circuits that build up the system.

We take as case study the differential system shown in Figure 4.26, which is used to illustrate different noise coupling mechanism that can degrade the performance of the VCO-based system. This modulator is based on the differential VCO shown in Figure 4.26(a), which has certain similarities with the VCO of [22] shown in Fig. 3.28(b). Its operation is based on two current-controlled ring oscillators driven by a differential transconductor, which is implemented using a source-degenerated PMOS differential pair. The phase of each oscillator can be disturbed through different mechanisms. On one hand, the output nodes w_p and w_n are typically connected to digital circuitry, whose fast transitions can inject charge to the oscillator internal capacitances. On the other hand, interferences can reach the CCO through the transconductor or the ground. As shown in Figure Fig. 4.26(a), a VCO is typically connected to a digital F2D converter (in some cases a level-shifter is required to adapt the voltage levels), and both subsystems share the same power supply network. Although voltage regulators (LDOs) are frequently used to generate different power supply domains, high-frequency noise can couple to the VCO if it is not properly filtered.

Injection locking is an special kind of interference that can take place when an oscillator is perturbed by a periodic signal whose frequency (or its harmonics) is close to the VCO oscillation frequency (or its harmonics). When this happens and there is a strong coupling mechanism between the VCO and the interference source, the VCO can become locked to the interference. In consequence, the VCO can stop reacting to small input voltage changes, and large input signal become affected

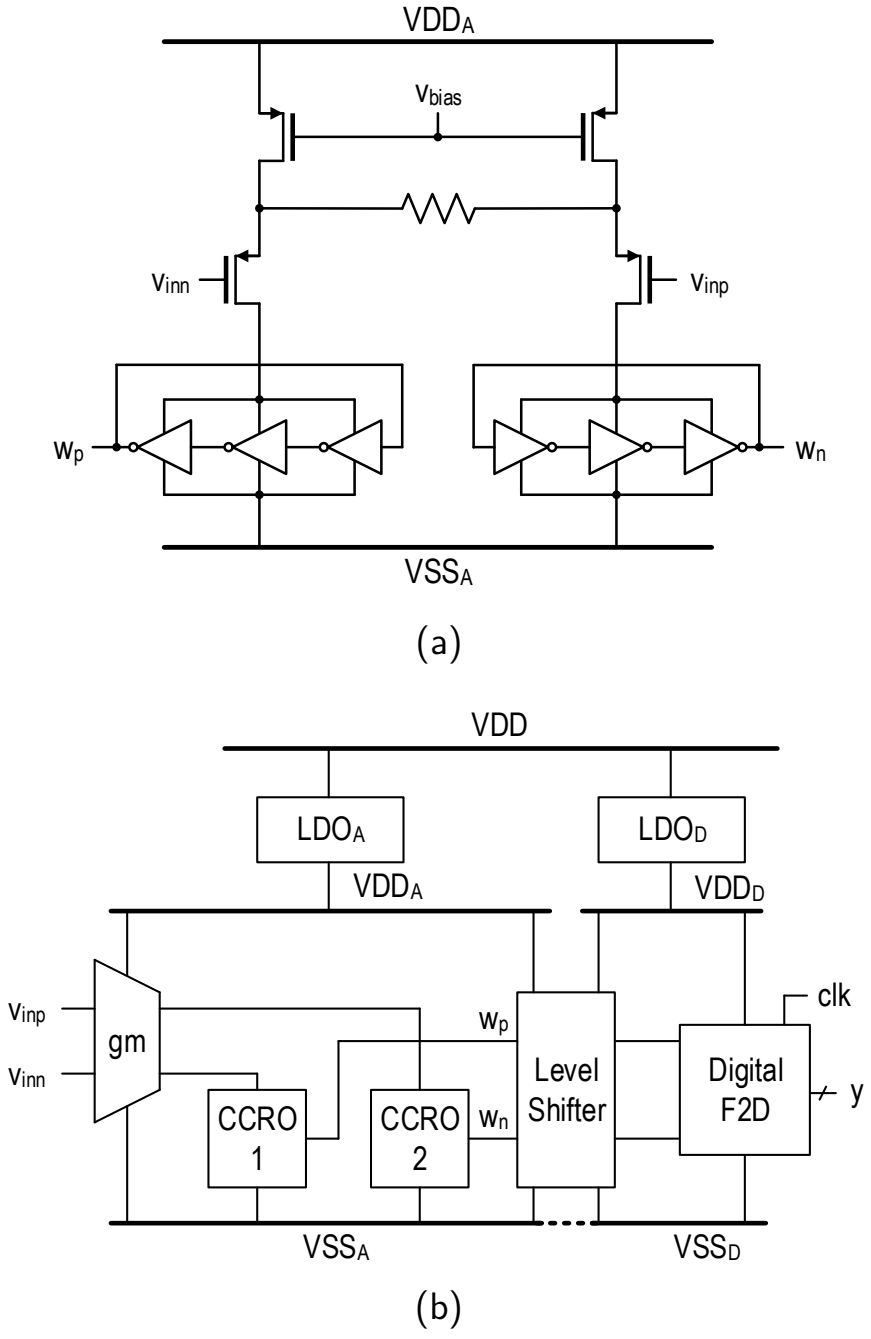


Figure 4.26: (a) Differential VCO composed of a transconductor and two CCOs. (b) Complete system including digital post-processing and power management.

by zero-crossing distortion. In the system of Fig. 4.26, the oscillation frequency of both CCOs are similar, and there are several strong coupling paths such as the ground connection, the transconductor resistance, and the supply node.

4.6 Conclusion

In this chapter we have applied the concepts presented in Chapter 3 to design high-order ΣΔ modulators implemented using oscillators, digital circuitry, and minimal analog circuitry. The resulting systems are potentially more efficient than classical ΣΔ modulators in terms of power consumption and area, specially in modern CMOS technologies. One of the main advantages of the proposed architecture is the elimination of feedback DACs, which typically consume a significant part of the total power and silicon area. In contrast, the proposed oscillator-based topology performs feedback integration using digital circuitry, which is an efficient alternative insensitive to circuit noise and clock jitter.

This chapter shows the procedure to transform a classical single-loop ΣΔ modulator into an oscillator-based ΣΔM, including the description of different PRI implementation variants and the main circuit impairments that degrade the performance of this kind of systems. This chapter is the basis for the two integrated circuits shown in chapters 7 and 8.

CHAPTER 5

SNDR limits of oscillator-based ADCs

5.1 Introduction

In this chapter we discuss the influence of phase noise and distortion in the performance of oscillator-based data acquisition systems. These two effects degrade the accuracy of the frequency-encoding process performed by the oscillator, that limits the maximum achievable SNDR of this kind of systems. We have taken VCO-based ADCs as case study, but the discussion presented in this chapter is valid for other oscillator topologies and applications.

The influence of phase noise in the performance of certain VCO-ADCs has been the focus of research during the last years [21,27,44,71]. In most of the cases, these works have studied phase noise in first-order noise-shaping VCO-ADC architectures like the ones described in Section 3.3 (see Figure 3.15(d)), which can be represented as shown in Figure 5.1. Phase quantization can be modeled as the addition of a quantization noise signal, which in most of the cases is assumed random (i.e., constant power spectral density) and independent from phase fluctuation due to circuit noise ($\phi(t)$). Both noise signals are sampled and high-pass filtered by the digital first-difference. Given that phase noise concentrates at

frequencies well below the sampling frequency, the effects of aliasing are typically negligible. Therefore, the influence of phase noise in the performance of this kind of systems can be estimated calculating the result of high-pass filtering phase fluctuations.

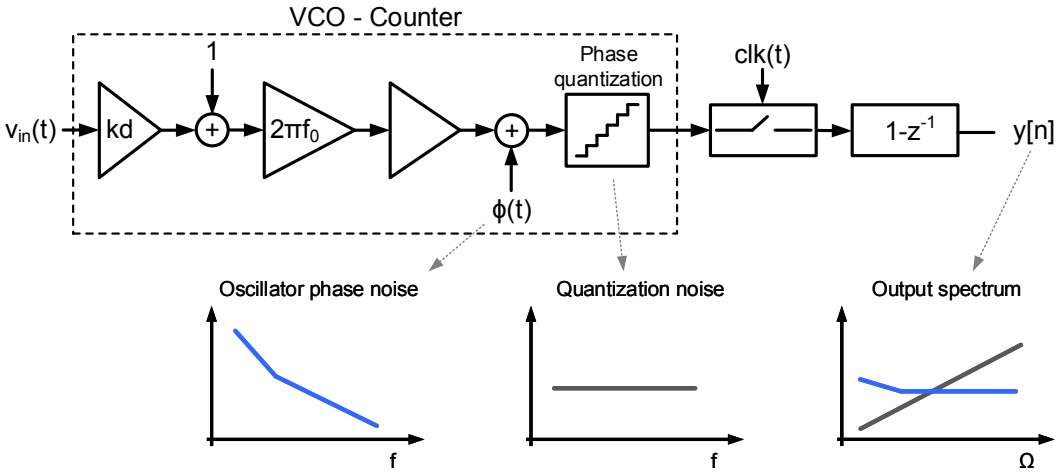


Figure 5.1: Classical approach to estimate the influence of phase noise in the performance of first-order VCO-ADCs.

However, this approach cannot be used to analyze other VCO-based modulators, like the high-order ΣΔM described in Chapter 4. Given that the VCO post-processing of this kind of systems is not based on the $1 - z^{-1}$ differentiation, the phase noise generated in the first oscillator cannot be evaluated taking the approaches available in the literature.

This work presents a different approach to analyze the influence of phase noise in the performance of oscillator-based systems. Rather than calculating how oscillator phase noise affects the output spectrum of the system, we propose to calculate the input referred noise equivalent which can be directly compared to the input signal. This allows the calculation of the SNR of any oscillator-based system, regardless of the post-processing applied.

In addition to phase noise, distortion may also limit the accuracy of the system for large input signals due to the nonlinear relationship between the input voltage and the oscillation frequency. This effect limits the dynamic range of the converter and plays an important role during the design of the VCO. As a main contribution, this chapter describes a simulation methodology that can reduce the simulation time

by orders of magnitude compared to noise enabled time domain simulations, yet keeping similar accuracy. This opens up the possibility to optimize the SNDR of oscillator-based systems by using iterative algorithms. The methodology presented in this chapter has been recently published in [72].

5.2 Phase noise

Ideally, the phase of a fixed-frequency oscillator should increase over time with a constant slope proportional to the oscillation frequency. However, electrical noise perturbs the voltages and currents of the circuit, which introduces random variations in the oscillator phase. These fluctuations are know as phase noise and limit the accuracy of the voltage-to-frequency conversion in VCOs.

5.2.1 Phase noise overview

Noise sources

In this section we focus on inherent noise, which is the noise generated by the components that build up the circuit [9], excluding interference noise which has been briefly described in Section 4.5.4. The two main sources of electrical noise relevant for most of the applications are thermal noise and flicker noise.

Thermal noise, also known as Johnson-Nyquist noise [73], is the consequence of the thermal excitation of charge carriers inside an electrical conductor. The spectral density of these perturbation is typically constant over frequency (i.e., it is white noise), and its power is proportional to the absolute temperature. Thermal noise is the main noise source in resistors, which can be modeled as a voltage source in series with a noise-free resistor, as shown in Figure 5.2(a). The PSD of this thermal noise is

$$V_{n\text{-}R}^2(f) = 4kTR, \tag{5.1}$$

where k is the Boltzmann constant, T is the absolute temperature in Kelvin, and R is the resistance in Ohms. Note that thermal noise is independent from the biasing of the resistor.

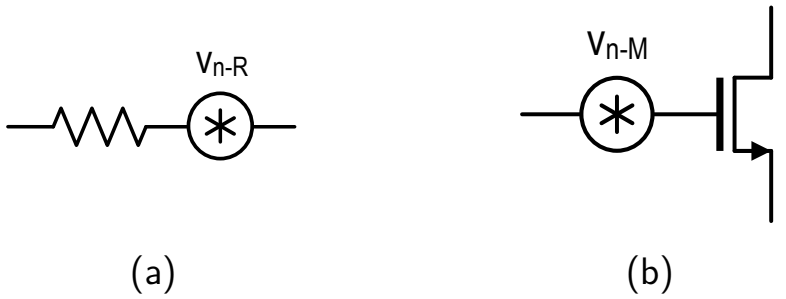


Figure 5.2: (a) Noise model of a resistor. (b) Noise model of a MOSFET.

MOS transistors also suffer from thermal noise. However, at low frequencies it is common that flicker noise (also known as 1/f noise due to its spectral density) dominates over thermal noise. Flicker noise depends on the biasing conditions of the transistor because its origin is related to the interaction between charge carriers moving across the semiconductor material [74]. The noise generated on a MOS transistor operating in active region can be modeled by means of a voltage source connected to the gate, as shown in Figure 5.2(b), whose spectral density is approximately [9]:

$$V^2_{n\text{-}M}(f) = V^2_{tn\text{-}M}(f) + V^2_{fn\text{-}M}(f) = 4kT\frac{2}{3}g_m + \frac{K}{WLC_{ox}f^{\alpha}}, \tag{5.2}$$

where g_m is the transistor transconductance, W and L are respectively its width and length, C_{ox} is the gate capacitance per unit area, α is a constant which in most of the cases is nearly 1, and K is a parameter that encompasses several fabrications and biasing details. Note that the first term of (5.2) represents thermal noise whereas the second one represents flicker noise. This expression is a simplification that does not reflect some interesting effects, such as the dependence between the current biasing and flicker noise power. One of the parameters commonly used to describe the noise present on a system is the corner frequency (f_c), which is the frequency above which thermal noise ($V_{tn\text{-}M}(f)$) dominates over flicker noise ($V_{fn\text{-}M}(f)$), as shown in Figure 5.3.

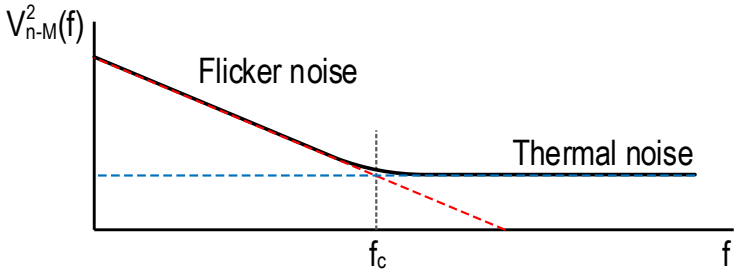


Figure 5.3: Typical noise spectral density in MOSFET devices.

Ciclostationary noise

The noise generated by the components that make up the oscillator is visible at the output modulated by the oscillation. This happens for two reasons: on one hand, the transfer function from the noise source to the oscillator output is time-variant and depends on the oscillation phase; on the other hand, the biasing of the components change over time, which causes the modulation of the biasing-dependent noise sources (e.g., flicker noise). As a result, in the spectrum of an autonomous oscillator circuit noise is concentrated around the fundamental component of the oscillation (and its odd harmonics in the case of an square oscillation), as shown in Figure 5.4. $S_w(f)$ is the single sideband (SSB) PSD of the oscillation $w(t)$.

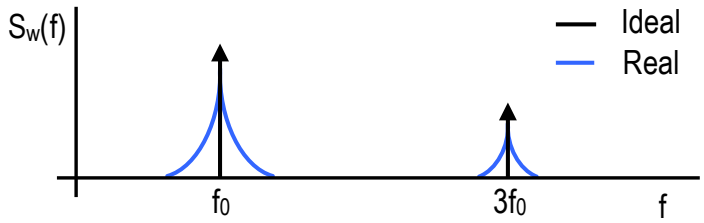


Figure 5.4: Effects of circuit noise in the PSD of an autonomous oscillator with square output.

Figure 5.5 shows the PSD of the oscillation close to the first harmonic, which can be divided between the lower sideband (LSB) and upper sideband (USB). The correlation between both sidebands determines whether noise perturbs the amplitude or the phase of the oscillation [75, 76]. Figure 5.6 illustrates this fact with two examples of

different type of correlations between two components ($S_w(f_0+\Delta f)$ and $S_w(f_0-\Delta f)$) respect to the fundamental tone ($S_w(f_0)$). Assuming that $S_w(f0+\Delta f) \ll S_w(f0)$, the correlation shown in Figure 5.6(a) implies the phase modulation (PM) of the oscillation, given that the combination of the two noise components is perpendicular to the fundamental component. In contrast, Figure 5.6(b) shows an example of amplitude modulation (AM).

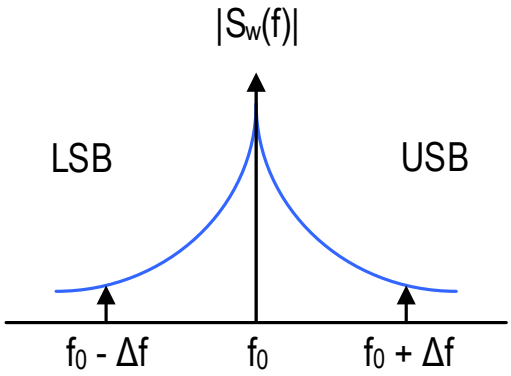


Figure 5.5: Typical PSD of an autonomous oscillator close to the center frequency.

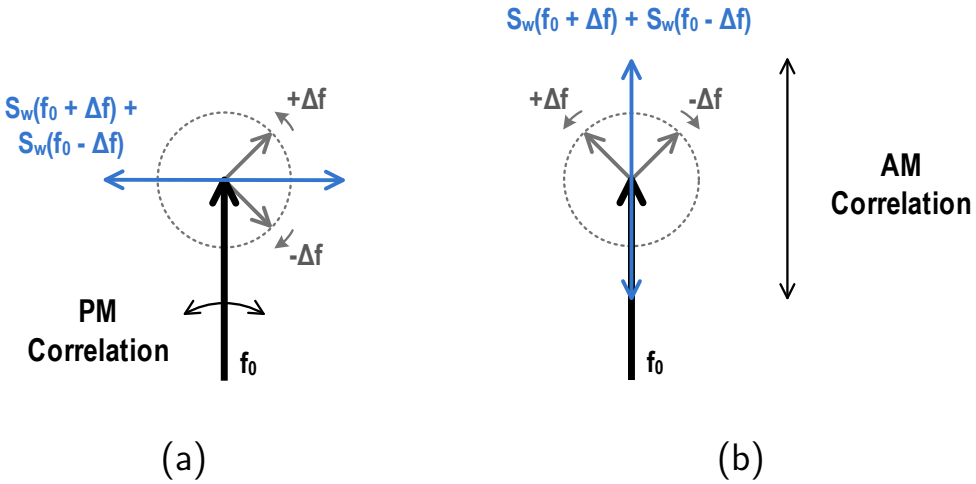


Figure 5.6: Two possible types of noise correlation LSB and USB. (a) PM correlation. (b) AM correlation.

The sideband correlation depends on the oscillator topology. In VCO-ADC applications, the oscillation is typically a square signal that can

properly drive the digital circuitry that follows the VCO. This is done either by selecting a VCO topology which produces an square signal, or by passing a non-square oscillation through an amplitude limiter. In any case, amplitude noise is suppressed and the oscillator mainly exhibits PM noise, at least at the frequencies of interest.

Phase noise

According to the IEEE standard [77], the phase fluctuation is denoted by $\phi(t)$, and it is given in radians. The one-sided PSD of the phase fluctuations is denoted by $S_\phi(\Delta f)$, and it is given in rad^2/Hz. The phase noise of an oscillator is denoted by $\mathcal{L}(\Delta f)$ and it is defined in [77] as

$$\mathcal{L}(\Delta f) \equiv \frac{1}{2} S_\phi(\Delta f). \tag{5.3}$$

This is a redefinition of the historical formulation of $\mathcal{L}(\Delta f)$, which was defined as the PSD in one phase noise modulation sideband normalized to the fundamental tone power:

$$\mathcal{L}(\Delta f) = \frac{S_w(f_0 + \Delta f)}{P_{\text{carrier}}}, \tag{5.4}$$

where, as previously stated, $S_w(f_0 + \Delta f)$ is the single sideband (SSB) PSD of the oscillation due to PM noise around f_0 (this is what a simple spectrum analyzer measures in the absence of AM noise). $P_{carrier}$ is the total signal power around f_0, which is also equivalent to the power of the fundamental harmonic of the noiseless oscillation. Definitions (5.3) and (5.4) are approximately equivalent for low phase fluctuations, but they differ at low offset frequencies.

The PSD of the phase fluctuations was firstly described by David B. Leeson [45, 78]. Nowadays [77], $S_\phi(\Delta f)$ (or $2\mathcal{L}(f)$) is commonly presented as shown in Fig. 5.7(a), assuming negligible AM noise as stated before. The span of each region depends on many parameters such as oscillation frequency, the oscillator topology and its quality factor. Note that $S_\phi(\Delta f)$ tends to infinity as Δf tends to zero. In the very low offset frequencies region, (5.3) and (5.4) are not compatible because it would

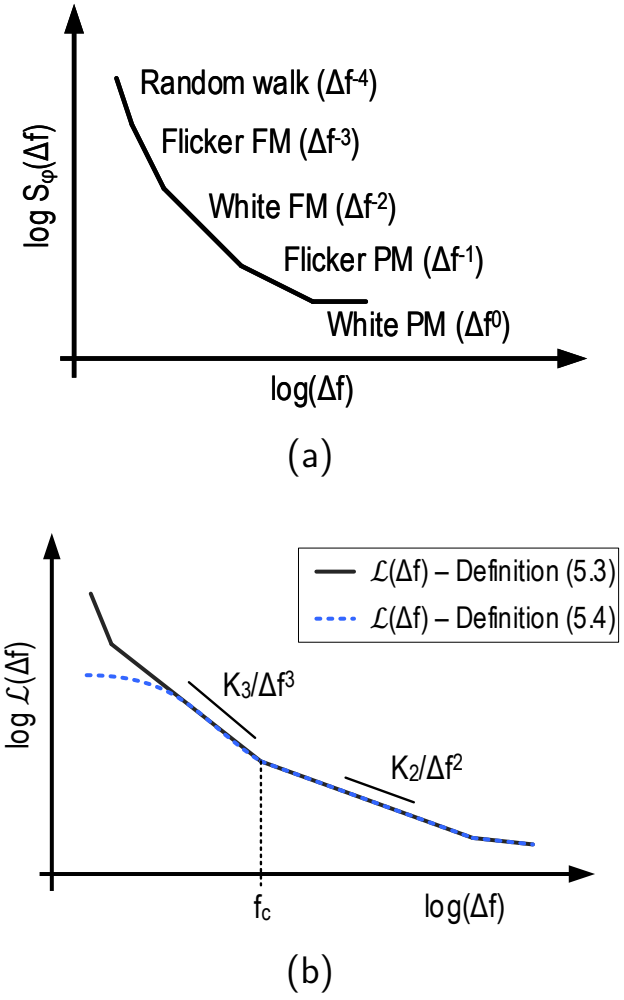


Figure 5.7: (a) Typical segments of $S_\phi(\Delta f)$ PSD. (b) Comparison between definitions (5.3) and (5.4) of $\mathcal{L}(f)$ at low and middle offset frequencies.

mean that $S_w(f_0 + \Delta f)$ also tends to infinity (what is senseless because signal power is finite). The spectrum of the oscillation close to the oscillation frequency has been discussed in [79–82], drawing the conclusion that the PSD tends to a constant finite value at very low offset frequencies, as illustrated in Fig. 5.7(b). This graph also depicts the simplified model of phase noise, where the five regions described in Fig. 5.7(a) are reduced to the two regions that typically domain at middle frequencies, in the band of interest of most applications. This simplification allows the description of the phase noise with only three parameters:

$$\mathcal{L}(\Delta f) = \frac{K_3}{\Delta f^3} + \frac{K_2}{\Delta f^2}, \tag{5.5}$$

where K_3 and K_2 are parameters defined by noise levels. These two parameters are related by $K_3 = K_2 \cdot f_c$, where f_c is the corner frequency which delimits the separation between the flicker noise and the white noise regions. For most of the oscillators used in VCO-ADCs, this description is accurate up to offset frequencies below the order of magnitude of the center oscillation frequency. Given that in most of applications this frequency is chosen to be well above the band of interest, this limit is relevant only for very high quality factor oscillators.

5.2.2 Input referred phase noise

The oscillation frequency of a real VCO can be written as follows:

$$f(t) = f_0 \cdot \Big(1 + g\big(v_{in}(t)\big)\Big) + f_n(t), \tag{5.6}$$

noident where $f(t)$ is the oscillation frequency at instant t, $f_n(t)$ is the random oscillation frequency variation due to noise, and $g(\cdot)$ is a function that describes the relationship between the input signal $v_{in}(t)$ and the oscillation frequency. Function $g(\cdot)$ depends on the topology of the oscillator, but in most cases it is nonlinear and it can be linearized around $v_{in}(t) = 0$ as follows:

$$f(t) = f_0 \cdot \Big(1 + k_d \cdot v_{in}(t) + \varepsilon\big(v_{in}(t)\big)\Big) + f_n(t), \tag{5.7}$$

noident where k_d is the relative frequency deviation factor (or gain) and $\varepsilon\big(v_{in}(t)\big)$ is a factor that represents the distortion components, which will be discussed in Section 5.3 and can be neglected in the noise analysis. $f_n(t)$ reduces the accuracy of the encoding process and limits the SNR of the converter because it is indistinguishable from a frequency variation produced by the input signal. In the same way as in conventional circuits the electrical noise is referred to the input, phase noise can be referred to the input of the VCO so it can be directly compared with the input signal, regardless the post-processing applied:

$$f(t) = f_0 \cdot \Big(1 + k_d \cdot \big(v_{in}(t) + r(t)\big)\Big). \tag{5.8}$$

The signal $r(t)$ is the input referred phase noise (IRPN) and represents a signal that, if applied to the input of a noiseless VCO, would produce an oscillation frequency variation similar to the one that a real oscillation exhibits with zero input due to phase noise.

Fig. 5.8(a) depicts the block diagram of a linear noisy VCO seen as a frequency integrator. In this model, the output of the integrator is the ideal phase of the oscillator to which the phase fluctuations are added. Among many others, one way to obtain a square wave from the phase is by calculating its sine and comparing the result with zero. Phase noise can be referred to the input of a noise-less VCO by simply multiplying the phase fluctuations $\phi(t)$ by the inverse of the transfer function seen from the input to the phase of the oscillator, as shown in Fig. 5.8(b). Therefore, the IRPN of a VCO can be expressed as

$$r(t) = \frac{1}{2\pi k_d f_0} \cdot \frac{d\phi(t)}{dt}. \tag{5.9}$$

And the one-sided PSD of the IRPN can be calculated as follows:

$$S_r(\Delta f) = S_\phi(\Delta f) \left(\frac{2\pi\Delta f}{2\pi k_d f_0}\right)^2. \tag{5.10}$$

Equation (5.10) can be combined with (5.3) to obtain

$$S_r(\Delta f) = S_\phi(\Delta f)\frac{\Delta f^2}{k_d^2 f_0^2} = \mathcal{L}(\Delta f)\frac{2\Delta f^2}{k_d^2 f_0^2}. \tag{5.11}$$

If the phase noise PSD follows the distribution described in (5.5) under the same assumptions, (5.11) can also be written as

$$S_r(\Delta f) = \left(\frac{2K_2}{f_c f_0^2 k_d^2}\right)\left(\frac{f_c}{\Delta f} + 1\right). \tag{5.12}$$

The SNR is given by the ratio between the signal power and noise power. Assuming that the effects of aliasing are negligible, input referred noise power can be calculated integrating the IRPN described in (5.11)

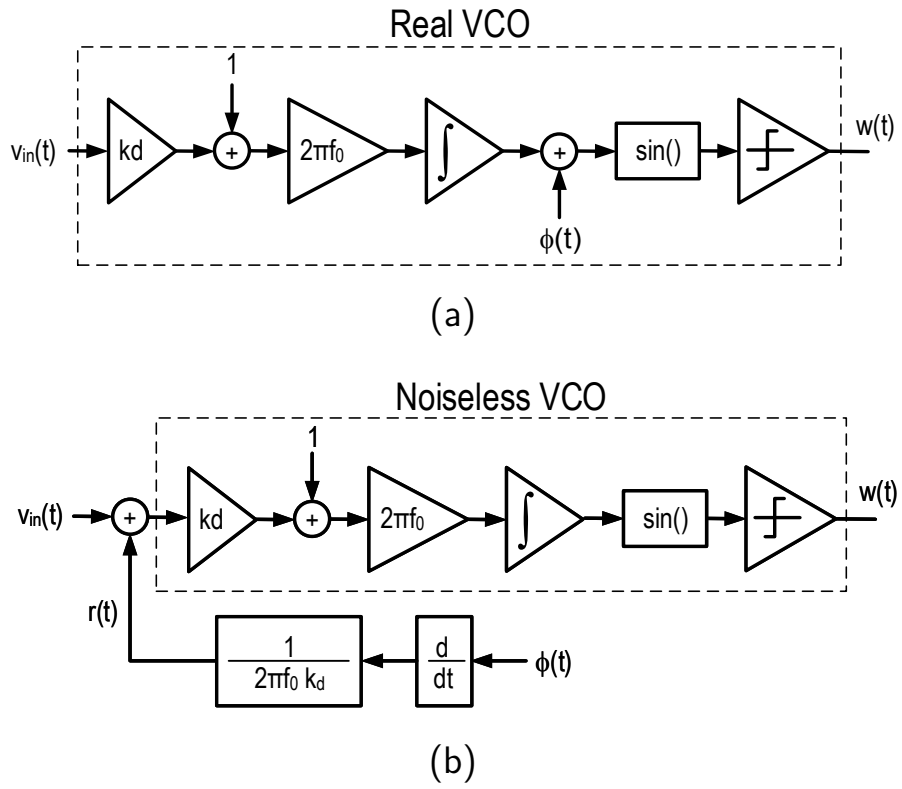


Figure 5.8: (a) Diagram of a real VCO with phase noise added to the phase of the oscillator. (b) Equivalent block diagram of the VCO with the phase noise referred to the input.

between the limits of the band of interest. The SNR of the VCO-ADC due to phase noise can be calculated comparing the input signal power to the input referred noise power as follows:

$$SNR = 10 \cdot log_{10}\left(\frac{P_{signal}}{P_{noise}}\right) = 10 \cdot log_{10}\left(\frac{v_{in\text{-}peak}^2/2}{\int_{f_{Lo}}^{f_{Hi}} S_r(\Delta f) d\Delta f}\right), \qquad (5.13)$$

where f_{Lo} and f_{Hi} are respectively the lower and upper limits of the band of interest, and $v_{in\text{-}peak}$ is the amplitude of the input tone.

System level simulations

In order to validate the model presented above, we have computed a behavioral simulation of the first-order XOR-based $\Sigma\Delta$ ADC depicted in

Figure 3.19(b) including an arbitrary level of phase noise. Figure 5.9(a) describes the SSB PSD of the oscillation, $S_w(f)$, that can be used to estimate the phase noise by applying (5.4). Figure 5.9(b) illustrates the equivalence stated in (5.3), given that $S_\phi(\Delta f)$ is about 3 dB above the $\mathcal{L}(\Delta f)$ estimated. Figure 5.9(c) compares the IRPN calculated by applying (5.11) to phase noise, to the spectrum of the data converter output bitstream $y[n]$ divided by the ADC gain (so it is also referred to the input). It can be observed that the matching between both simulations is limited up to the frequency on which quantization noise exceeds phase noise. The gain of this XOR-based VCO-ADC can be derived from the term BB introduced in [51]. At frequencies well below the sampling frequency, it can be demonstrated that the gain of this ADC is

$$BB(f) \approx \frac{2k_d f_0}{f_s}, \qquad \text{if } f \ll f_s. \tag{5.14}$$

5.3 Distortion

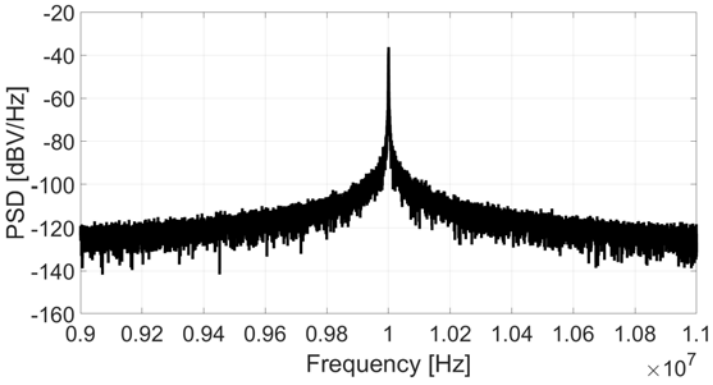
In addition to phase noise, the distortion of the VCO is an important nonideality that can limit the performance of the ADC. Distortion is due to the nonlinear relationship between the input magnitude and the oscillation frequency, which corresponds to the function $g(\cdot)$ introduced in (5.6). The nonlinear function $g(\cdot)$ can be expressed as the following polynomial:

$$g\big(v_{in}(t)\big) \approx k_{d1} v_{in}(t) + k_{d2} v_{in}(t)^2 + k_{d3} v_{in}(t)^3 + ... \tag{5.15}$$

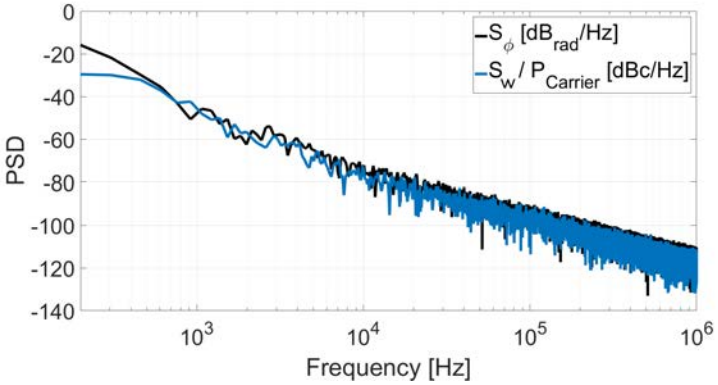
For a sinusoidal input with amplitude A and frequency ω_{in}, the oscillation frequency can be rewritten as follows:

$$\begin{aligned} f(t) = & f_0 \cdot \Big(1 + k_{d1} A \cdot \cos(\omega_{in} t) + k_{d2} A^2 \cdot \cos^2(\omega_{in} t) + \\ & k_{d3} A^3 \cdot \cos^3(\omega_{in} t) + k_{d4} A^4 \cdot \cos^4(\omega_{in} t) + ...\Big), \end{aligned} \tag{5.16}$$

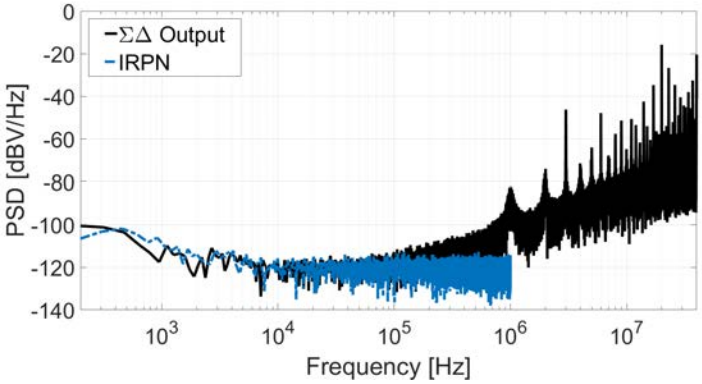
which after a few trigonometrical transformation can be expressed as:



(a)



(b)



(c)

Figure 5.9: (a) Power spectrum of the oscillation $S_w(f)$. (b) Phase noise and phase fluctuation power spectral density. (c) IRPN and output data power spectral density.

$$
\begin{aligned}
f(t) = & f_0 \cdot \left(\left(1 + \frac{A^2 k_{d2}}{2} + \frac{3A^4 k_{d4}}{8} + \frac{10A^6 k_{d6}}{32} + ... \right) + \right. \\
& \cos(\omega_{in} t) \left(A k_{d1} + \frac{3A^3 k_{d3}}{4} + \frac{10A^5 k_{d5}}{16} + ... \right) + \\
& \cos(2\omega_{in} t) \left(\frac{A^2 k_{d2}}{2} + \frac{A^4 k_{d4}}{2} + \frac{15A^6 k_{d6}}{32} + ... \right) + \\
& \left. \cos(3\omega_{in} t) \left(\frac{A^3 k_{d3}}{4} + \frac{5A^5 k_{d5}}{16} + ... \right) + ... \right) + ...
\end{aligned} \tag{5.17}
$$

The amount of terms required to accurately calculate the signal to distortion ratio (SDR) depends on the oscillator topology and on the application, but in most of the cases $\{|Ak_{d1}|\} \gg \{|A^2 k_{d2}|, |A^3 k_{d3}|\} \gg \{|A^4 k_{d4}|, |A^5 k_{d5}|, ...\}$. Therefore, the signal-to-distortion ratio can be estimated as follows:

$$
\mathrm{SDR}(A) \approx 10 \log_{10} \left(\frac{\left(4 A k_{d1}\right)^2}{\left(2A^2 k_{d2}\right)^2 + \left(A^3 k_{d3}\right)^2} \right). \tag{5.18}
$$

5.4 Periodic steady-state based simulations

Due to the time-varying behavior of oscillators, classical analysis based on small-signal linearization such as AC and Noise analysis are not suitable for simulating VCOs. Transient noise analysis can accurately simulate the behavior of the VCO-based system, but this demands a significant amount of computing power and time. This issue is magnified in some VCO applications on which the time constants of the oscillator subcircuits are several orders of magnitude shorter than the length of the simulation required to obtain relevant results. Given the highly iterative nature of the design and optimization processes, transient simulations are not always an efficient tool to face the design phase.

In this section we describe how to estimate the limitations that a given VCO imposes to a VCO-based system in terms of distortion and phase noise without performing long transient simulations. Some simulation

options may differ from the ones used in this section depending on the design environment (as a reference, in this case we are using Cadence® Virtuoso® Design Environment version IC6.1.6.500.6).

We have taken as case study the first-order VCO-based ADC depicted in Figure 5.10, assuming a bandwidth from 1 kHz to 100 kHz. This system consists of an 11-stage voltage controlled ring oscillator, and the XOR-based F2D converter described in Fig. 3.19. Given that the amplitude of the oscillation $w(t)$ depends on the input signal v_{in}, a level shifter would be required to generate an square oscillation compatible with digital circuitry. For the sack of simplicity, only the VCO has been simulated at transistor level using realistic models, whereas the level shifter and the F2D converter has been emulated using MATLAB®. Under nominal conditions ($v_{in} = 1$ V), the oscillation frequency of the VCO is approximately 60 MHz.

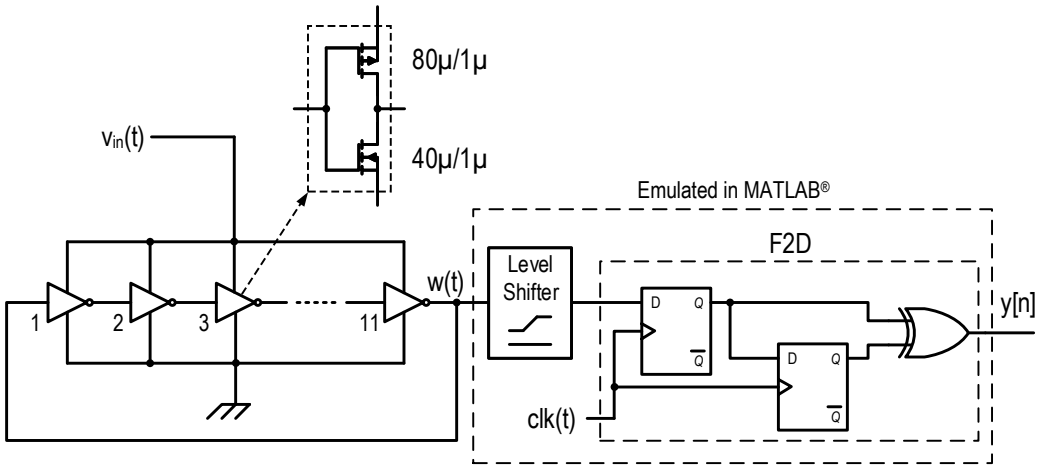


Figure 5.10: Simulated VCO-based ADC.

Simulating this VCO with the appropriate settings to obtain an acceptable accuracy may take a few hours. In our case, with the simulation setup that we have available, simulating this circuit for 4 milliseconds takes between 3 and 16 hours, depending on the maximum step size chosen. Fortunately, there are other tools capable of simulating the behavior of oscillators and their noise. For example, Cadence® Spectre® RF Option provides the Harmonic Balance (HB) analysis and the Shooting Newton method to calculate the periodic steady-state (PSS) of oscillators. The Shooting Newton method calculates the time-domain PSS

and it is suitable for highly nonlinear circuits such as ring oscillators, relaxation oscillators, and frequency dividers. HB performs a frequency-domain analysis, which is more efficient for weak and midly nonlinear circuits such as LC oscillators [83]. The VCRO simulated is a strongly nonlinear circuit with sharp transitions, so the Shooting Newton method is in principle more suitable. A PSS simulation can accurately determine in a few seconds that the oscillation frequency of this VCO. Taking advantage of the PSS sweep tool, we can perform several PSS analysis while sweeping the input voltage in order to estimate the oscillation frequency for different input voltages, resulting in the plot shown in Fig. 5.11.

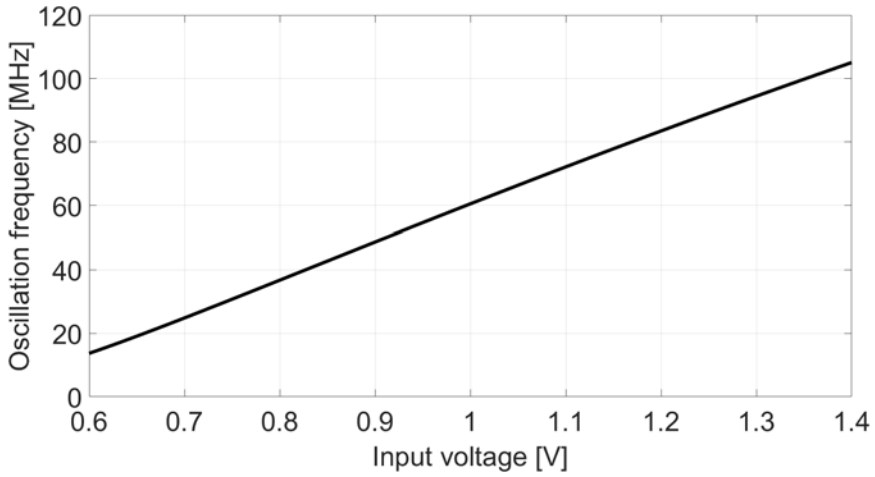


Figure 5.11: Relationship between oscillation frequency and input voltage obtained through PSS sweep simulations.

Table 5.1 shows the coefficients obtained from applying the polynomial curve fitting MATLAB® function *polyfit()* to the set of points plotted in Fig. 5.11. As shown in Figure 5.12, the resulting 8^{th} degree polynomial describes the relationship between the input voltage and the oscillation frequency in the range 1 V $\pm$ 400 mV with a deviation lower than 1 kHz. These coefficients can be combined with equation (5.18) to plot the SDR against input level curve depicted in Figure 5.13.

After calculating the PSS, the pnoise analysis available in our design environment can be used to estimate the phase noise of the oscillator. This tool allows the calculation of different types of phase noise, depending on the simulation setup. Table 5.2 shows the type of noise that result from the pnoise simulation for four different simulation setups, which are

Table 5.1: Polynomial coefficients obtained from the curve of Fig. 5.11

Parameter	Value	Parameter	Value
k_{d1}	1.94 V^{-1}	k_{d5}	-0.124 V^{-5}
k_{d2}	-0.2 V^{-2}	k_{d6}	0.917 V^{-6}
k_{d3}	-0.226 V^{-3}	k_{d7}	-3.75 V^{-7}
k_{d4}	0.22 V^{-4}	k_{d8}	4.36 V^{-8}

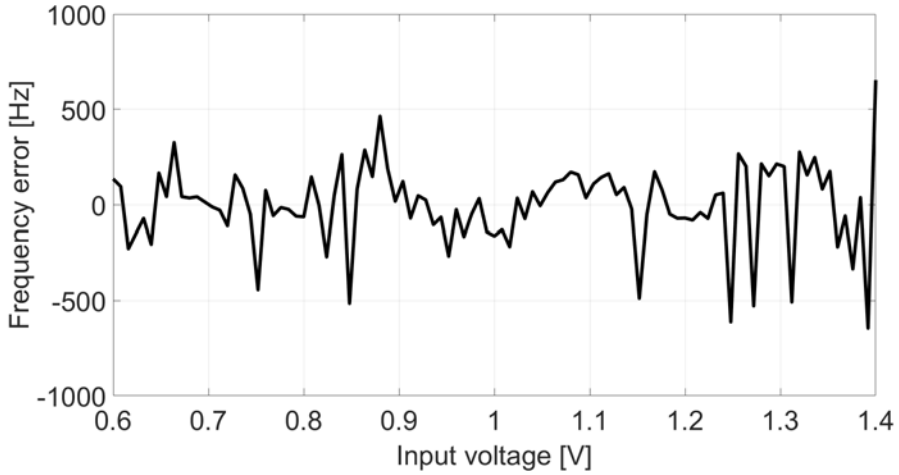


Figure 5.12: Difference between the oscillation frequency obtained by PSS simulation and the polynomial described in Table 5.1.

of special interest in our application.

On one hand, the simulations computed choosing "Modulated" noise estimate the sideband correlation and allow the separation PM and AM noise. On the other hand, choosing "Sources" noise implies that the simulator calculates the phase noise according to definitions (5.3) or (5.4), depending on the parameter "lorentzian". Fig. 5.14 shows the results of pnoise simulations with the different options described in the table. It can be observed that AM noise is negligible compared with PM noise for most of the frequencies. In addition, the phase noise computed selecting the noise type "Sources" is 3 dB below the PM noise and it is limited at low offset frequencies if "lorentzian = yes", in concordance

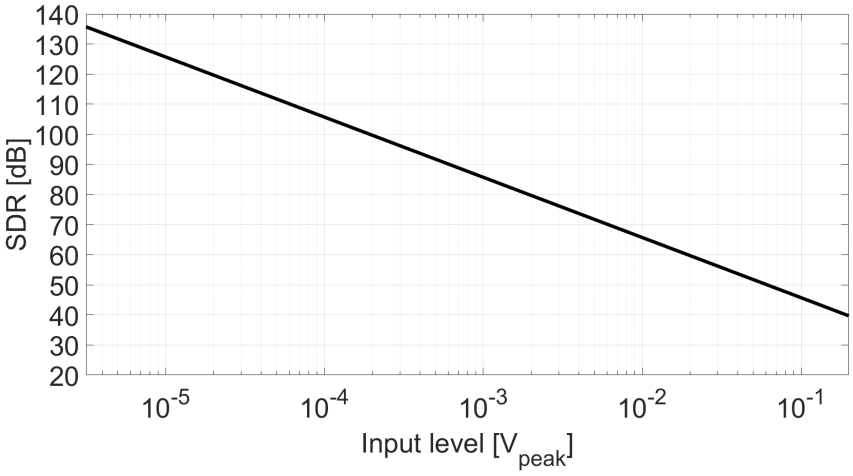


Figure 5.13: Signal to distortion ratio for different input levels.

Table 5.2: Results obtained from different pnoise simulation setups.

Pnoise setup	Simulation result
Modulated - PM	$S_\phi(\Delta f)$
Modulated - AM	Amplitude fluctuations
Sources - Lorentzian = no	$\mathcal{L}(\Delta f)$ - Definition (5.3)
Sources - Lorentzian = yes	$\mathcal{L}(\Delta f)$ - Definition (5.4)

with (5.3).

According to equation (5.11), both $S_\phi(\Delta f)$ and $\mathcal{L}(\Delta f)$ (definition (5.3)) can be used to calculate the input referred phase noise. The noise power integrated from 1 kHz and 100 kHz is approximately 5 μV^2. As mentioned above, assuming that aliasing does not have a significant impact on the noise spectral distribution at the output of the system, the SNR of the converter can be estimated applying equation (5.13). Figure 5.15 shows the SNR for different input signal levels.

Figure 5.16(a) shows the comparison between the SNDR curve estimated using the simulation strategy described in this section, and the SNDR obtained using time-domain simulations. The black curve is the result of combining Figures 5.13 and 5.15. The blue squares indicate the

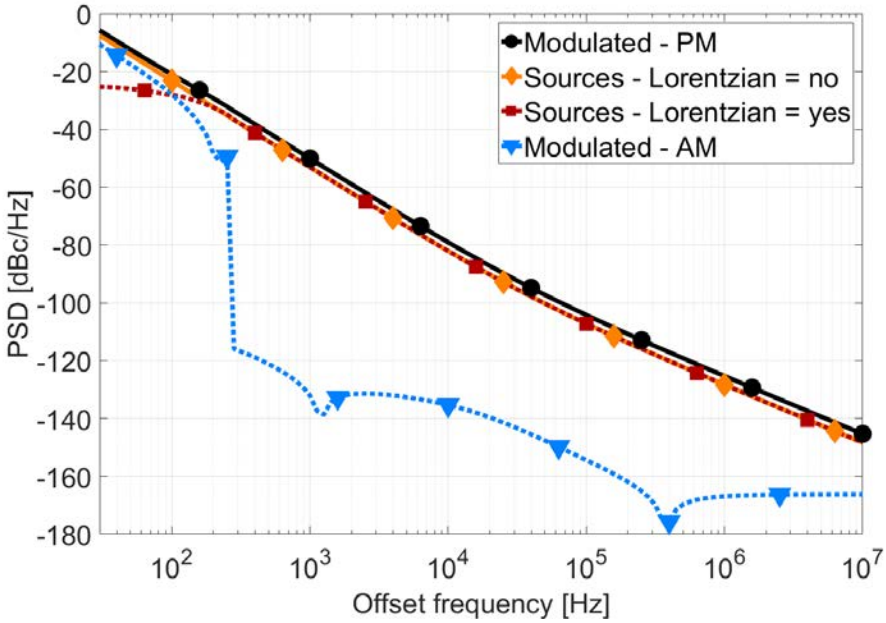


Figure 5.14: Comparison between different periodic noise simulations.

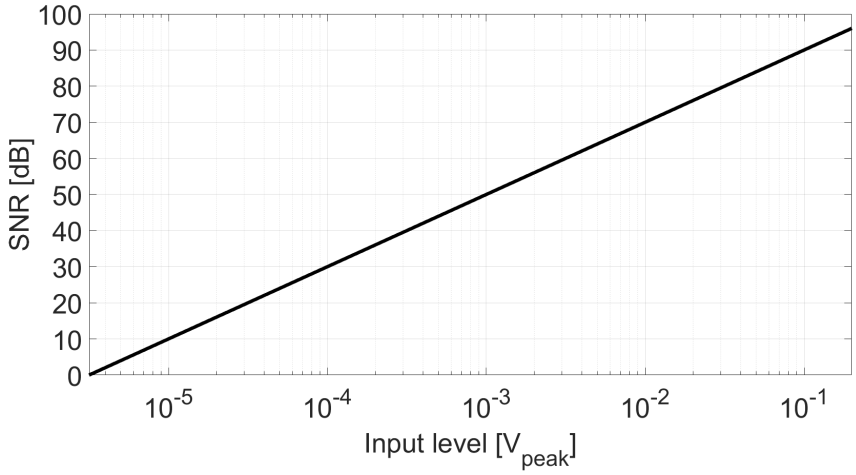
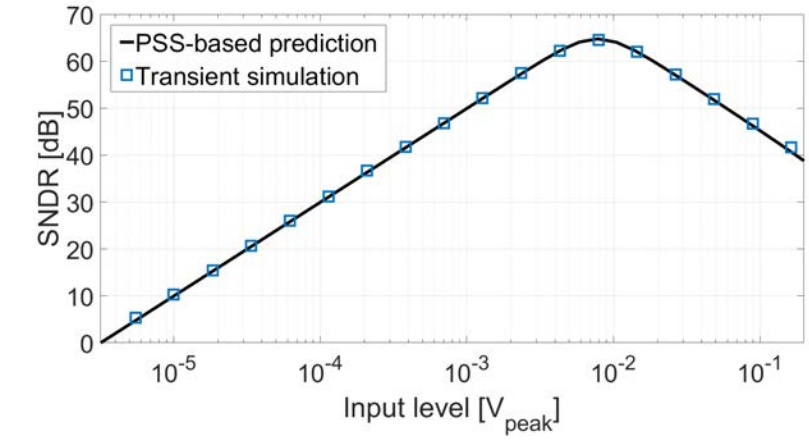
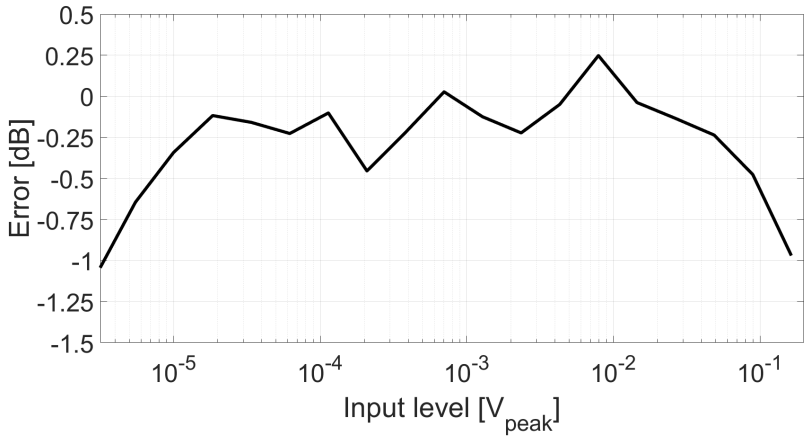


Figure 5.15: Signal to noise ratio for different input levels estimated using the input referred phase noise.

SNDR obtained from measuring the output spectra computed through transient simulations. As shown in Figure 5.16(b), the difference between both simulation methodologies is lower than 1 dB for most of the range evaluated.



(a)



(b)

Figure 5.16: (a) Performance of circuit shown in Figure 5.10 calculated using transient simulations and estimated from PSS and pnoise simulations. (b) SNDR difference between both methodologies.

5.5 Conclusions

In this chapter we have described the influence of phase noise and distortion in the performance of oscillator-based systems. We have proposed a methodology to evaluate the maximum achievable SNDR of an oscillator based on two simulations: a PSS sweep is used to calculate the oscillation frequency, the gain, and the distortion of the oscillator; and a periodic noise analysis is used to calculate the phase noise, which can

be subsequently referred to the input of the converter to estimate the SNR. This method can be applied to any oscillator, independently of the system architecture, and allows the estimation of the SNDR without resorting to transient simulations. As an advantage, the computing time of our proposed method is at least one order of magnitude faster, which facilitates the optimization of the oscillator circuit.

CHAPTER 6

Influence of sampling clock jitter in $\Sigma\Delta$ modulators

6.1 Introduction

Continuous-time $\Sigma\Delta$ ADCs present interesting advantages compared to their discrete-time counterparts, such as potentially higher achievable sampling rate and lower power consumption. In addition, CT-$\Sigma\Delta$ modulators benefit from inherent antialiasing filtering, whereas their DT equivalent require dedicated filters before sampling [84]. However, CT-$\Sigma\Delta$ converters are more sensitive to sampling period random variations (i.e., clock jitter). The errors introduced by clock jitter are visible on the output spectrum and may limit the signal-to-noise ratio of the ADC.

The effects of clock jitter in $\Sigma\Delta$ modulators have been widely studied during the last two decades [64–70]. The mechanisms whereby clock jitter degrades the performance of the converter depend on the modulator topology (i.e. loop filter order, number of bits of the quantizer, feedback DAC topology, etc). For example, the advances and delays of the clock edges respect to their ideal position may cause errors in the sampled values. Fortunately, the error power inside the band of interest is attenuated by the loop filter. On the other hand, the pulse duration of the feedback DACs is frequently proportional to the sampling period,

for example when NRZ DACs are used (the duration of the pulse is the sampling period). Therefore, random period variations imply random amounts of charge injected to the integrators. The main source of noise is typically the DAC in the outer filter loop because its error is injected at the input of the modulator, so its power contribution in the band of interest is not attenuated by the filter loop.

The analysis of a modulator in presence of clock jitter presents further challenges due to the varying frequency of the sampling clock. These difficulties are frequently circumvented modeling the effects of clock jitter as the addition of error signals to certain nodes of an equivalent system sampled by an ideal clock. However, finding the set of error signals that produce a completely equivalent system is not straightforward, and accuracy is sometimes partially sacrificed for the sack of simplicity. Indeed, most of the analysis available in the literature are focused on studying only certain effects of clock jitter in the performance of the system. Fig. 6.1 illustrates a generic CT-ΣΔ modulator on which jitter is modeled as the addition of a noise signal (n_{DAC}) at the output of the feedback DAC. This approach has become very popular because it can be used to model the modulation of the feedback DAC pulse width, which is one of the dominant error sources introduced by clock jitter. However, calculating the spectral properties of signal n_{DAC} is typically a challenging task due to the system complexity and non-uniform sampling.

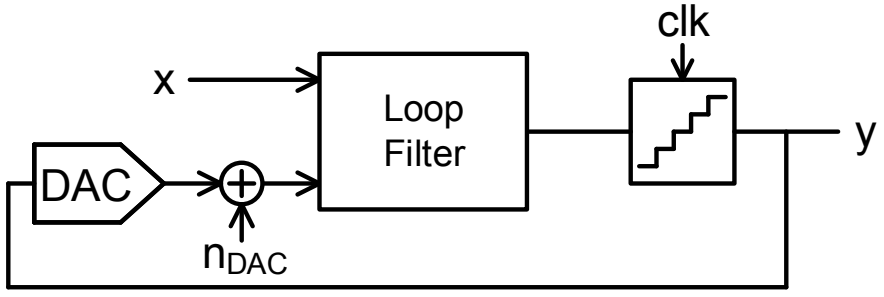


Figure 6.1: Classical modeling of clock jitter as additive noise injected into the feedback loop.

In this chapter we propose a time-base projection that simplifies the modeling of clock jitter in CT-ΣΔ modulators without loss of accuracy. The proposed transformation consists on referring all the signals and

operations to a time-base relative to the phase of the sampling clock, instead of to the physical time as is traditionally done. The result is a system on which the sampling rate is constant, and clock jitter is modeled as an alteration of the integrator gain and the modulation of the input signal frequency. This system is completely equivalent to the original modulator, but it is easier to analyze and simulate since its sampling clock is ideal. Therefore, the proposed time-base projection opens up new analysis possibilities, making possible the accurate identification of all the errors induced by clock jitter.

6.2 Jitter analysis based on a relative time-base projection

The period of a "real-world" clock signal can be expressed as

$$T_s[n] = T_{s0} + \Delta T_j[n] = T_{s0} \cdot \big(1 + e_j[n]\big), \tag{6.1}$$

where T_{s0} is the ideal clock period, and ΔT_j is the random period variation due to jitter. $e_j[n]$ is the period variation normalized to the ideal sampling period:

$$e_j[n] = \frac{\Delta T_j[n]}{T_{s0}} = \frac{t_{n+1} - t_n}{T_{s0}} - 1, \tag{6.2}$$

where t_n and t_{n+1} are the time instants on which the n^{th} and $(\mathrm{n+1})^{\mathrm{th}}$ clock rising edges occur.

The spectral properties of $e_j[n]$ depend on the clock source: a free-running oscillator produces a clock with mainly white period spectrum; on the other hand, an oscillator locked to a high-purity reference oscillator generates a clock signal whose period variation depends on the loop filter design [85,86]. A continuous time signal $e_j(t)$ can be obtained applying a zero-order hold to the sequence $e_j[n]$, as shown in Fig. 6.2, that can be expressed as a function of time as follows:

$$e_j(t) = \sum_{k=-\infty}^{+\infty} e_j[k] \left(u\left(t - \sum_{i=-\infty}^{k} \left(1 + e_j[i]\right) \cdot T_{s0} \right) - u\left(t - \sum_{i=-\infty}^{k+1} \left(1 + e_j[i]\right) \cdot T_{s0} \right) \right). \tag{6.3}$$

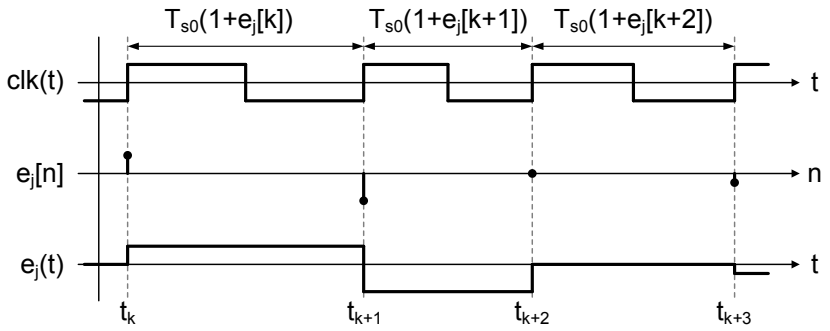


Figure 6.2: Clock signal and normalized period variation represented respect to the real-world time (t).

As stated in the introduction, describing the behavior a complex system complicates when the sampling period randomly changes over time. For this reason, we propose to describe all the signals referred to a different time-base, the relative time t_r, which can be expressed as a function of the physical time t as follows:

$$t_r(t) = nT_{s0} + \frac{t - t_n}{1 + e_j(t)}, \quad t_n \leq t < t_{n+1}, \quad \forall n \in \mathbb{Z}. \tag{6.4}$$

Fig. 6.3 shows the graphical representation of t_r as a function of t. Note that the slope of $t_r(t)$ in the derivable regions of the function can be denoted as

$$\frac{dt_r}{dt} = \frac{1}{1 + e_j(t)}, \quad t_n < t < t_{n+1}, \quad \forall n \in \mathbb{Z}. \tag{6.5}$$

Fig. 6.4 illustrates how the signals described in Fig. 6.2 look like when referred to t_r. Since the contraction/elongation of the time-base compensates the delays/advances of the sampling instants, the clock signal restores its ideal period:

$$t_r(t_{n+1}) - t_r(t_n) = T_{s0}. \tag{6.6}$$

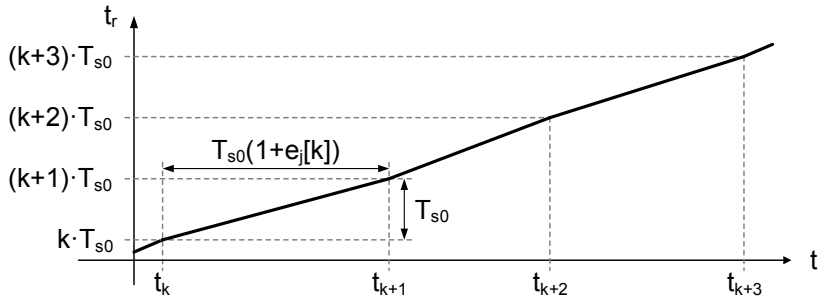


Figure 6.3: Proposed relative time t_r represented respect to the real-world time (t).

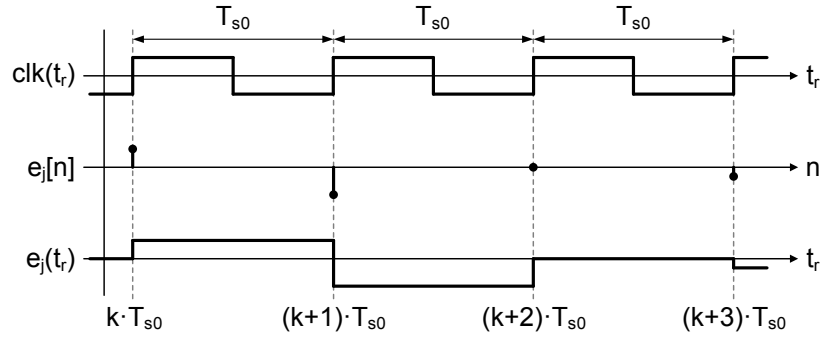


Figure 6.4: Clock signal and normalized period variation represented in the relative time-base (t_r).

The period variation (e_j) can be also referred to t_r as follows:

$$e_j(t_r) = \sum_{k=-\infty}^{+\infty} e_j[k]\Big(u\big(t_r - kT_{s0}\big) - u\big(t_r - (k+1)T_{s0}\big)\Big). \tag{6.7}$$

The implications of the adoption of the time-base proposed depends on the modulator topology. Fig. 6.5 shows a classical second order CT-ΣΔ, where the shape of the feedback pulse depends on the DAC topology (in this section we consider NRZ DACs for simplicity). Describing this system in the proposed time-base relative to the sampling clock requires two transformations.

Firstly, real-world integrators integrate their input signals respect to the physical time t, so they must be adapted to the proposed time-base.

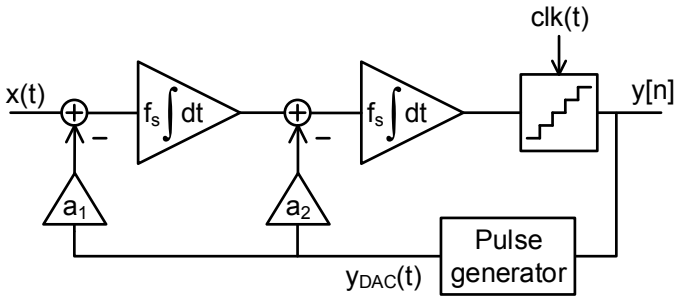


Figure 6.5: Generic second order continuous-time ΣΔ modulator.

Let x_1 and x_2 be respectively the input and the output of an analog integrator, as shown in Fig. 6.6(a). The relationship between these two signals can be expressed through the well known differential equation:

$$\frac{dx_2(t)}{dt} = x_1(t). \tag{6.8}$$

In order to perform this integration respect to t_r, equation (6.8) can be modified applying the chain rule as follows:

$$\frac{dx_2(t_r)}{dt} = \frac{dx_2(t_r)}{dt_r}\frac{dt_r}{dt} = x_1(t_r), \tag{6.9}$$

which in combination with (6.5) results in

$$x_2(t_r) = \int \big(1 + e_j(t_r)\big)x_1(t_r)dt_r. \tag{6.10}$$

Therefore, an integrator like that of Fig. 6.6(a) can be replaced with an integrator preceded by a multiplication by the sampling time normalized to the ideal sample time $(1 + e_j(t_r))$, as shown in Fig. 6.6(b).

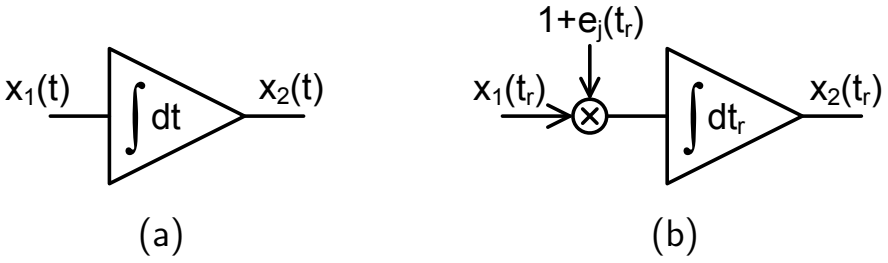


Figure 6.6: (a) Model of an integrator in t respect to t. (b) Model of an integrator in t respect to t_r.

In addition, any external signal has to be described using the proposed time-base t_r. If the input of the system $x(t)$ is a cosine wave of amplitude A and frequency f_{t0} like

$$x(t) = A \cdot \cos\Big(\int 2\pi f_t(t)dt\Big), \text{ where } f_t(t) = f_{t0}, \tag{6.11}$$

we can apply a procedure similar to the one used to obtain (6.10) to rewrite equation (6.11) as:

$$\begin{aligned} x(t_r) =& A \cdot \cos\left(\int 2\pi f_t(t_r)dt_r\right), \\ & \text{where } f_t(t_r) = \big(1 + e_j(t_r)\big)f_{t0}. \end{aligned} \tag{6.12}$$

In other words, clock jitter also modulates the frequency of the input tone. This effect is the representation on the relative time-base of the signal degradation due to the non-uniform sampling that the non-ideal clock implies.

The other external signal in the system taken as case study is the sampling clock which, as explained before, results in a square wave of constant period T_{s0} when referred to t_r. Fig. 6.7 illustrates how the system of Fig. 6.5 can be described using the proposed projection. This model is a theoretical analysis tool that can be used to study the modulator assuming constant sampling period, independently of the jitter power and spectral shape. Moreover, system-level simulations benefit from the simplicity of this model without compromising accuracy.

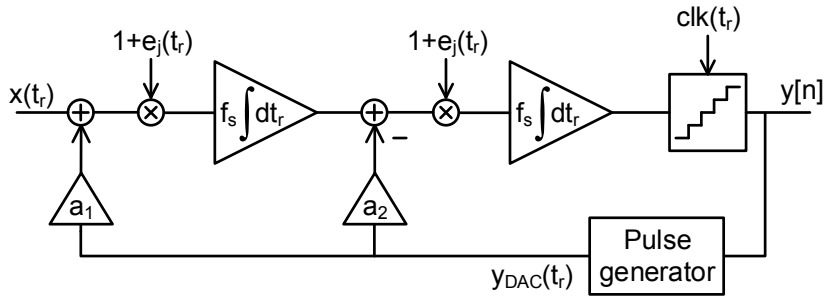


Figure 6.7: Generic second order continuous-time ΣΔ modulator described respect to t_r

Fig. 6.8 shows the output spectra of two modulators simulated using a behavioral model. The first spectrum, Y, is obtained simulating the system of Fig. 6.5 with $a_1 = 1$, $a_2 = 3/2$, and the signal $x(t) = 0.01 \cdot \sin(2\pi t f_s/512)$ applied to the input. Period jitter ($e_j[n]$) is a zero-mean normally distributed random sequence (flat spectral distribution) whose standard deviation equals 0.01. The second spectrum, Y_r, is the output of the equivalent system shown in Fig. 6.7, on which the sampling clock is ideal and the input signal is as described in (6.12). It can be observed that the result of both simulations is identical.

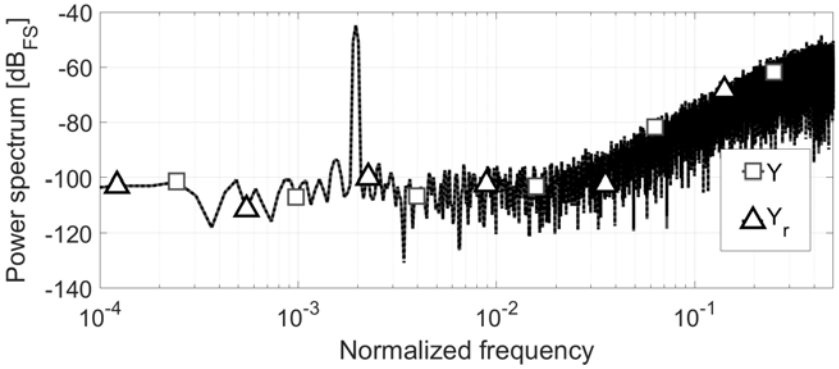


Figure 6.8: Output spectra of the systems shown in Figs. 6.5 (Y) and 6.7 (Y_r).

6.3 Application to CT-ΣΔ modulators with NRZ DACs

In this section we present how the model introduced in Section 6.2 can be used to analyze the effects of clock jitter in a CT-ΣΔ modulator with NRZ DACs.

Lets consider the system of Fig. 6.5, on which the pulse generator is a zero order hold. This system can be transformed into the one shown in Fig. 6.9 after splitting the input signal path and both feedback loops and changing the time-base of the integrators (as shown in Fig. 6.6(b)) and external signals. For a sinusoidal wave of amplitude A and constant frequency f_t, the input tone can be referred to t_r by adding an error

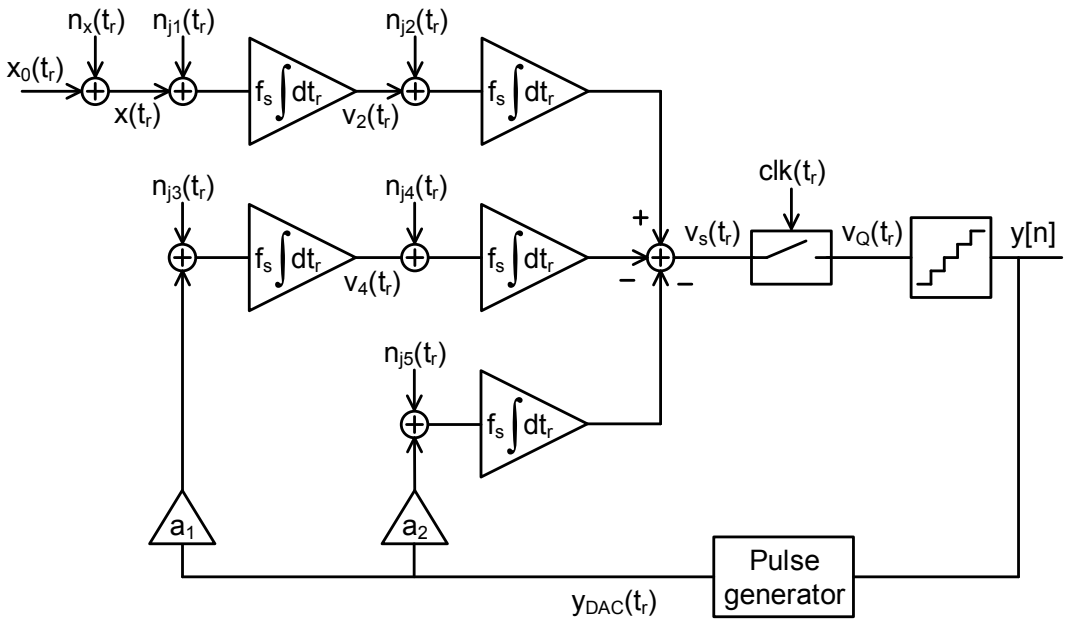


Figure 6.9: Alternative representation of the system of Fig. 6.7.

signal $n_x(t_r)$ to the ideal sinusoid $x_0(t_r)$ as follows:

$$x(t_r) = x_0(t_r) + n_x(t_r), \tag{6.13}$$
$$\text{where } x_0(t_r) = A \cdot \cos\Big(\int 2\pi f_{t0} dt_r\Big).$$

The modulation of the integrators gains can also be expressed as the addition of an error signal at the input of each integrator. Therefore, we can identify five additional sources of noise: the error of both integrators due to the input signal (n_{j_1} and n_{j_2}), the error of both integrators due to the first DAC (n_{j_3} and n_{j_4}), and the error of the second integrator due to the second DAC (n_{j_5}). These errors are described by the following expressions:

$$n_{j_1}(t_r) = x(t_r) \cdot e_j(t_r), \tag{6.14}$$

$$n_{j_2}(t_r) = v_2(t_r) \cdot e_j(t_r), \tag{6.15}$$

$$n_{j_3}(t_r) = a_1 \cdot y_{DAC}(t_r) \cdot e_j(t_r), \tag{6.16}$$

$$n_{j_4}(t_r) = v_4(t_r) \cdot e_j(t_r), \tag{6.17}$$

$$n_{j_5}(t_r) = a_2 \cdot y_{DAC}(t_r) \cdot e_j(t_r), \tag{6.18}$$

where $y_{DAC}(t_r)$ is the continuous-time signal resulting of passing the output sequence through a zero-order hold, and $v_2(t_r)$ and $v_4(t_r)$ are:

$$v_2(t_r) = f_s \int \big(x(t_r) + n_{j_1}(t_r)\big) dt_r, \tag{6.19}$$

$$v_4(t_r) = a_1 \cdot fs \int \big(y_{DAC}(t_r) + n_{j_3}(t_r)\big) dt_r. \tag{6.20}$$

In order to compare these noise sources with the input signal, we can calculate the input referred equivalent as follows:

$$N_{j_k^*-IR}(s) = \left(N_{j_k}(s) \frac{V_{S_{in}}(s)}{N_{j_k}(s)} \right)^* \cdot \left(\frac{V_{S_{in}}(s)}{X(s)} \right)^{-1}, \tag{6.21}$$

where $V_{S_{in}}(s)/N_{j_k}(s)$ is the transfer function from the $\mathrm{k_{th}}$ noise source to the input of the sampler, $V_{S_{in}}(s)/X(s)$ is the transfer function from the input of the modulator to the input of the sampler, and the operator $(\cdot)^*$ represents sampling with aliasing [87]. Note that the Laplace transform has to be referred to the time-base relative to the sampling period.

On one hand, n_{j_1} and n_{j_3} are the errors injected at the input of the first integrator, so they can be referred to the input as:

$$N_{j_1^*-IR}(s) = \left(N_{j_1}(s) \cdot \frac{f_s^2}{s^2} \right)^* \cdot \left(\frac{s^2}{f_s^2} \right), \tag{6.22}$$

$$N_{j_3^*-IR}(s) = -\left(N_{j_3}(s) \cdot \frac{f_s^2}{s^2} \right)^* \cdot \left(\frac{s^2}{f_s^2} \right). \tag{6.23}$$

On the other hand, the noise produced by the second integrator can be referred to the input as follows:

$$N_{j_2^*-IR}(s) = \left(N_{j_2}(s) \cdot \frac{f_s}{s} \right)^* \cdot \left(\frac{s^2}{f_s^2} \right), \tag{6.24}$$

$$N_{j_4^*-IR}(s) = -\left(N_{j_4}(s)\cdot\frac{f_s}{s}\right)^*\cdot\left(\frac{s^2}{f_s^2}\right), \tag{6.25}$$

$$N_{j_5^*-IR}(s) = -\left(N_{j_5}(s)\cdot\frac{f_s}{s}\right)^*\cdot\left(\frac{s^2}{f_s^2}\right). \tag{6.26}$$

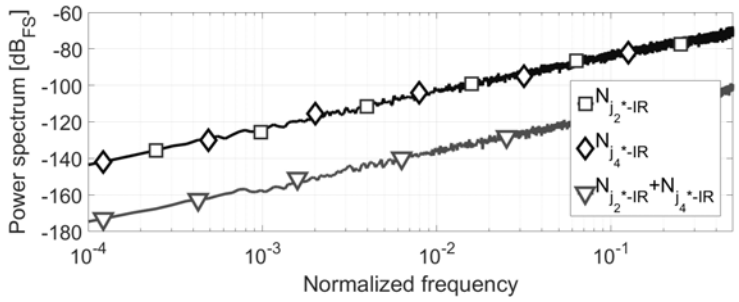
The system of Fig. 6.9 has been simulated using a behavioral model with the same parameters as in Fig. 6.8. Fig. 6.10 shows the result of averaging the spectra obtained in 16 simulations.

It can be observed that the six noise sources described before are not necessarily independent. Fig. 6.10(a) shows how $N_{j_2^*-IR}(f)$ is partially counterbalanced by $N_{j_4^*-IR}$ due to the similarities between $v_2(t_r)$ and $v_4(t_r)$ for medium and high input levels. Likewise, $N_{j_1^*-IR}$ is also partially compensated by $N_i^* - IR$ at very low frequencies, as shown in Fig. 6.10(b). Note that different system parameters, input signals, and spectral distribution of e_j may result in different correlations between noise signals.

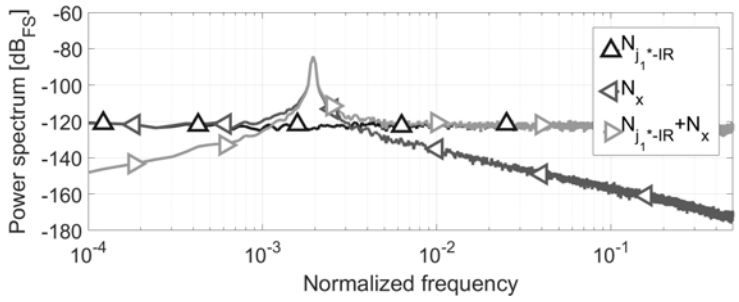
The output spectrum of the modulator is presented in Fig. 6.10(c), together with the resulting four noise contributors. The output spectrum is overlapped at low frequencies with $N_{j_3^*-IR}$, which is clearly the dominant noise source at low frequencies.

6.4 Application to a CT-ΣΔ modulator with SC based feedback DACs

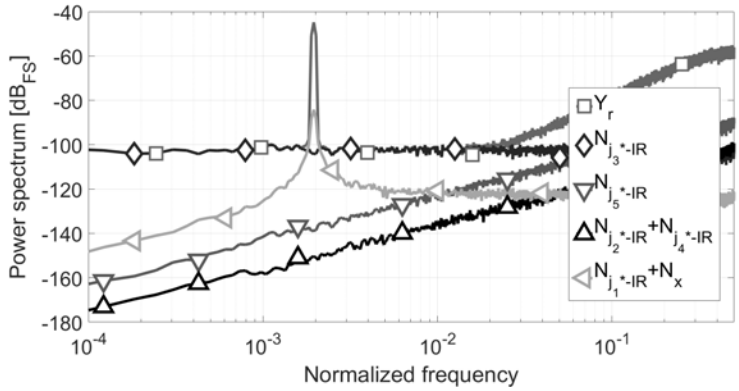
Different shapes of feedback pulses have been proposed to overcome the limitations of NRZ DACs [88]. A popular topology that improves jitter sensitivity is the switched-capacitor (SC) based feedback DAC [59]. As the feedback pulse is controlled by charging and discharging a capacitor, the amount of charge injected to the integrator is made nearly independent of the sampling period. In this section we illustrate how the proposed time-base projection can be applied to a second order CT-ΣΔ with SC-based DACs, on which the feedback pulse follows:



(a)



(b)



(c)

Figure 6.10: Spectra of different signals of the system of Fig. 6.9 with NRZ DACs. (a) Correlation between noise sources in the second integrator. (b) Correlation between input error and noise in the first integrator. (c) Output spectrum and main noise contributors.

$$y_{DAC}(t) = y[n] \cdot e^{\frac{-(t-t_n)}{RC}}, \;\; t_n \leq t \leq t_{n+1}, \;\; \forall n \in \mathbb{Z}. \tag{6.27}$$

Fig. 6.11 illustrates how the time contraction/elongation due to the

time-base change can be seen as the modulation of the discharge time constant. Therefore, the feedback pulse can be described in the projected time-base as follows:

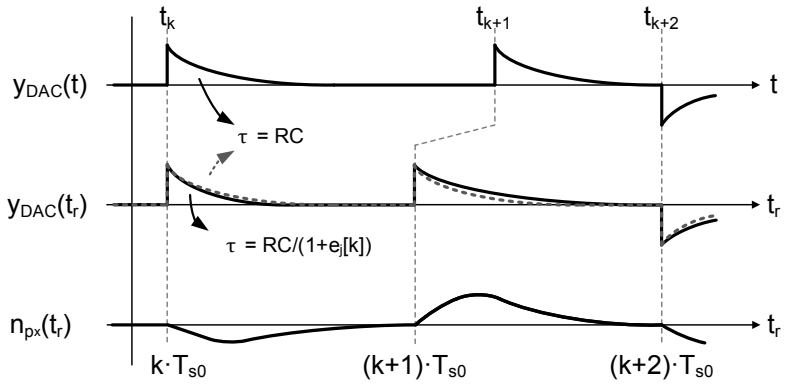


Figure 6.11: Signals related to the operation of an ideal SC-based DAC in presence of clock jitter

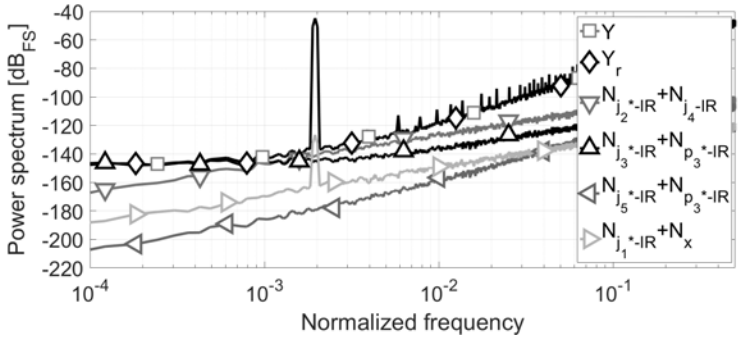
$$y_{DAC}(t_r) = y[n] \cdot e^{\frac{-(t_r - t_n)(1+e_j[n])}{RC}}, \qquad t_n \leq t_r \leq t_{n+1}, \ \ \forall n \in \mathbb{Z}. \tag{6.28}$$

We can model the variability of the time constant as the addition of the error signal n_{p_i}, which can be defined as:

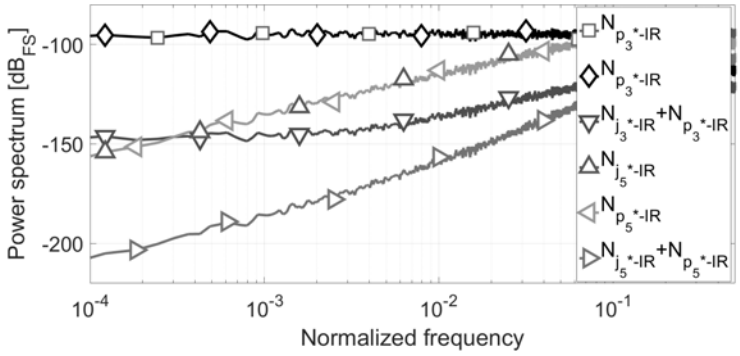
$$n_{p_i}(t_r) = y[n]\left(e^{\frac{-(t_r - t_n)(1+e_j[n])}{RC}} - e^{\frac{-(t_r - t_n)}{RC}}\right), \qquad t_n \leq t_r \leq t_{n+1}, \ \ \forall n \in \mathbb{Z}. \tag{6.29}$$

The systems of Figs. 6.5 and 6.9 have been simulated using a SC-based pulse generator and the same input signal. In this case, the sequence $e_j[n]$ is a high-pass filtered signal (i.e., we assume that the clock is synthesized using a PLL) with 0.01 of standard deviation. Fig. 6.12(a) shows the output spectrum of Fig. 6.5 (Y), which as expected is equivalent to the output of Fig. 6.9 (Y_r). In addition to slight differences at high frequencies due to the different shape of feedback pulse, it can be observed that noise at low frequencies is considerably lower than in Fig. 6.10, and

$N_{j_1^*-IR} + N_x$ is now the main contributor. This happens because $N_{p_k^*-IR}$ (n_{p_k} referred to the input) counterbalances $N_{j_3^*-IR}$ and $N_{j_5^*-IR}$, as shown in Fig. 6.12(b).



(a)



(b)

Figure 6.12: Spectra of different signals of the system of Fig. 6.9 with SC-based DACs and high-pass filtered jitter. (a) Correlation between noise sources. (b) Output spectrum and main noise contributors.

6.5 Conclusion

In this chapter we present a modeling methodology that simplifies the study of the effects of clock jitter in the performance of CT-ΣΔM. The proposed method is based on projecting all the signals and operations over a time-base relative to the sampling period. The resulting model is completely equivalent to the original system, and it can be analyzed assuming constant clock rate without loss of accuracy. As an example,

we have used the time-base projection to model and simulate two CT-ΣΔ modulators. Nevertheless, this method is potentially advantageous to analyze the influence of clock jitter in other topologies that can not be easily analyzed using existing approaches, such as oscillator-based converters or band-pass modulators.

Part III

Experimental results

CHAPTER 7

Chip 1: Second-order oscillator-based $\Sigma\Delta$ modulator with multi-bit PRIs

7.1 Introduction

This chapter describes the design and implementation of a second-order oscillator-based $\Sigma\Delta$ modulator. The main objective of this prototype is to test the feasibility of the modulator architectures introduced in Chapter 4. The proposed modulator has been designed for audio applications, aimed at digitizing the signal generated by analog MEMS microphones, as shown in Fig. I.2(b). The ASIC has been implemented in 0.13 μm CMOS technology, which is a node frequently used for this kind of applications due to its low fabrication costs. Our requirements are not the common specifications of microphone readout circuits, which typically demand dynamic ranges higher than 100 dB-A [3]. Instead, given that the primary objective of this chip is the study of this new architecture, we have targeted a dynamic range slightly lower (93 dB-A).

The proposed system consists of two phase referenced integrators, each based on the combination of a current-controlled oscillator (CCO1

and CCO2) with an up-down counter (UDC1 and UDC2), interconnected as described in Section 4.4. The single-bit output of the modulator is generated by a digital comparator driven by a 10 MHz sampling clock. Although lower sampling rates are more common in MEMS microphones (typically in the range between 700 kHz and 5 MHz [2]), emerging interfaces like MIPI SoundWire® tolerate sampling frequencies up to a few tens of MHz. Given that the center frequencies of both oscillators (97.5 MHz and 200 MHz respectively) are significantly higher that the sampling rate, both UDC1 and UDC2 require several tenths of states. We have resorted to logic synthesis tools to implement most of the digital circuit which, as explained in Chapter 4, may present several challenges.

In addition to the development of novel high-order oscillator-based modulators, the secondary objective of this integrated circuit is the validation of part of the noise calculations presented in Chapter 5. Therefore, the output of the first oscillator will be connected to an output pad, in order to facilitate the measurement of phase noise.

7.2 System-level design

Figure 7.1 shows the simplified block diagram of the proposed oscillator-based ADC, which operates as a second order ΣΔ modulator. This converter consists of two phase referenced integrators, whose interconnection is performed using a multi-bit bus (from UDC1 to DCO2). In order to simplify the digital circuitry that performs the discrete-time feedback integration, this modulator is based on a single-bit quantizer. For simplicity, the output bitstream is generated by a digital single-bit quantizer, whose output is '0' or '1' depending on if the output of UDC2 is respectively below or above an arbitrary threshold. In consequence, only two different values can be subtracted to each up-down counter. Table 7.1 summarizes the key parameters of the system described in Fig. 7.1.

Both the VCO of the first stage and the DCO of the second stage consist of an oscillator driven in current. On one hand, CCO1 is controlled by a transconductance gm, which generates a current dependent

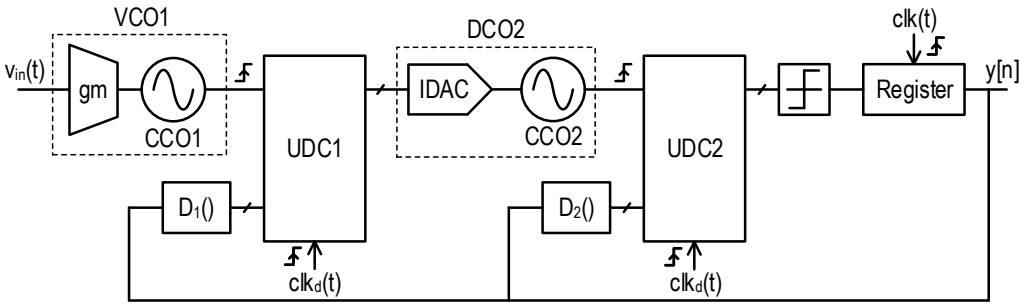


Figure 7.1: Simplified block diagram of the proposed second-order oscillator-based ΣΔ ADC with multi-bit interconnections.

Table 7.1: Parameters of the proposed oscillator-based ADC.

Parameter	Value	Parameter	Value
K_{VCO}	-800 MHz/V	K_{DCO}	2.9 MHz/code
f_{VCO_0}	97.5 MHz	f_{DCO_0}	200 MHz
$D_1(0)$	8	$D_2(0)$	10
$D_1(1)$	12	$D_2(1)$	30
d_1	4	d_2	20
f_s	10 MHz	Input full-scale	±21.6 mV
T_d	5 ns	AOP	121 dB_{SPL}

on the input voltage. The center oscillation frequency of this oscillator is f_{VCO_0} = 97.5 MHz, and the gain is K_{VCO} = -800 MHz/V. The chosen gain is negative in anticipation of the transconductor architecture which, as will be described in Section 7.3.1, produces an inversion. On the other hand, CCO2 is driven by a 64-element current DAC (IDAC), whose control signals are generated by the first up-down counter. The center oscillation frequency of the DCO2 is f_{DCO_0} = 200 MHz, and the gain is K_{DCO} = 2.9 MHz/code.

The value of both UDCs is decreased on each rising edge of clk_d, which is the system clock (clk) with a delay of T_d = 5 ns. This delay guarantees that the output is stable before the feedback integration is performed. The values subtracted to UDC1 are 8 for y = '0' and 12 for y = '1'. In the case of UDC2, the values subtracted during the feedback integration are respectively 10 and 30. This combination of oscillation

frequencies, gains, and digital values has been determined following the procedure described in Section 4.4.

Figure 7.2 shows the output spectrum result from a behavioral simulation of the proposed system for a 1 kHz -20 dB_{FS} input tone. The SNDR measured is 68.27 dB, which increases up to 73.75 dB-A after A-weighting.

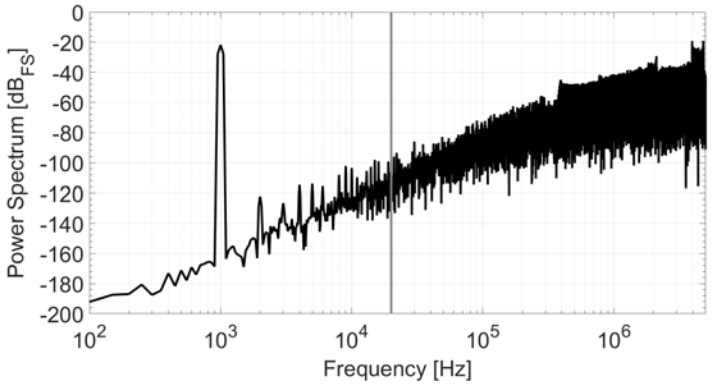


Figure 7.2: Output spectrum of a behavioral simulation for a 1 kHz -20 dB_{FS} input tone.

7.3 Circuit-level design

7.3.1 Voltage-controlled oscillator

Figure 7.3 depicts the schematic of VCO1, whose core is a current-controlled 5-stage ring oscillator. The control current is generated using a PMOS current source, whose gate voltage is externally generated. This transconductor topology is very sensitive to process and temperature variations, and it introduces distortion for large input voltages. Although this is not the optimal solution for a marketable product, it offers a versatility useful for a test chip.

Table 7.2 describes the dimensions and the values of the main transistors and components that make up the VCO. Figure 7.4 shows the simulated relationship between the oscillation frequency and the input voltage. Using this set of parameters, the nominal oscillation frequency

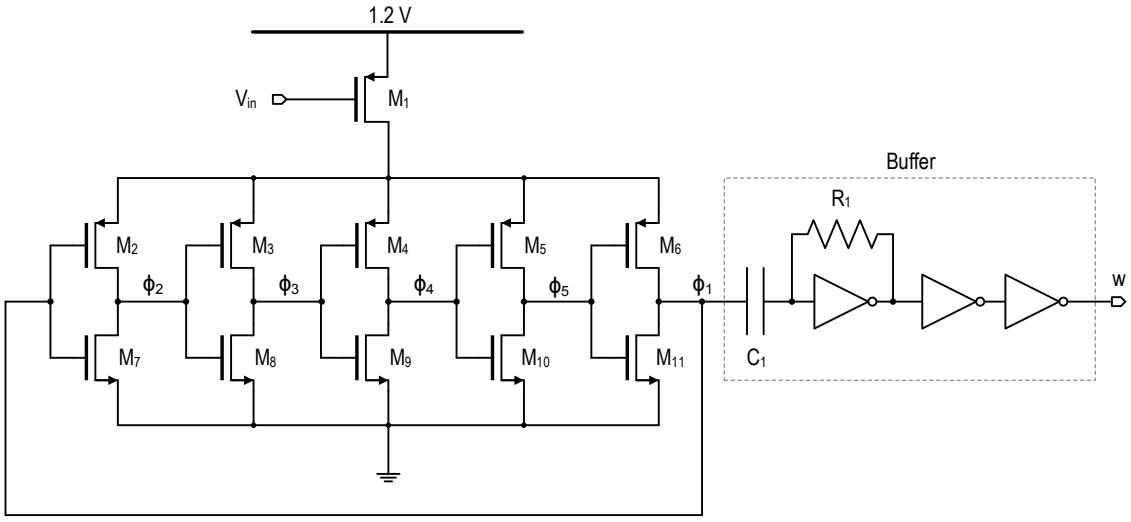


Figure 7.3: Proposed 5-stage current-controlled ring oscillator driven by a PMOS current source.

is reached when the input voltage is V_{in} = 567 mV, which implies that the drain current of M_1 is 58 μA. Under these conditions, the voltage levels of the oscillator phases are between 0 mV and 700 mV. Therefore, a buffer is required to generate an square oscillation compatible with digital circuitry. The proposed buffer consists of a coupling capacitor followed by three CMOS inverters, the first of them linearized with a feedback resistor.

Table 7.2: Components of the VCO shown in Fig. 7.3.

Device	W	L
M_1	48 μm	1.2 μm
$M_{2\text{-}6}$	40 μm	400 nm
$M_{7\text{-}11}$	20 μm	400 nm
Device	Value	
C_1	50 fF	
R_1	40 kΩ	

As mentioned in the introduction, the secondary objective of this test chip is to verify the input referred phase noise model described in Chapter 5. Therefore, the output of the VCO must be visible from the outside through one of the output pads. In order to minimize potential

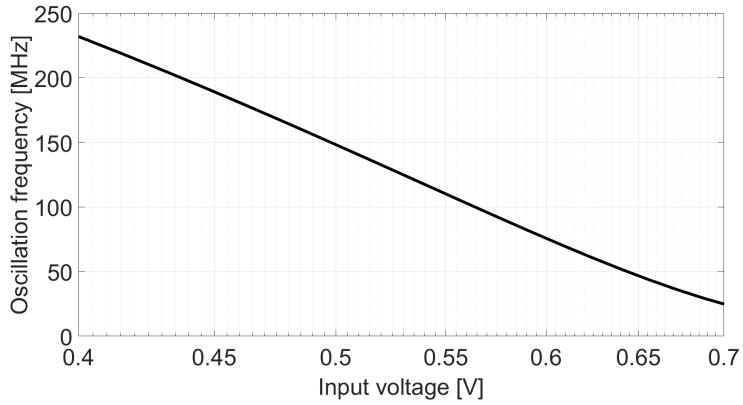


Figure 7.4: Simulated VCO oscillation frequency against input voltage.

interferences, the output of the VCO has been connected to an asynchronous frequency divider composed of three D-type flip-flop connected in cascade. Therefore, the oscillation frequency of the signal transmitted through the pads is divided by 8 (i.e., approximately 12 MHz for nominal conditions). Figure 7.5 shows the simulated phase noise at the output of the frequency divider, which will be taken as reference in Section 7.4.

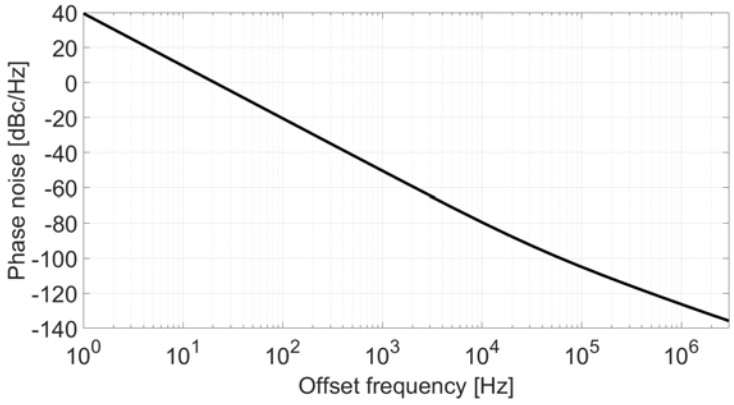


Figure 7.5: Simulated phase noise obtained after the frequency divider.

7.3.2 Digitally-controlled oscillator

The proposed digitally controlled oscillator is the combination of a multi-bit current DAC and a 5-stage current-controlled ring oscillator, as shown in Figure 7.6. Table 7.3 summarizes the dimensions of the transistors that compose the DCO.

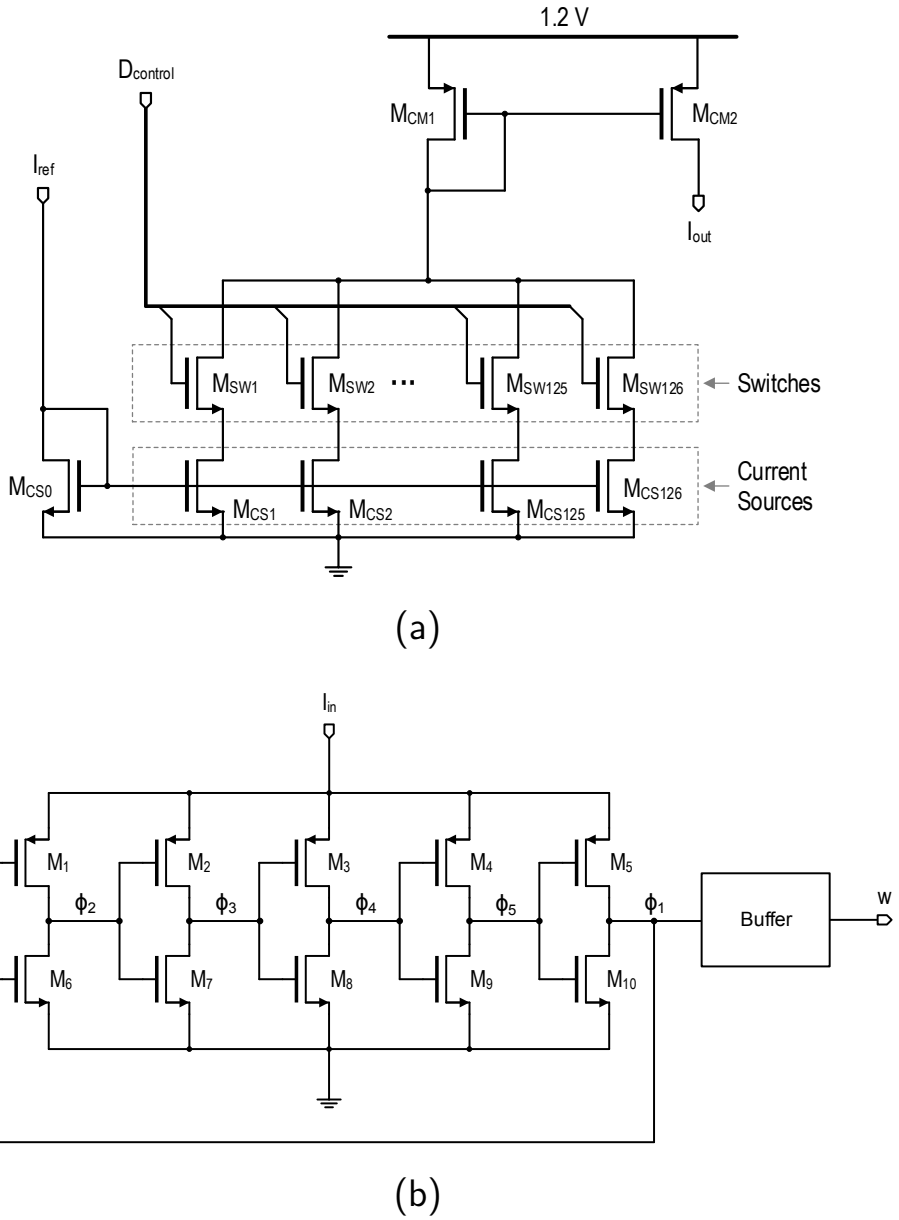


Figure 7.6: Proposed digitally controlled oscillator. (a) Multi-bit current DAC. (b) 5-stage current-controlled ring oscillator.

The IDAC is based on the reference current I_{ref} (of approximately 830 nA) provided by a bandgap circuit. This current is halved and copied to 126 elements ($M_{CS1\text{-}CS126}$), which can be enabled and disabled with the switches ($M_{SW1\text{-}SW126}$). The resulting current is copied and doubled by the current mirror ($M_{CM1\text{-}CM2}$), whose output current is directly injected to the CCO. From the 126 elements, 64 are connected to the output of UDC1 whereas the remaining 62 are reserved for trimming

Table 7.3: Components of the DCO shown in Fig. 7.6.

Device	W	L
M_{CM1}	144 μm	12 μm
M_{CM2}	288 μm	12 μm
$M_{SW1\text{-}SW126}$	2 μm	400 nm
M_{CS0}	4 μm	6 μm
$M_{CS1\text{-}CS126}$	2 μm	6 μm
$M_{1\text{-}5}$	12.5 μm	400 nm
$M_{6\text{-}10}$	5 μm	400 nm

purposes. The trimming elements are grouped in 5 clusters (of 32, 16, 8, 4, and 2 elements), which are controlled by 5 bits. In the nominal case, 26 elements are enabled providing a current of approximately 21.6 μA. Figure 7.7 shows the simulated IDAC current for 65 possible input codes.

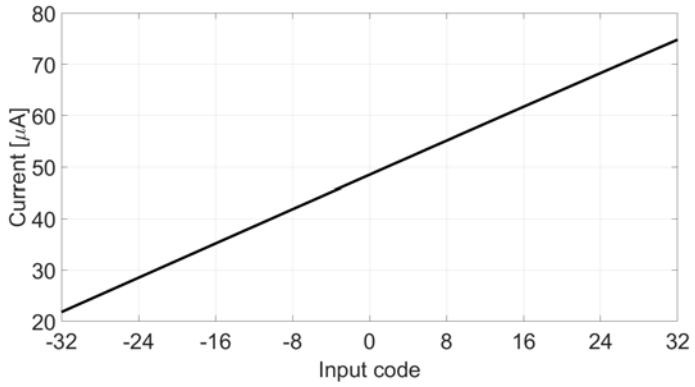


Figure 7.7: Simulated IDAC current against digital code.

The current controlled oscillator depicted in Figure 7.6(b) consists of a 5-stage ring of CMOS inverters, whose delay depend on the current generated by the IDAC. Figure 7.8 displays the relationship between the input code and the CCO oscillation frequency. It can be observed that for the oscillation frequency reached for null input is 209 MHz, which is slightly higher than the target nominal frequency (200 MHz). Nevertheless, simulations show that this difference does not have a significant impact on the system performance.

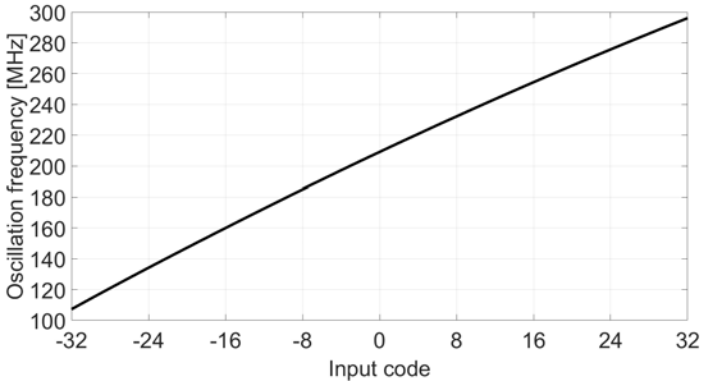


Figure 7.8: Simulated CCO oscillation frequency against digital code.

7.3.3 Digital circuitry

Both UDCs have been implemented based on a semi-custom design flow using Cadence®. Figure 7.9 depicts the simplified schematic of the implemented UDC1, which consists of two digital accumulators. The first accumulator is driven by the output of CCO1 (w), and increases its value in 1 unit each CCO1 rising edge. On the other hand, the second accumulator is driven by the delayed clock (clk_d), and its value is increased on $D_1(0) = 8$ or $D_1(1) = 12$, depending on the ADC output (y). The value of both accumulators is combined through a synchronization logic, which periodically decreases the values of both accumulator to avoid their saturation. The difference between the two accumulators is processed using a rotatory algorithm, which generates the 64 control signals for the current DAC of the second stage mimicking the operation of the DWA algorithm described in Fig. 4.7(b).

The second up-down counter is considerably simpler because it is directly connected to a single-bit clocked quantizer. On one hand, given that the output of UDC2 is not used to control a multi-bit DAC, there is no need for a rotatory algorithm. On the other hand, the output of both accumulators does not need to be continuously combined, and the subtraction can be performed at the end of the sampling period, using the system clock.

Unfortunately, circuit-level simulations revealed a malfunction in the operation of the complete system. Figure 7.10 shows the output spec-

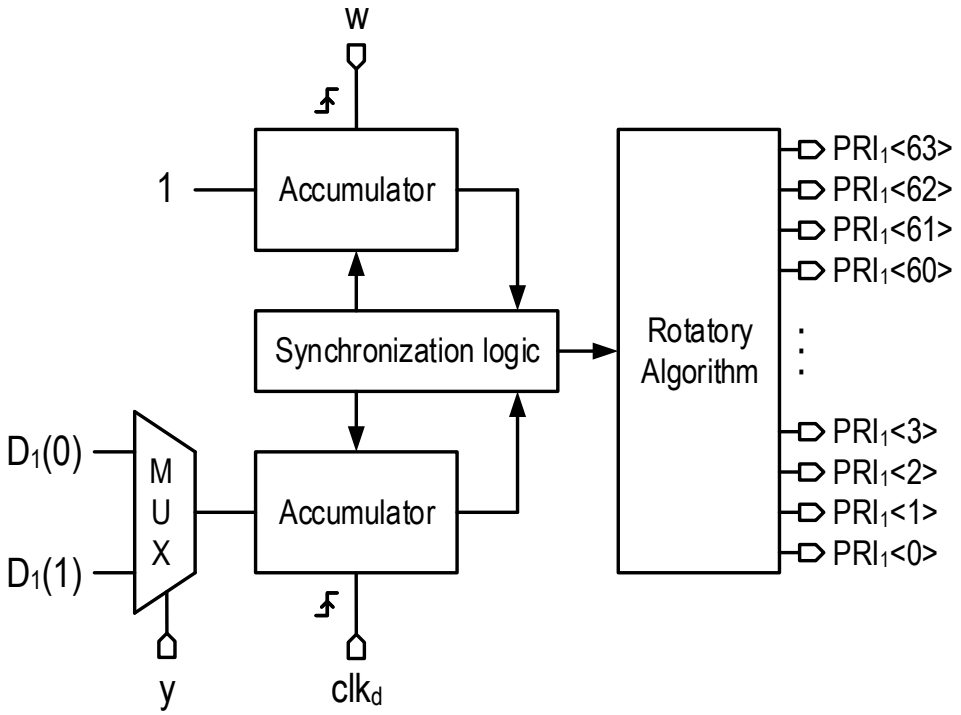


Figure 7.9: Simplified diagram of the proposed UDC1.

trum result from a simulation of the proposed system for a 5 kHz -20 dB_{FS} input tone. Note that the simulated noise spectral density shows only first order noise shaping, and the distortion is unexpectedly high for the input amplitude used. The resulting SNDR and SNR are respectively 34.68 dB and 52.54 dB, which are considerably below the target performance obtained in the system-level simulation of Fig. 7.2. Further simulations have shown that the loss of performance has its origin in the wrong operation of both UDCs, in spite of the efforts devoted to design up-down counters robust against synchronization problems.

7.4 Experimental results

The proposed oscillator-based second order ΣΔ modulator has been fabricated in 130 nm standard CMOS technology. However, given that we were not able to fix the malfunction in the digital circuitry before the tape out to fabrication, the resulting test chip has been used to verify the input referred phase noise model described in Section 5.2.2. Figure 7.11 depicts the die micrograph of this chip.

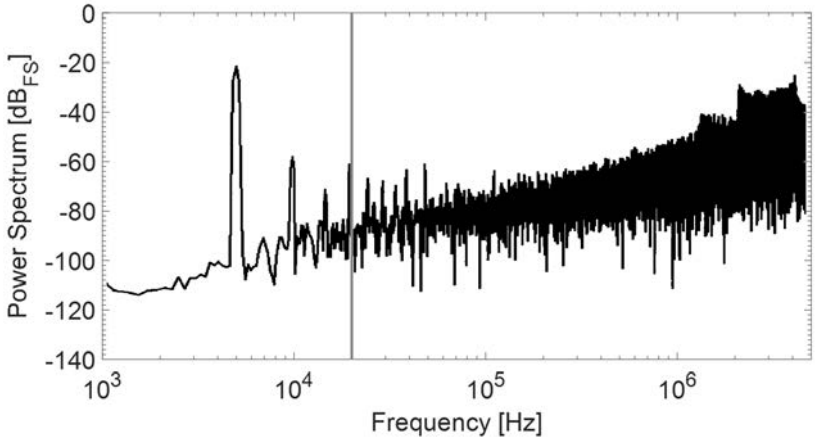


Figure 7.10: Output spectrum of a circuit-level simulation for a 5 kHz -20 dB_{FS} input tone. Unexpected distortion and loss of second order noise shaping reveal a malfunction in the operation of the up-down counters.

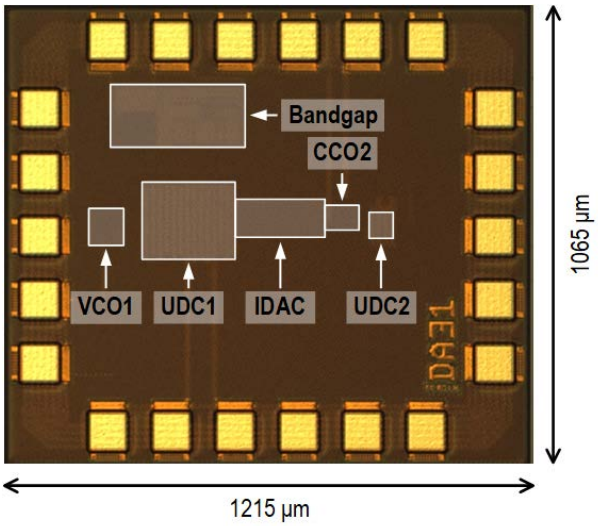


Figure 7.11: Die micrograph.

Figure 7.12 illustrates the experiment carried out based on the prototype fabricated. The idea is to measure the spectrum of the oscillation using an spectrum analyzer, whose output is processed applying the input referred phase noise equations. The resulting noise is compared to output of an XOR-based F2D converter emulated in MATLAB®. The sampling frequency must be high enough to keep quantization noise (which in this case show first order noise shaping) below the contribution

of phase noise at low frequencies. In this case, the sampling frequency chosen is 1 GHz. Due to equipment limitations, the spectral characteristics below 1 kHz can not be accurately captured. In consequence, we have analyzed the noise in the band from 5 kHz to 50 kHz instead of in the audio band.

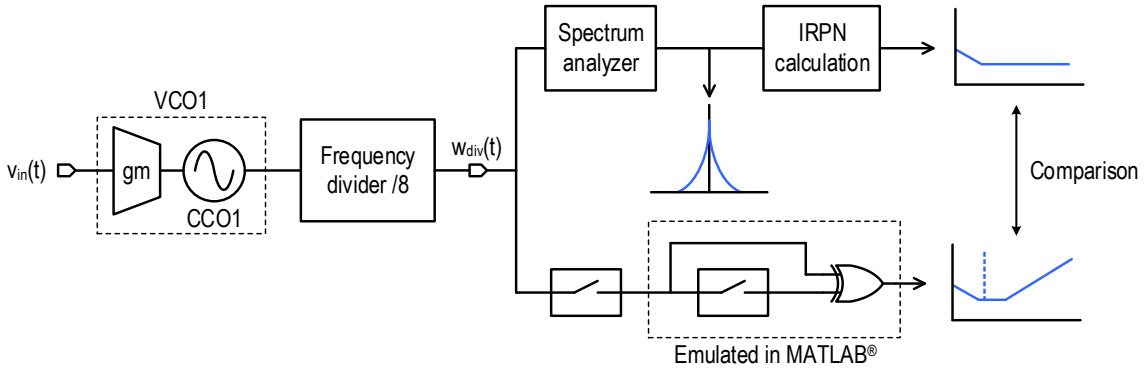


Figure 7.12: Experiment overview.

Firstly, the oscillation frequency response has been characterized by a DC sweep at the VCO input, as shown in Figure 7.13. Note that measured oscillation frequencies are slightly below the simulated frequencies (see Fig. 7.13) divided by 8, due to the influence of parasitics and process variations. We have taken 12 MHz (i.e., 96 MHz before the divider) as center oscillation frequency, which is reached when the input signal is 500 mV. The gain of the VCO can be obtained from this plot by calculating the slope of this graph around the point (v_{in} = 500 mV, f_0 = 12 MHz). In this case the absolute value of the slope is about K_{VCO} = -76.4 MHz/V, what leads to k_d = -6.4 V^{-1}.

After this, the oscillator has been connected to a frequency stabilization loop, as shown in Figure 7.14. We have used the phase and frequency comparator available in the commercial integrated circuit 74HC4046A (*PC2* output). This loop, whose bandwidth is well below the band of interest, keeps the oscillation frequency centered at 12 MHz compensating any undesired slow frequency drift, and enabling more accurate measurements of $S_w(f)$ with a spectrum analyzer.

This test fixture has been used to measure and calculate the graphs presented in Figure 7.15. Figure 7.15(a) shows the spectrum of the oscillation around f_0, which has been used to estimate the phase noise

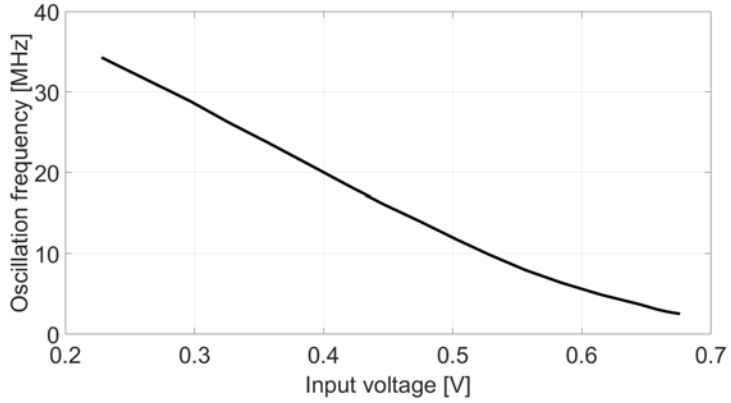


Figure 7.13: Measured oscillation frequency vs. input voltage.

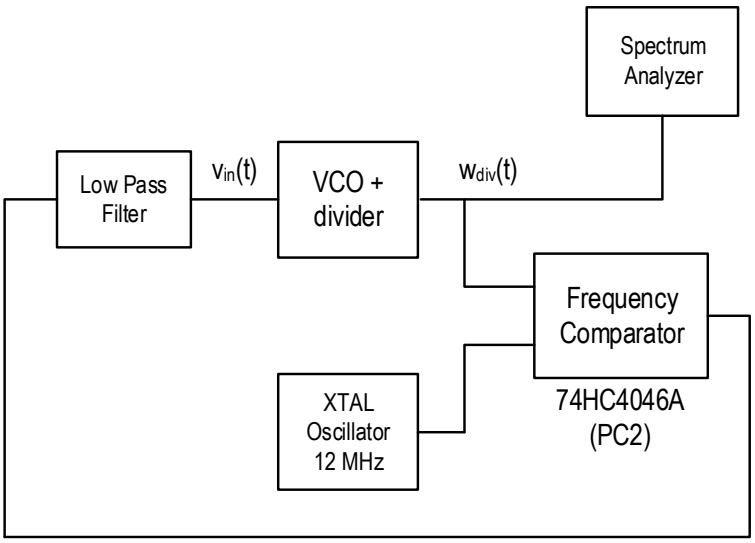
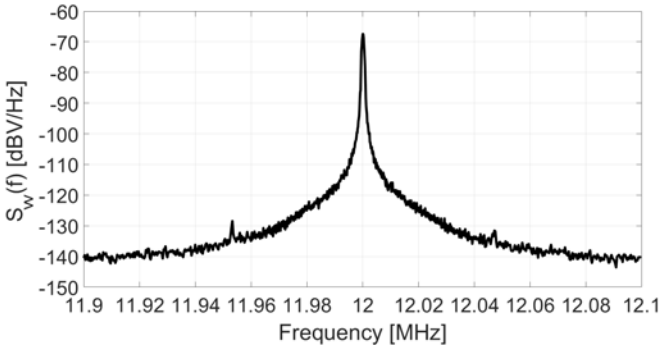
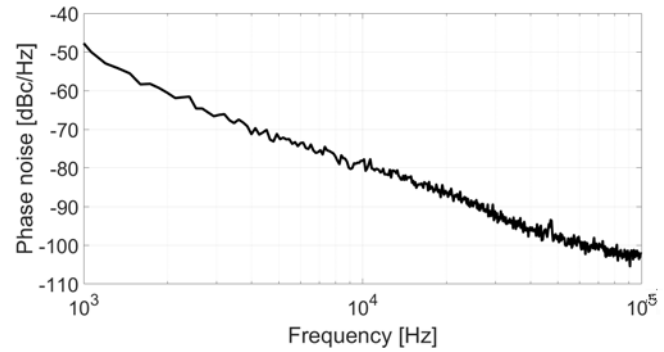


Figure 7.14: Test fixture for phase noise measurements.

depicted in Figure 7.15(b) by applying equation (5.4). Note that the result is very close to the simulated phase noise shown in Fig. 7.5, except for the unexpectedly high noise around 20 kHz. Input referred phase noise is calculated by applying equation (5.11) to the measured phase noise.The result is presented in Figure 7.15(c) together with the PSD of the output of the ADC properly scaled by the inverse of the ADC gain. Equation (5.13) can be used to calculate the SNR due to phase noise. We take as example a 0.55 $\mathrm{mV_{peak}}$ input tone and a band of interest from 5 kHz to 50 kHz. The noise power obtained by numerically integrating $S_r(\Delta f)$ across this band is 11.6 $\mu\mathrm{V}^2$, and therefore the SNR predicted is 41.16 dB.



(a)



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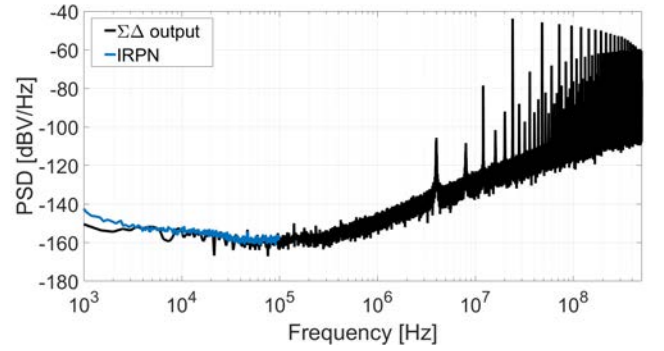


(c)

Figure 7.15: (**a**) $S_v(f)$ measured with an spectrum analyzer; (**b**) Phase noise derived from $S_w(f)$; (**c**) Comparison between the IRPN calculated from $\mathcal{L}(\Delta f)$ and the DFT of the measured ADC output.

After the idle channel measurement, the test fixture has been modified adding a balun transformer at the VCO input in order to inject a modulating signal in the loop without modifying the conditions used in

the previous measurement. A tone of 0.55 mV_{peak} at 15 kHz has been added to the input of the VCO. Figure 7.16 shows the power spectrum of the converter after applying the same post-processing than in the previous measurement. The SNR obtained from this test is 42.72 dB in the bandwidth from 5 kHz to 50 kHz. Therefore, the deviation between theory and simulation is less than 2 dB.

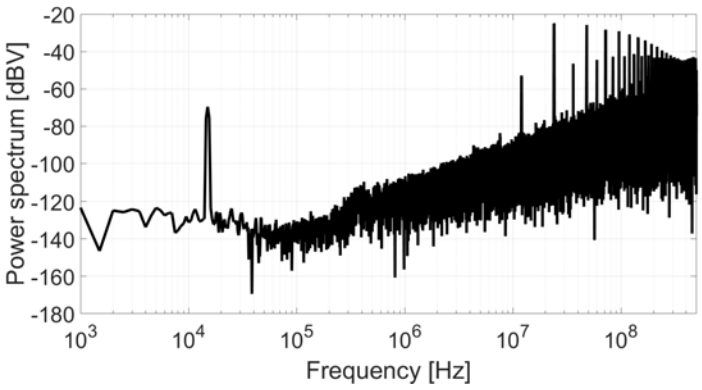


Figure 7.16: Power spectrum of the ADC output.

7.5 Conclusion

In this chapter we have designed a second-order oscillator-based ΣΔ modulator implemented in 0.13 μm CMOS technology. The proposed chip consists of two oscillators connected to two multi-bit up-down counters. Feedback integration has been implemented using digital circuitry, as described in Chapter 4. Given the complexity of the system, logic synthesis tools have been used to implement both UDCs. Unfortunately, digital circuitry shows a malfunction, and second-order noise shaping has not been achieved. We believe that the malfunction has been caused by an error in the logic synthesis process, which was not optimized for the design of digital systems with multiple asynchronous clock signals, as is the case of the UDCs described in Section 4.3. In order to prevent these errors, we propose the design and implementation of a second-order oscillator-based ΣΔ modulator using simpler single-bit up-down counters. This implementation will be presented in Chapter 8.

On the other hand, the first VCO has been used to evaluate the

accuracy of the calculations presented in Chapter 5, comparing its input referred phase noise with its output spectrum. The difference between the estimation of our theoretical model and computer simulations differ from practical measurements in less than 2 dB, confirming the validity of the analysis methodology.

CHAPTER 8

Chip 2: Second-order oscillator-based $\Sigma\Delta$ modulator with single-bit PRIs

8.1 Introduction

In this chapter we address the redesign of the second-order oscillator-based $\Sigma\Delta$ modulator described in Chapter 7. Given that the malfunction detected in the previous prototype has been linked to the complexity of the multi-bit architecture and the logic synthesis methodology, we have decided to implement a second-order oscillator-based $\Sigma\Delta$ modulator with single-bit PRIs.

The proposed converter consists of two single-ended branches which can be combined in a pseudo-differential architecture, making it compatible with both single-ended and differential capacitive MEMS microphones. The sampling frequency is 20 MHz, which is potentially compatible with the MIPI SoundWire® standard. The single-ended configuration occupies an active area of 0.02 mm^2 in standard 0.13 μm CMOS technology, is powered at 1.8 V with a current consumption of 155 μA, and achieves an A-weighted dynamic range of 98 dB-A. The

pseudo-differential configuration achieves 103 dB-A of A-weighted dynamic range, at the expense of doubling the area and power consumption. The results presented in this chapter have been recently published in [89].

8.2 System-level design

Fig. 8.1 depicts the block diagram of the proposed VCO-based second-order ΣΔ modulator. The system consists of two single-ended branches, each of them composed of a VCO, a DCO, two UDCs, and a feedback generator (FB). For the sack of simplicity, in the following paragraphs we focus on only one of the branches.

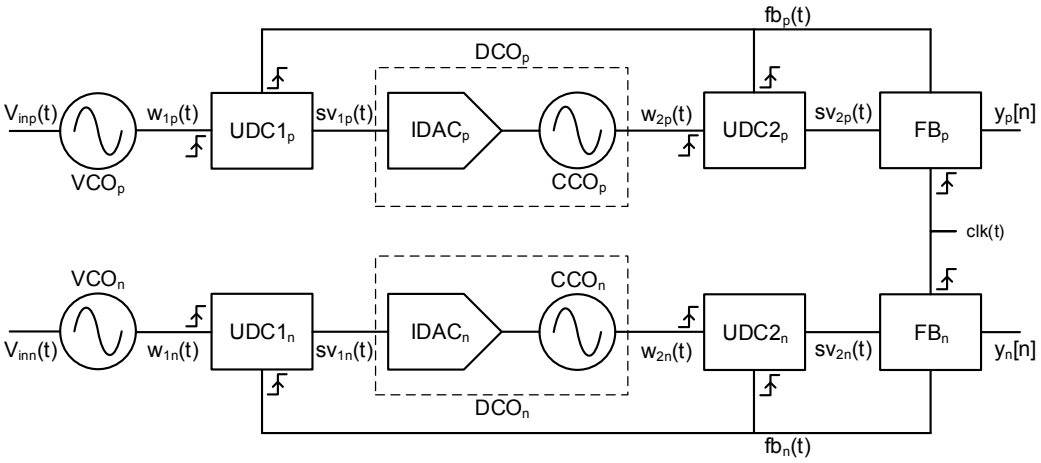


Figure 8.1: Simplified block diagram of the proposed second-order oscillator-based ΣΔ ADC with single-bit interconnections.

Similarly to the systems described in Chapters 3 and 4, the proposed converter replaces classical integrators with phase referenced integrators. However, there are two major differences between this modulator and the previous test chip. On one hand, the output of both up-down counters (i.e., UDC1 and UDC2) is single-bit, which can only take the values '0' and '1'. In consequence, the digitally controlled oscillator has only two possible oscillation frequencies. On the other hand, as a necessary condition to keep all the interconnections single-bit, the values subtracted to the up-down counters throught the feedback path are restricted to '0' or '1', depending on the modulator output (i.e., $D_1(y) = D_2(y) = y$).

This eliminates the need for a complex logic function implementation to subtract a variable amount to a multi-bit UDC. Instead, a feedback generator can be used to generate a feedback only when the UDCs need to be decreased (i.e., when the value sampled is '1') and remain static when the output is '0'. In consequence, the feedback input of the up-down counters can be responsive to rising edges, and the need for a clock signal is eliminated.

The input voltage controls the oscillation frequency of the VCO, whose output is the FM signal $w_1(t)$. The center oscillation frequency is $f_0 = 4.8$ MHz and the oscillator gain is $K_{VCO} = 7.2$ MHz/V (the relative frequency deviation is $k_d = K_{\mathrm{VCO}}/f_0 = 1.5$ V^{-1}). Assuming a maximum input swing of ±320 mV (for 125 dB$_{\mathrm{SPL}}$), the oscillation frequency falls then within the range of 2.5 MHz to 7.1 MHz. "UDC1" is a 1-bit up-down counter, whose value is increased on each rising edge of $w_1(t)$ and decreased on each rising edge of the feedback, $fb(t)$. The output of this UDC is fed into the second stage, which consists of a DCO and a second UDC. The DCO consists of a current DAC (IDAC) followed by a CCO. The CCO can oscillate at only two different frequencies: $f_{low} = 2.5$ MHz when UDC1 is '0', and $f_{high} = 9.5$ MHz when UDC1 is '1'. Therefore, we can define the sensitivity of the DCO as $K_{DCO} = 7$ MHz/code. Finally, the output of UDC2 is sampled by FB, which also generates the feedback pulse $fb(t)$ with a delay of $T_d \approx 2$ ns. This delay is intentionally generated to ensure that the output value used to generate the feedback pulse is stable. Table 8.1 summarizes the main parameters of the proposed system.

This set of parameters has been chosen with two goals. On one hand, these parameters must be chosen to place the poles and the zeros in the correct position to achieve the target NTF and STF, as described in Chapter 4. On the other hand, the appropriate selection of frequencies and coefficients is required to avoid the saturation of the 1-bit UDCs. The oscillation frequencies of both oscillators must be lower than the sampling frequency in order to avoid that two rising edges of the same oscillator are produced before a feedback pulse is generated to reset the UDCs. In addition, given that a rising edge of the DCO is required to generate the feedback pulse, f_{high} must be kept above the maximum

Table 8.1: Parameters of the proposed oscillator-based ADC.

Parameter	Value	Parameter	Value
K_{VCO}	7.2 MHz/V	K_{DCO}	7 MHz/code
f_{VCO_0}	4.8 MHz	f_{DCO_0}	2.5 MHz
$D_1(0)$	0	$D_2(0)$	0
$D_1(1)$	1	$D_2(1)$	1
d_1	1	d_2	1
f_s	20 MHz	Input full-scale	±320 mV
T_d	2 ns	AOP	125 dB_{SPL}

oscillation frequency of the VCO. Finally, equations (4.14) and (4.16) must be taken into account to guarantee that the average value of y, sv_1, and sv_2 is contained between 0 and 1.

Fig. 8.2 illustrates the behavior of one of the channels of this VCO-ADC with the set of parameters proposed, considering $T_d \approx 0$ for simplicity. At instant t_1, the rising edge in $w_1(t)$ sets the output of the UDC1 ($sv_1(t)$) to '1'. When this happens, the frequency of the DCO changes from f_{low} to f_{high}, so its phase ($\varphi_{DCO}(t)$) climbs at higher rate. At t_2 this phase reaches 2π, which generates a rising edge on $w_2(t)$ and therefore $sv_2(t)$ is set to '1'. At t_3, the rising edge of the clock *clk* samples

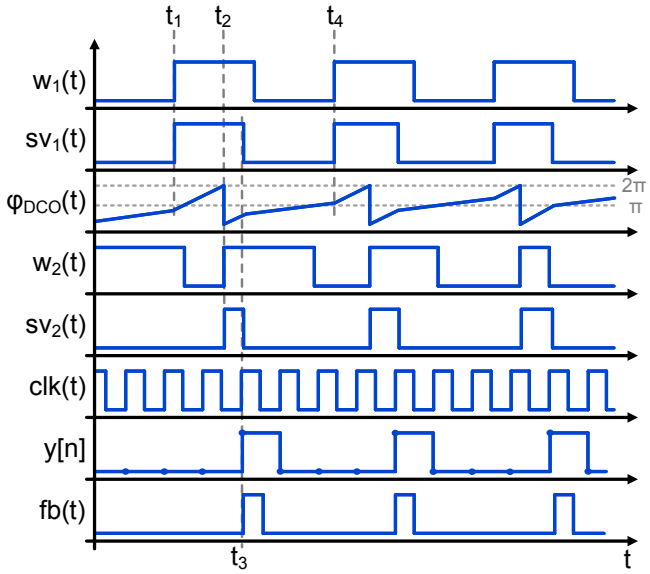
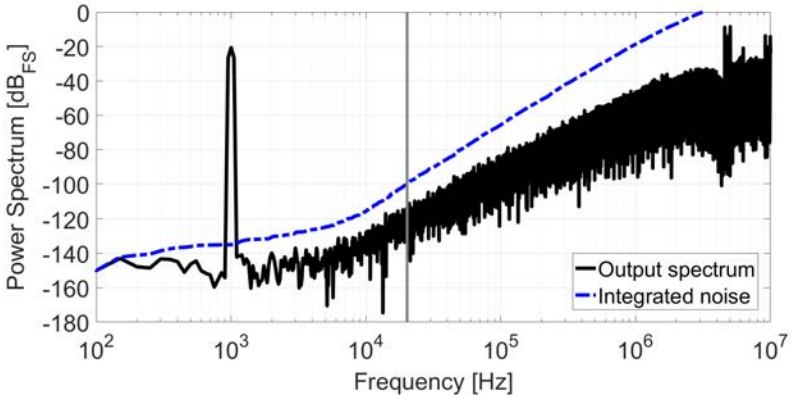


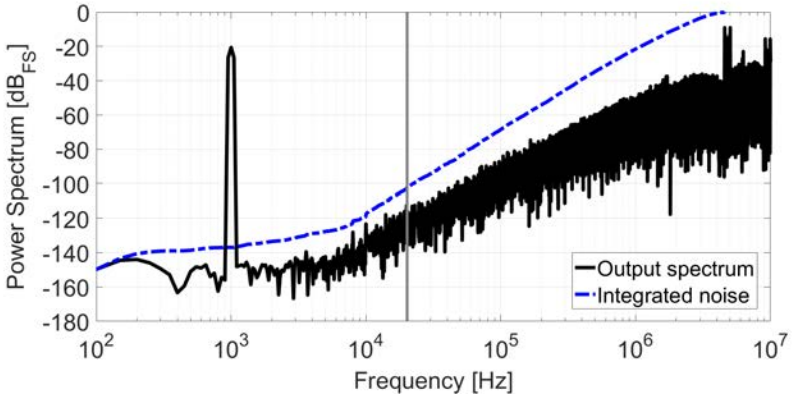
Figure 8.2: State variables of one of the branches of Fig. 8.1.

for first time when $sv_2(t) = 1$, generating a short pulse in $fb(t)$ which clears both UDCs. This sets the oscillation frequency of the DCO back to f_{low} until t_4, the next rising edge of $w_1(t)$.

Figs. 8.3 and 8.4 show the result of behavioral simulations of the proposed system for two different input signals assuming ideal conditions. Second order noise shaping is clearly visible in both single-ended and pseudo-differential configurations. Simulations shown in Fig. 8.3 have been computed applying a -20 dB_{FS} input tone at 1 kHz. The SNDR obtained in the single-ended converter (Fig. 8.3(a)) in 20 kHz is 81.4 dB, which increases up to 88 dB-A using A-weighting. In the case of the pseudo-differential converter (Fig. 8.3(b)), the SNDR is 83.8 dB



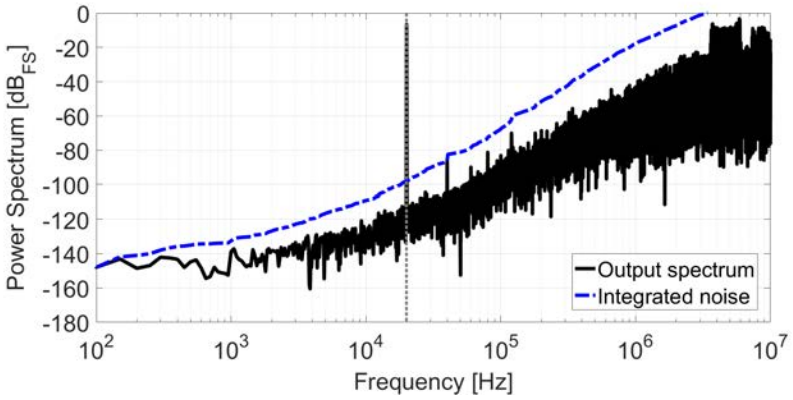
(a)



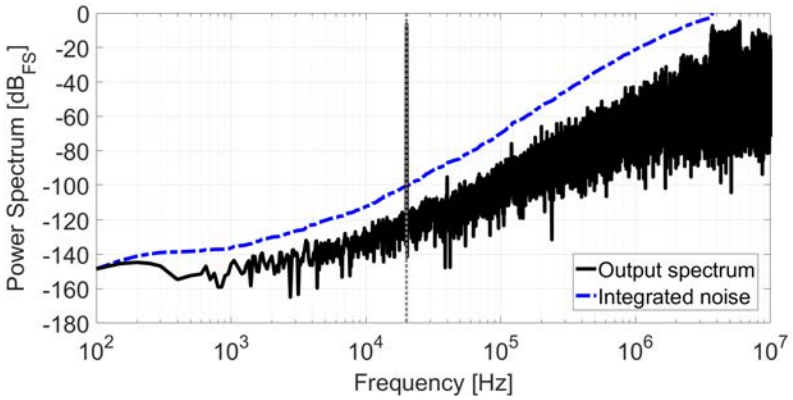
(b)

Figure 8.3: Simulated spectra for an input signal of -20 dB_{FS} at 1 kHz. (a) Single-ended converter. (b) Pseudo-differential converter.

(90.4 dB-A). Fig. 8.4 shows the simulated spectra of both configurations for a -6 dB_{FS} and 20 kHz input tone. The SNR obtained from these simulations is respectively 93.3 dB and 95.9 dB.



(a)



(b)

Figure 8.4: Simulated spectra for an input signal of -6 dB_{FS} at 20 kHz. (a) Single-ended converter. (b) Pseudo-differential converter.

However, the performance obtained by simulation is difficult to achieve in silicon due to the nonidealities mentioned in Section 4.5. Firstly, the nonlinear relationship between the input voltage and the oscillation frequency of the first oscillator injects distortion, which limits the SNDR for large input signals. This is a major disadvantage in several applications, and makes mandatory the use of linearity correction techniques [20, 90, 91]. However, as explained in appendix A, audio applications typically tolerate a certain level of distortion for very large input signals. Therefore, the target levels of linearity may be reached

without any distortion compensation mechanism. In addition to distortion, phase noise may also limit the resolution of the VCO-ADC for any input amplitude. Although both the VCO and the DCO generate phase noise, the phase fluctuations produced by the VCO of the first stage typically dominate over the phase noise generated at the second stage, given that any noise injected into the second stage is high-pass filtered by the system loop.

Another important nonideality that must be considered is the jitter of the sampling clock which, as explained in Section 4.5, is the random variation of the sampling period. The impact of clock jitter in the performance of the system is strongly dependent on the modulator topology, specially on the feedback mechanism. Given that in this VCO-based ΣΔ modulator the integration of the feedback is done in discrete time, the proposed system shows better tolerance to clock jitter than classical CT ΣΔ with continuous time feedback integration. Fig. 8.5 shows the SNDR of the proposed system at -20 dB_{FS} for different values of clock jitter. It can be observed that the SNDR is almost constant up to a jitter standard deviation of 1% of the ideal sampling period (T_s).

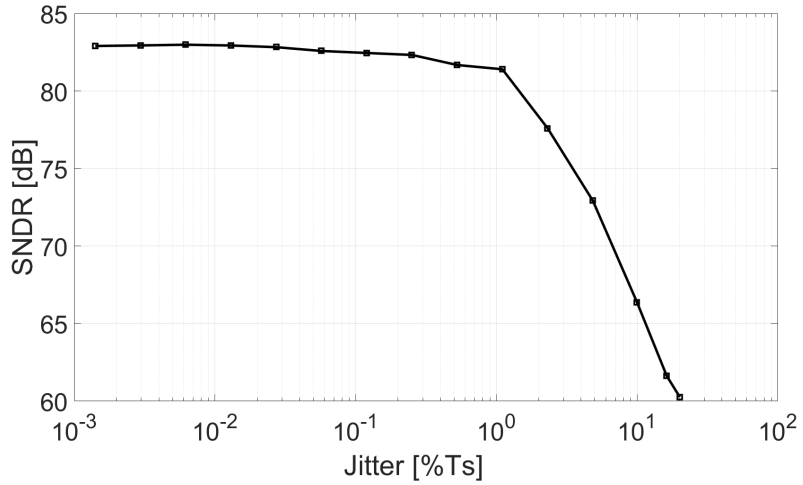


Figure 8.5: Simulated SNDR at -20 dB_{FS} for different values of clock jitter standard deviation referred to the ideal sampling period.

Finally, metastability may be a problem in the digital circuitry due to the non-synchronization between the oscillators and the sampling clock. On one hand, both UDCs have two inputs: the feedback pulse which is synchronized with the sampling clock, and the oscillation which is

asynchronous. The potential conflict arises when a rising edge happens in both inputs almost simultaneously. The UDC must be capable of handling this situation (at least in the wide majority of the cases), so both edges are properly taken into account. On the other hand, the feedback generator also has two inputs: the sampling clock, and the output of the UDC2 whose rising edges are asynchronous while the falling edges are synchronized with the feedback pulse and therefore with the sampling clock.

8.3 Circuit-level design

8.3.1 Voltage-controlled oscillator

As stated before, the VCO of the first stage deserves special attention because it performs the critical voltage-to-frequency conversion of the input signal, which sets the limit in the maximum achievable resolution of the ADC. Fig. 8.6 shows the proposed VCO, which is composed of a 3-stage single-ended voltage-controlled ring oscillator followed by a buffer and a level-shifter. As mentioned before, ring oscillators are widely used in VCO-ADCs [27, 46, 48] due to their sensitivity and low phase noise.

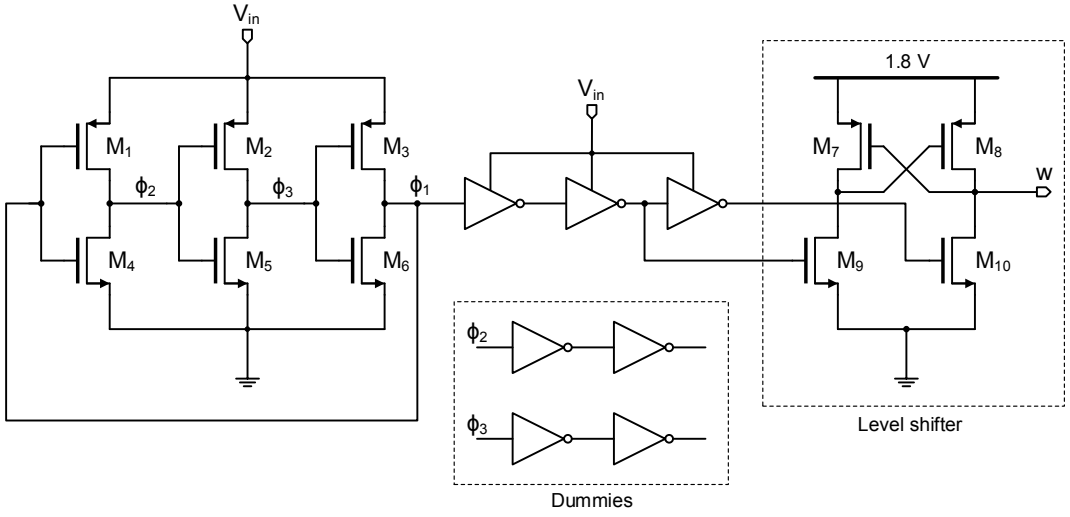


Figure 8.6: Proposed 3-stage single-ended voltage-controlled ring oscillator.

Another advantage of these oscillators is that they can be used in multibit configurations using the multiple phases of the ring. However, given that our priority is simplifying the digital circuit that follows the oscillator, we only use one of the outputs of the ring oscillator. Table 8.2 shows the dimensions of the transistors used in this circuit.

Table 8.2: Components of the VCO shown in Fig. 8.6.

Device	W	L
M_1 - M_3	72 μm	8 μm
M_4 - M_6	48 μm	8 μm
M_7 - M_8	1 μm	400 nm
M_9 - M_{10}	4.8 μm	400 nm

With these dimensions, the target oscillation frequency and gain (i.e., $f_0 = 4.8$ MHz and $K_{VCO} = 7.2$ MHz/V) are reached when the DC input voltage is 1.1 V for nominal conditions. However, temperature and process variations alter the oscillation frequency for a given DC input voltage. Monte Carlo simulations show that the standard deviation of the oscillation frequency at 1.1 V is approximately 250 kHz. Very high oscillation frequencies may result in the saturation of UDC1 for high input levels. In contrast, lower oscillation frequencies imply lower VCO sensitivity, which attenuates the input signal (see Figure 4.16). Moreover, lowering the VCO frequency increases the power of PFM harmonics, which may degrade the performance of the modulator. System-level simulations have been used to check that the converter tolerates a variation of ± 1 MHz (4σ) without significant loss of performance.

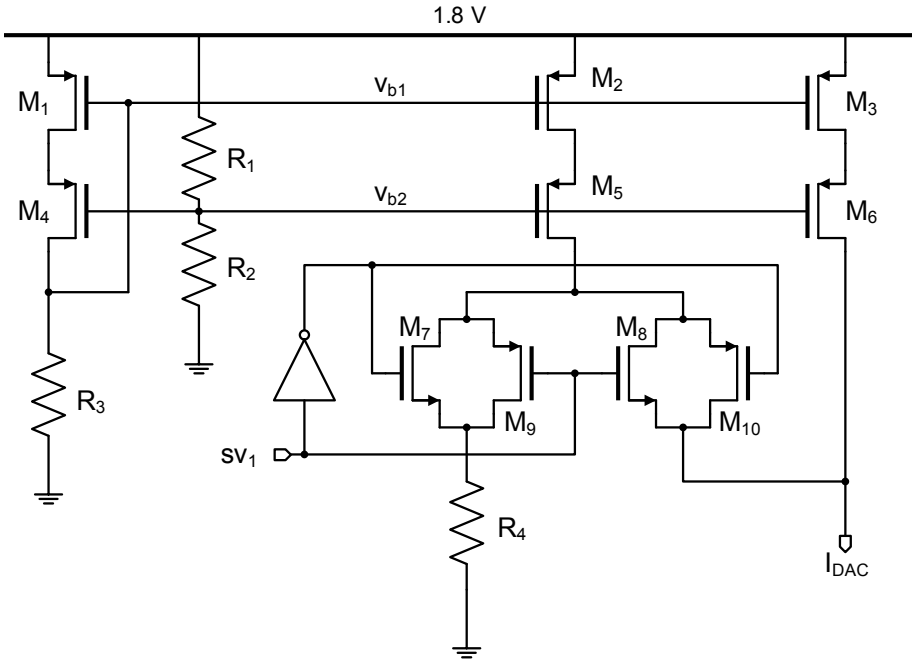
One of the phases of the ring oscillator (ϕ_1) is taken as the main output, and it is connected to a couple of inverters to square the oscillation. The amplitude of this oscillation depends on the supply of the inverters, so a level shifter is required to obtain an oscillation level compatible with the digital circuitry whose supply voltage is 1.8 V. The other two outputs of the ring oscillator, ϕ_2 and ϕ_3 are connected to dummy inverters in order to maintain the symmetry of the oscillator. The current consumption of the VCO (including inverters and level-shifter) is 75 μA at the center frequency.

8.3.2 Digitally-controlled oscillator

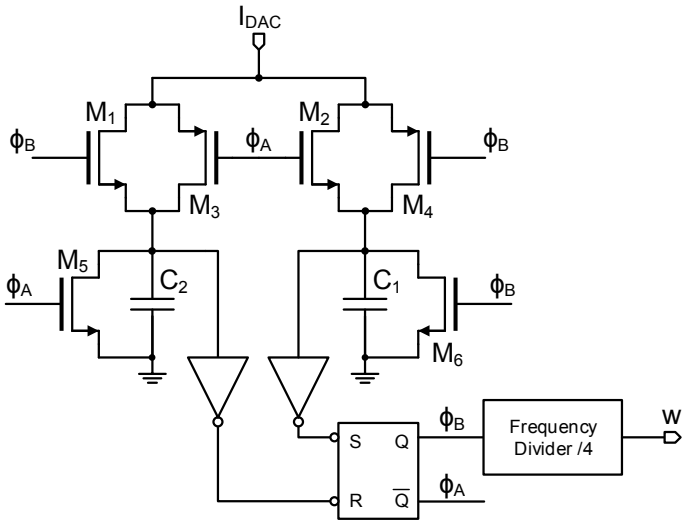
The DCO of the second stage can oscillate only at $f_{low} \approx 2.5$ MHz or $f_{high} \approx 9.5$ MHz, which has two interesting features: firstly, the oscillator is intrinsically linear because it can only oscillate at two different frequencies; secondly, given that these two frequencies are very different, the error introduced by random phase fluctuations (including power supply noise and the intrinsic phase noise of the oscillator) is in comparison small, and has less impact on the resolution of the ADC. However, given that the output of the first UDC consists of pulses which can be very short, the voltage-to-frequency response of the DCO must be fast enough to properly respond to these pulses, as was shown in Fig. 8.2. Note that errors introduced after the first integrator (VCO1) are high-pass filtered due to the system loop. Among many others possibilities, one solution is the combination of a 1-bit current DAC followed by the current-controlled oscillator (CCO) shown in Fig. 8.7.

The IDAC of Fig. 8.7(a) has a current source (M_3 and M_6) which drives 5 μA into the output. In addition, another current source (M_2 and M_5) generates 15 μA which is routed through an analog multiplexer ($M_7 - M_{10}$). When the control signal sv_1 is low, this current is thrown away through the resistor R_4 to maintain the current source properly biased. When sv_1 is high, the current is added to the output, so the total output current is 20 μA. The resistive voltage divider composed of R_1 and R_2 is used to generate the voltage reference for the cascodes (v_{b2}). Furthermore, R_1 generates a reference current of 5 μA, which in combination with M_1 and M_4 generates the voltage v_{b1}.

The CCO, shown in Fig. 8.7(b), is a relaxation oscillator in which two capacitors are alternately charged and discharged. When $\phi_A = \overline{\phi_B} = 1$, the current provided by the IDAC is used to charge the capacitor C_1 through M_2 and M_4, while C_2 is cleared by M_5. When the voltage of C_1 reaches the threshold voltage of the inverter to which it is connected (approximately 0.9 V), the set-reset (SR) flip-flop is toggled and the capacitors C_1 and C_2 exchange roles. Note that the output of this oscillator is digital without the need for a level-shifter. Using capacitors of 250 fF, the oscillation frequencies obtained are $f_{low} \approx 10$ MHz and



(a)



(b)

Figure 8.7: Proposed digitally controlled oscillator. (a) 1-bit current DAC. (b) Current-controlled oscillator.

$f_{high} \approx 38$ MHz, which have been divided by four with a frequency divider composed of two T-type flip-flops in cascade to obtain the target values. The total current consumed by the DCO, taking into account

the biasing circuit and the digital circuitry, is 55 μA.

Table 8.3: Components of the IDAC shown in Fig. 8.7(a).

Device	W	L	Device	Resistance
M_1, M_3, M_5, M_6	2.4 μm	800 nm	R_1	220 kΩ
M_2, M_5	7.2 μm	800 nm	R_2	140 kΩ
M_7 - M_8	1 μm	400 nm	R_3	240 kΩ
M_9 - M_{10}	2.5 μm	400 nm	R_4	40 kΩ

Table 8.4: Components of the CCO shown in Fig. 8.7(b).

Device	W	L
M_1, M_2, M_5, M_6	1 μm	400 nm
M_3, M_4	2.5 μm	400 nm
Device	Capacitance	
C_1,C_2	250 fF	

8.3.3 Digital circuitry

Appart from the two oscillators described in the previous subsections, each single-ended branch requires two UDCs and a feedback generator. The schematic of the UDCs is shown in Fig. 8.8. It can be observed that it is, in essence, similar to the phase and frequency comparator that can be found in some PLLs. Two D-type flip-flops FF1 and FF2 are set to '1' by rising edges on inputs *w* and *fb* respectively. When both flip-flops are '1', FF3 resets the flip-flops as shown in Fig. 8.9. This circuit behaves as a two-bit up/down counter whose output is a thermometric code. As stated in Section 8.2, with the set of frequencies chosen the counter only needs one bit, and therefore output "P_0" has not been used. System-level simulations have been run to check that neither of the UDCs gets saturated for any input level in the range of interest. This is similar to the simulations that are run in classical CT-ΣΔ modulator to estimate the size of the state variables. A potential source of errors is related to the pulse generated by FF3 to reset the other two flip-flops. While this

signal is active (low), neither FF1 nor FF2 can react to rising edges on their respective clock input ports. The duration of this pulse is set by the logic circuit that accompanies FF3, which ensures that the pulse is long enough to reset both FF1 and FF2. Circuit-level simulations show that the duration of this pulse is between a 600 ps and 1.4 ns, depending on temperature and process variations. We have checked by means of system-level simulations that the errors caused by receiving a rising edge in any of the inputs while flip-flops are being reset is not a significant a noise source compared to other dominant noise sources, such as the phase noise of the first oscillator.

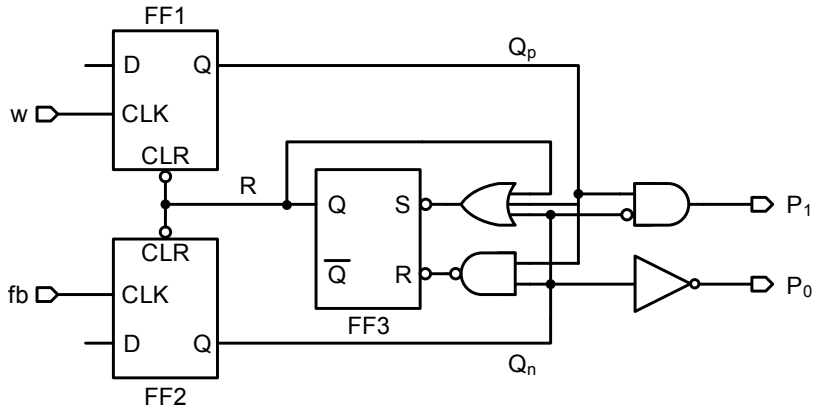


Figure 8.8: UDC diagram.

The feedback generator is depicted in Fig. 8.10. The first flip-flop (FF1), samples the output of the UDC2 (sv_2) and generates the output bitstream (y). The second flip-flop (FF2) samples the output with the clock delayed about 2 nanoseconds (clk_d), and sends a pulse through *fb* every time it samples a '1'. Note that this delay of 2 ns corresponds to the parameter T_d of Fig. 4.16. Fig. 8.11 describes the behavior of this circuit. In this case, FF1 may be sensitive to metastability because sv_2 and *clk* are not synchronized. However, the delay between *clk* and clk_d ensures that signal y is stable before it is sampled by FF2, so metastability errors are improbable. This has been checked by extensive circuit-level simulation.

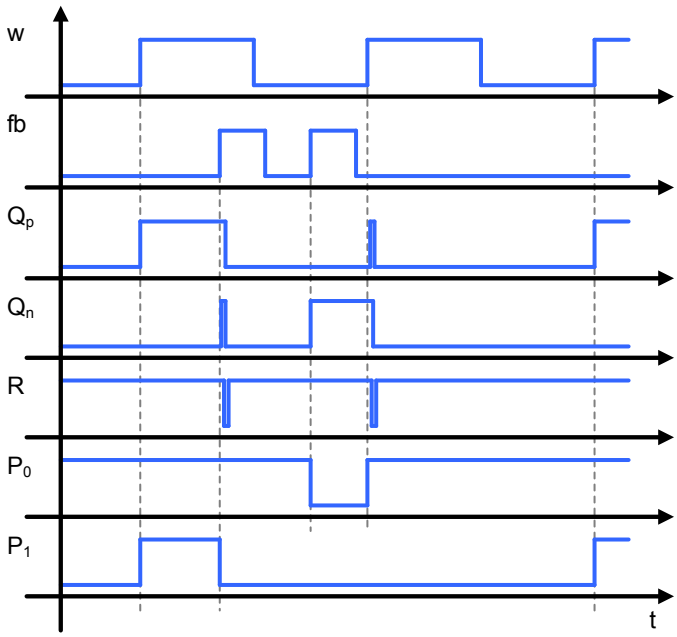


Figure 8.9: UDC behavior.

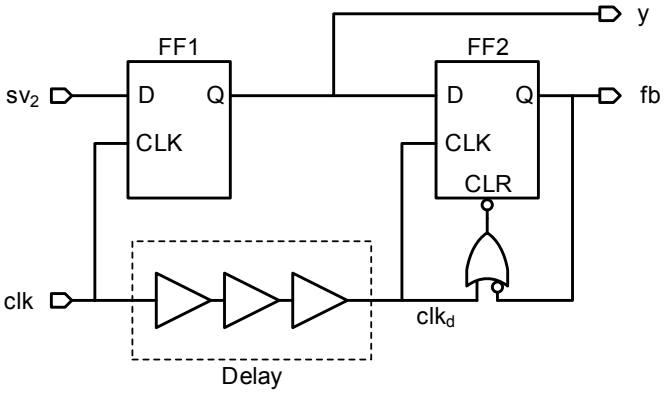


Figure 8.10: Feedback generator schematic.

8.4 Experimental results

The proposed second order VCO-based ΣΔ modulator has been fabricated in 130 nm standard CMOS, resulting in the integrated circuit shown in Fig. 8.12. Each single-channel modulator is laid out over the white rectangles marked in the die photo, which have a size of 330 μm x 100 μm. This area includes supplementary circuitry for testing purposes, but the active area of the chip occupies 0.02 mm^2 for each single-channel modulator and 0.04 mm^2 for the pseudo-differential converter. Each

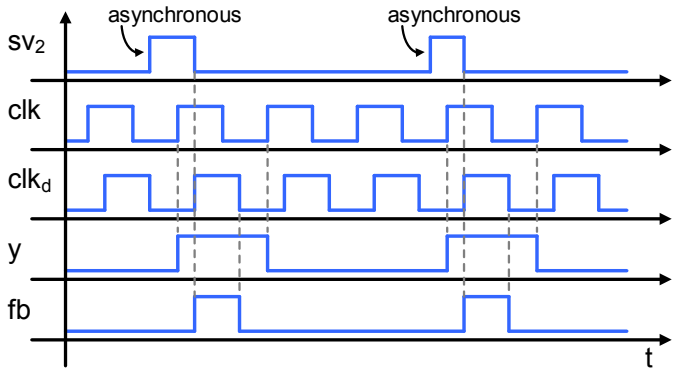


Figure 8.11: Feedback generator behavior.

channel has a pad for the input voltage, another for the output data bit-stream, and two multiplexed digital test pads to monitor internal signals, such as the outputs of the oscillators and the UDCs.

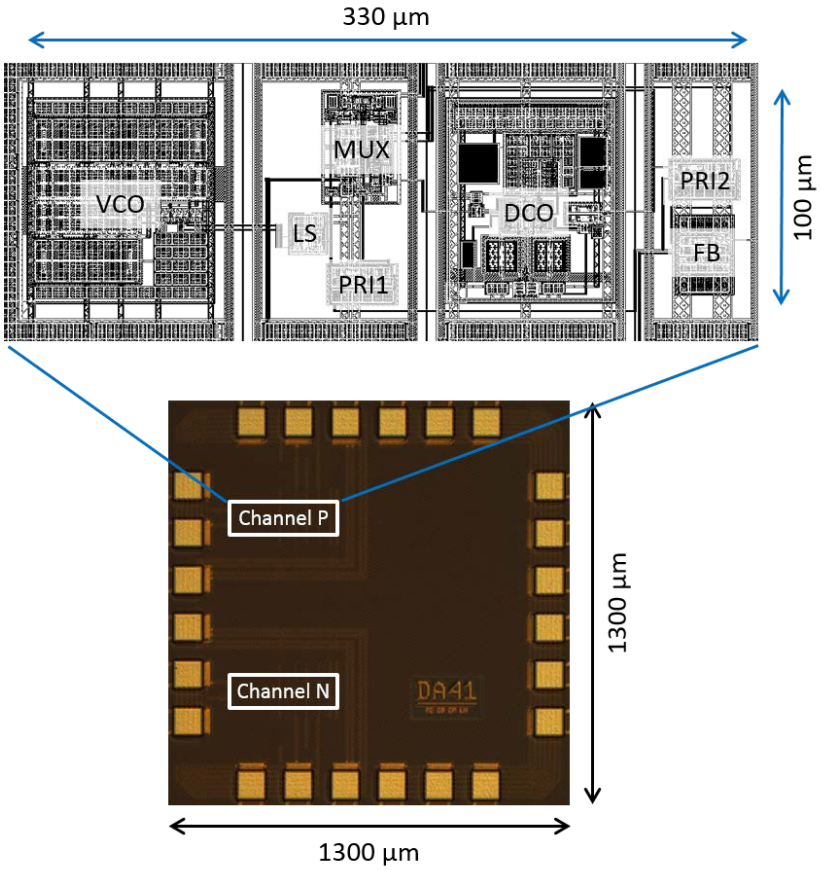


Figure 8.12: Die micrograph with dimensions.

The measured oscillation frequency for a 1.1 V of input DC voltage was slightly below the values obtained by simulation, and we had to

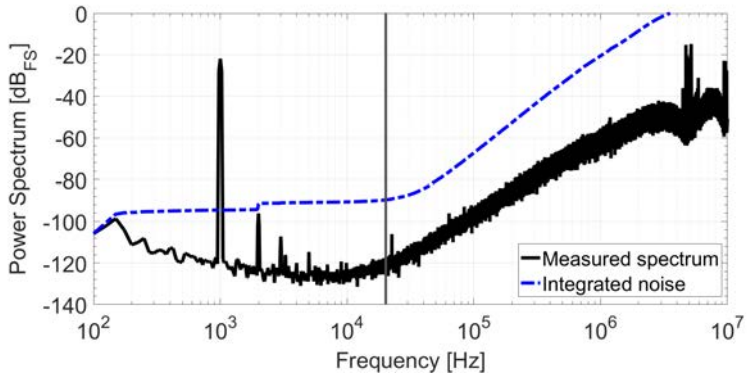
increase the DC level to 1.16 V in order to reach the nominal center oscillation frequency and oscillator gain (4.8 MHz and 7.2 MHz/V respectively). The digital test pads allow to measure the oscillation frequencies of the DCO, which are $f_{low} \approx 2.5$ MHz or $f_{high} \approx 9.5$ MHz.

Table 8.5: Performance summary and comparison with prior art

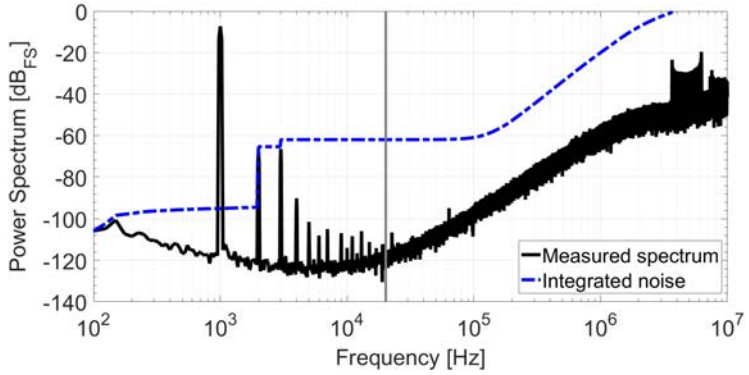
Parameter	**This ADC**		[2]	[3]	[92]	[93]	[94]	[95]	[96]
Tech. [nm]	**130**		180	160	180	40	28	160	180
VDD [V]	**1.8**		1.8	1.6	1.8	2.5/1.2	3.3/1	1.8	5/1.8
BW [kHz]	**20**		20	20	24	24	24	20	20
F_S [MHz]	**20**		2.4	3	6.144	6.5	24	11.29	2.56
$SNDR_{peak}$ [dB]	**69.6**	**76.6**	80	91.3	98.2	90	98.5	103	99.3
DR [dB]	**93.5**	**98.5**	96	103.1	103	102	100.6	109	101.3
DR [dB-A]	**98**	**103**	-	106	-	-	-	-	-
Power [mW]	**0.28**	**0.56**	0.73	0.39	0.28	0.5	1.13	1.12	1.1
FoM_S [dB]	**172**	**174**	170.4	180	182.3	179	173.8	181.5	173.9
Area [mm^2]	**0.02**	**0.04**	0.4	0.21	1.25	0.05	0.022	0.16	0.38

The performance of the ADC has been measured by adding a 1 kHz tone through a coupling capacitor to the required 1.16 V DC level generated using potentiometers at the input of the converter. Fig. 8.13 shows the measured performance of the proposed ADC in the single-ended configuration. The spectrum of Fig. 8.13(a) has been measured applying an input signal of 32 mV_{peak} (-20 dB_{FS}). The peak SNDR obtained is 69.6 dB, and 71.2 dB-A when A-weighting is applied. Fig. 8.13(b) shows the measured spectrum for an input signal of -5.5 dB_{FS}, on which the VCO nonlinearity limits the SNDR to 56.6 dB (55.4dB-A). In Fig. 8.13(c) we can observe the SNDR measured for different input levels, referred to the input full-scale (320 mV_{peak}). The dynamic range obtained without and with A-weighting is respectively 93.5 dB and 98 dB-A. The current consumption of this converter is 155 μA powered at 1.8 V.

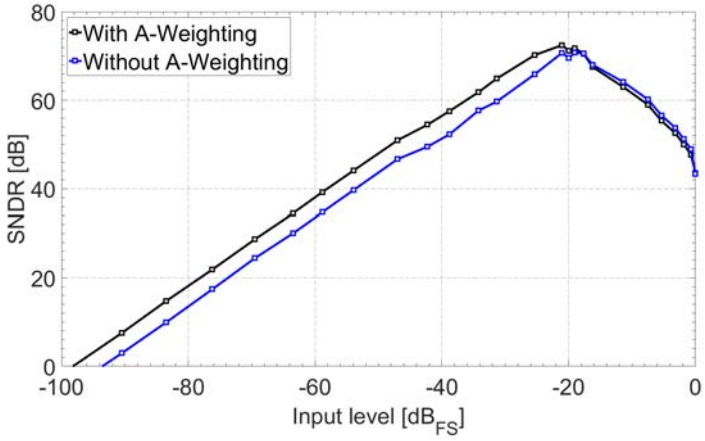
At the cost of doubling the power and the area, the pseudo-differential



(a)

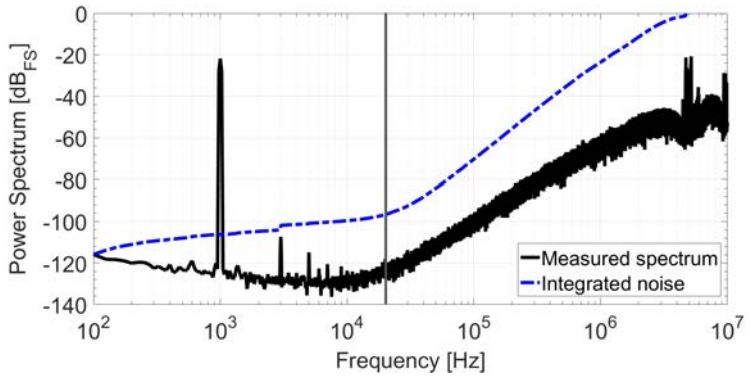


(b)

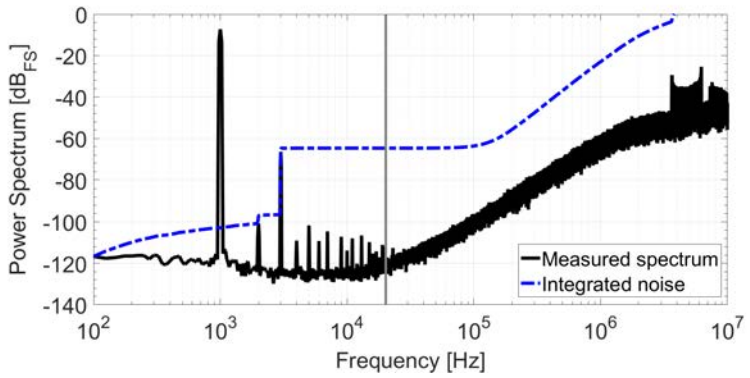


(c)

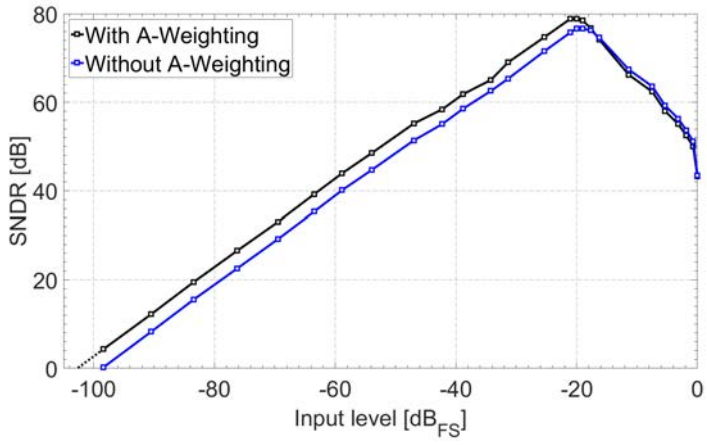
Figure 8.13: Measurements of the single-ended configuration. (a) Measured spectrum at -20 dB_{FS}. (b) Measured spectrum at -5.5 dB_{FS}. (c) Measured SNDR for different input levels.



(a)



(b)



(c)

Figure 8.14: Measurements of the pseudo-differential configuration. (a) Measured spectrum at -20 dB_{FS}. (b) Measured spectrum at -5.5 dB_{FS}. (c) Measured SNDR for different input levels.

configuration has a superior performance, as shown in Fig. 8.14.The SNDR at -20 dB_{FS} (64 mV_{peak}) calculated from the spectrum shown in Fig. 8.14(a) is 76.7 dB (78.9 dB-A). Fig. 8.14(b) depicts the measured spectrum at -5.5 dB_{FS}, on which the SNDR obtained is 59.2$\tilde{d}$B (58dB-A). The dynamic range is also extended to 98.5 dB (103 dB-A), as can be observed in Fig. 8.14(c). As expected, the even harmonics produced by the nonlinearities of the input VCO are canceled because of the differential operation. However, the SNDR for large input signals is still limited by the distortion of the VCOs. Nevertheless, the linearity achieved in both configurations is above 40 dB-A of SNDR for the maximum input level (AOP), making them suitable for low-cost microphones without the need for linearity compensation circuits.

It can be observed that, in addition to the even harmonics compensation, the differential configuration also reduces the low frequency noise that is visible in Fig. 8.13(a) below 1 kHz. This noise comes from the coupling of power supply noise to the input of both VCOs through the off-chip common mode generator that produces the 1.16 V. As this noise is added directly to both inputs, the single-ended configuration is very sensitive to power supply noise, whereas in the differential configuration it is attenuated by the common-mode rejection ratio (CMRR). We have measured this ratio by connecting the input of both channels to a 100 mVpp sine wave at 1 kHz and quantifying the attenuation observed at the differential output. The resulting CMRR is 52.3 dB, which can be improved by enhancing the matching between both VCOs, as shown in Fig. 8.15. In this graph we display the CMRR obtained for different values of the correction factor $g_{matching}$, which has be used to calculate the output sequence as follows: $y_{diff}[n] = y_p[n] \cdot g_{matching} - y_n[n]$. It can be observed that the CMRR can reach above 87 dB with the appropriate matching between the two VCOs.

The achieved Schreier figure-of-merit (FoM) [10], which is defined as $FoM_S = DR + 10\log_{10}(BW/P)$, is 172 dB for the single-ended modulator and 174 dB for the pseudo-differential converter. Table 8.5 shows a summary of the key parameters obtained in this chip in comparison with the result of other audio converters reported in the last years. While the measured DR and FoM_s are in par with other works, the area occupied

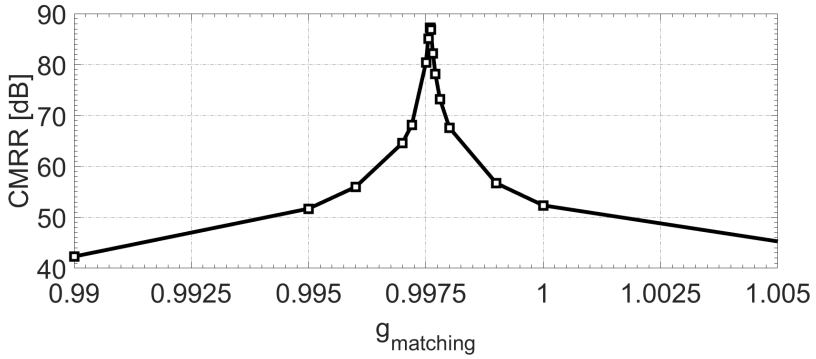


Figure 8.15: CMRR for different mismatch gain correction factors.

by our design is significantly smaller that most of them. The only papers in this selection with similar areas are [93] and [94], which were implemented in modern technologies (40 nm and 28 nm respectively).

8.5 Conclusion

In this chapter we have presented a second-order oscillator-based ΣΔ modulator with single-bit PRIs in 0.13 μm CMOS technology. This ADC is aimed for low-cost audio application, on which silicon area reduction is priority. The proposed converter consists of oscillators and digital circuitry, applying the concept of phase referenced integrators to replace classical integrators and DACs. In consequence, neither operational amplifier nor highly-linear circuits are required.

In contrast to the multi-bit architecture presented in Chapter 7, the converter proposed in this chapter has been implemented using single-bit up-down counters. The resulting system is considerably simpler and it allows the gate level design of the digital circuitry in order to avoid the malfunctions detected in the previous prototype.

The resulting chip works both as a single-channel converter and in a pseudo-differential configuration. The single-channel system reaches 71.2 dB-A of peak SNDR, 98 dB-A of dynamic range, and 155 μA of current consumption. The pseudo-differential system has 78.9 dB-A of peak SNDR, 103 dB-A of dynamic range, and it consumes 310 μA. The area occupied by each channel is 0.02 mm^2 (i.e., 0.04mm^2 for the pseudo-

differential architecture), which is significantly smaller than most of audio converters with similar performance.

Part IV

Conclusion

CHAPTER 9

Conclusions and future work

This work is a survey of the opportunities to develop oscillator-based data converters for audio applications. In particular, we have studied different options for digitizing sound pressure variations combining capacitive MEMS microphones with oscillator-based $\Sigma\Delta$ modulators.

The first architecture considered is the connection of the capacitive sensor as the load of an oscillator in order to control its oscillation frequency through the sensor capacitance. This approach is very appealing because it does not require the biasing circuitry that is typically used in existing microphone readout circuits. However, our feasibility analysis has shown that MEMS parasitics limit the performance of this implementation. As a consequence, we decided to focus on the development of efficient analog-to-digital converters, considering that the MEMS is connected to a biasing circuitry that provides an analog signal, as is done in existing readout circuits. The ADC topology that we have considered is a high-order oscillator-based $\Sigma\Delta$ modulator. This kind of systems can be designed based on the equivalence between a classical integrator and phase referenced integrators built combining oscillators with digital circuitry. The resulting integrator presents potential advantages such as lower supply voltage, compact footprint, and scalability in modern technologies. In this work, we have proposed different implementation alternatives to overcome some of the challenges of this architecture, and

we have fabricated and measured two testchips to demonstrate the feasibility of this approach.

We have also worked on the development of simulation and analysis methodologies for different effects that degrade the performance of oscillator-based ADCs. The main limitations of this kind of architectures are phase noise and distortion, which limit the accuracy of the frequency-encoding process. Transient simulations are often used to estimate the influence of these two effects in the converter. However, the computation time required to perform these simulations is too long, specially in some high resolution applications. In consequence, we have developed a simulation method aimed to reduce the computation time and allow the use of iterative algorithms during the design phase. The other impairment studied is clock jitter, whose effects are also a common limitation in classical continuous-time $\Sigma\Delta$ implementation. However, most of the clock jitter analysis available in the literature are aimed at the dominant error sources of specific modulator topologies. In this work we have presented a time-base projection that facilitates the study of the influence of clock jitter in any modulator topology without loss of accuracy.

In summary, the main contributions of this work are:

I. The feasibility analysis of capacitance-controlled oscillators for the readout of capacitive MEMS presented in Chapter 2. We have studied the parasitics due to the MEMS construction and its connection with the ASIC. In addition, we have performed a survey of potential capacitance-controlled oscillators, including LC and inductor-less oscillators. We have found that this approach is not efficient for several reasons. The main reason is that MEMS parasitics reduce the sensitivity of the oscillator, which is already insufficient due to the low capacitance variation of the MEMS microphone.

II. The high-order single-loop oscillator-based $\Sigma\Delta$ modulator described in Chapter 4. We have used the phase referenced integrator model of a VCO-counter unit as described in Chapter 3 to propose a novel $\Sigma\Delta$ modulator. The proposed architecture can be implemented using only oscillators, DACs, and digital circuitry, which can be very efficient in area, specially in modern technologies.

III. The input referred phase noise model and the simulation strategy presented in Chapter 5. Although phase noise has been intensively studied during several decades, previous analysis of the influence of phase noise in oscillator-based modulators are restricted to certain modulator topologies. In contrast, the methodology presented in Chapter 5 can be applied to any oscillator regardless its post-processing. We also described a simulation strategy to estimate the SNDR of an oscillator-based converters very efficient in time, which can be easily combined with iterative algorithms and optimization tools.

IV. The time-based projection proposed in Chapter 6 for the study of clock jitter in continuous-time $\Sigma\Delta$ modulators. This approach allows the modeling of clock jitter as additive noise without loss of accuracy, and can be applied to almost any modulator topology. This method is potentially advantageous to study the influence of clock jitter in certain modulator topologies that can not be easily analyzed using existing methods, such as oscillator-based converters or band-pass modulators.

V. The experimental validation of II through the design and implementation of a second-order VCO-based $\Sigma\Delta$ modulator with single-bit interstage connection presented in Chapter 8. In this case, the interconnection between the first and the second stage was single-bit, which allowed the simplification of the digital circuitry to avoid the problems described in Chapter 7. The resulting integrated circuit achieved the expected performance, reaching 103 dB-A of dynamic range in the pseudo-differential configuration. Although the power consumption and the figure-of-merit was slightly worse than other converters reported during the last years, the silicon area occupied by the pseudo-differential converter was approximately 0.04 mm^2, which is significantly smaller than most of audio converters with similar performance.

Finally, we would like to propose several ideas that may be of interest for future research:

- Modification of the MEMS microphone to reduce the parasitics that

difficult its integration with the oscillator. This modifications may include:

  - ◇ Reduction of the membrane and backplate resistance using different materials in the construction of these structures. Alternatively, a conductive coating may be deposited over both structure to reduce its equivalent resistance.
  - ◇ Reduction of the interconnection parasitics by fabricating a monolithic MEMS with the readout circuit implemented in the same chip as the MEMS sensor.

- Design and implementation of a fourth-order VCO-based ΣΔ modulator, including an analysis of the noise contribution of each stage in terms of phase noise and phase quantization noise.
- Design of a power-efficient input stage for the pseudo-differential VCO-based ΣΔ presented in Chapter 8 compatible with both SBP and DBP MEMS.
- Complete integration of the simulation strategy described in Chapter 5 into the optimization tools currently available in design environments.
- In-depth study of the influence of clock jitter in oscillator-based ΣΔM and band-pass ΣΔM using the time-base projection presented in Chapter 6.

Appendices

APPENDIX A

Performance metrics for audio ADCs and sensors

The competitiveness of a sensor application is given by several factors. On one hand, the cost of the sensor is mainly determined by the fabrication costs such as silicon area, technology, package cost, complexity and cost of the sensing element, etc. On the other hand, the performance of the sensor depends on the resolution achieved and on the power consumed by the system. Here, we will explain the relevant parameters related to MEMS microphones.

One of the main nonidealities that limit the resolution of the sensor is distortion. The nonlinear operation of some stages of the system causes the appearance of harmonic components at frequencies multiple of the input signal. The two parameters commonly used to quantify the distortion present on the output signal for a sinusoidal input tone are the total harmonic distortion (THD) and the signal to distortion ratio (SDR). The THD is given by the following expression:

$$THD = \frac{\sum_{h=2}^{+\infty} V_{h \cdot f_{in}}^2}{V_{f_{in}}^2}, \tag{A.1}$$

where $V_{f_{in}}^2$ is the power of the fundamental tone and $V_{h \cdot f_{in}}^2$ is the power

of the h-th harmonic. The THD is typically expressed in percentage. In contrast, the SDR is given in decibels, and follows

$$SDR = 10\log_{10}\frac{V_{f_{in}}^2}{\sum_{h=2}^{+\infty} V_{h\cdot f_{in}}^2} = -10\log_{10}(THD). \tag{A.2}$$

Another nonideality that degrades the performance of the system is noise, which appears in the output spectrum spread over a wide range of frequencies. The signal to noise ratio is expressed in decibels and can be calculated using the following equation:

$$SNR = 10\log_{10}\frac{V_{f_{in}}^2}{\int_{BW_{lo}}^{BW_{hi}} V_n^2(f)df} \tag{A.3}$$

where BW_{lo} and BW_{hi} are respectively the lower and the upper limit of the band of interest (we assume that the noise out of this band will be digitally filtered in a post-processing stage), and $V_n(f)$ is the power spectral density (PSD) of the noise. Variants of the SNR are commonly used to limit the noise contribution taken into account in the calculation of this metric. For example, the SQNR refers to the signal to quantization noise ratio, on which only the noise added in the quantization process is considered. Another common metric is the signal to noise and distortion ratio (SNDR), which is given by the following expression:

$$SNDR = 10\log_{10}\frac{V_{f_{in}}^2}{\sum_{h=2}^{+\infty} V_{h\cdot f_{in}}^2 + \int_{BW_{lo}}^{BW_{hi}} V_n^2(f)df}. \tag{A.4}$$

All these metrics depend on the input signal, and must be always given indicating the input level used to calculate them. Conversely, there are other parameters used to quantify the system performance that are independent of the input level. For example, the dynamic range (DR) represents the range of input levels for which the resolution of the sensor reaches the specifications considered acceptable in that particular application. Figure A.3 illustrates an example of a dynamic range plot on which the SNDR is plotted for different input levels. The dynamic range is the difference in decibels between the maximum input level (typically

limited by distortion or stability issues) and the minimum input level (limited by the noise floor of the system).

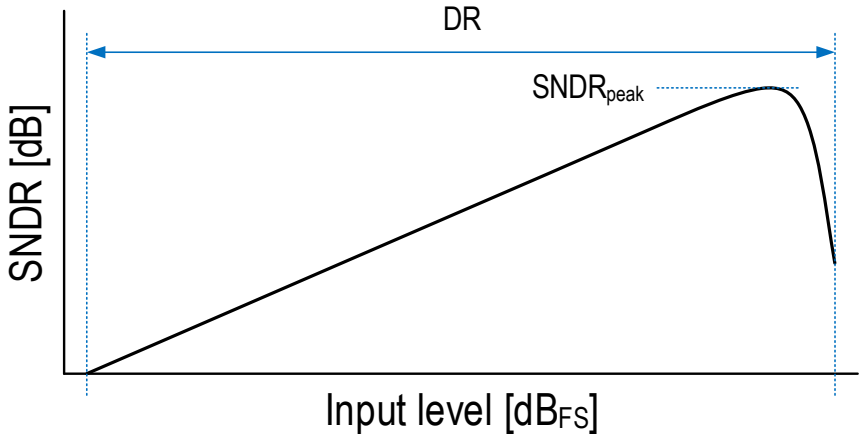


Figure A.1: Example of a dynamic range plot.

Finally, the following two figures-of-merit (FoM) are commonly used to quantify the competitiveness of an ADC in terms of performance and power consumption. On one hand, the FoM derived from the work of Robert Walden [97, 98] is defined as:

$$FoM_W = \frac{P}{2BW \cdot 2^{\frac{DR-1.76}{6.02}}}, \tag{A.5}$$

where P is the power consumption and BW is the bandwidth of the converter. On the other hand, the Schreier FoM presented in [10] is defined as:

$$FoM_S = DR + 10\log_{10}(BW/P). \tag{A.6}$$

A popular variation of these FoMs [99, 100] replaces the DR by the $\text{SNDR}_{\text{peak}}$, which is the maximum SNDR obtained for the whole range of input levels.

A.1 Considerations for audio acquisition systems

In the particular case of audio acquisition systems, there are a few additional consideration that must be taken into account. Firstly, the input level is determined by the sound pressure level (SPL) which is measured in dB_{SPL}. The reference sound level (0 dB_{SPL}) corresponds to a pressure variation of 20 μPa_{rms}, which is considered closed to the threshold of human hearing. Furthermore, in some applications it is common to apply A-weighting to the output spectrum before calculating the SNR, SNDR, and DR. A-weighting is a filtering that mimics how the sensitivity of the human ear changes over frequency. Figure A.3 shows the gain of the A-weighting filter for different frequencies in the range from 20 Hz to 20 kHz. Note that most of the attenuation occurs at low frequencies. The reference input frequency commonly used in this kind of application is 1 kHz, frequency at which the gain of the A-weighting filter is nearly 0 dB. In order to differentiate whether we are applying A-weighting or not, we use dB-A instead of dB to express the SNR/SNDR/DR of a system when it has been calculated using A-weighting.

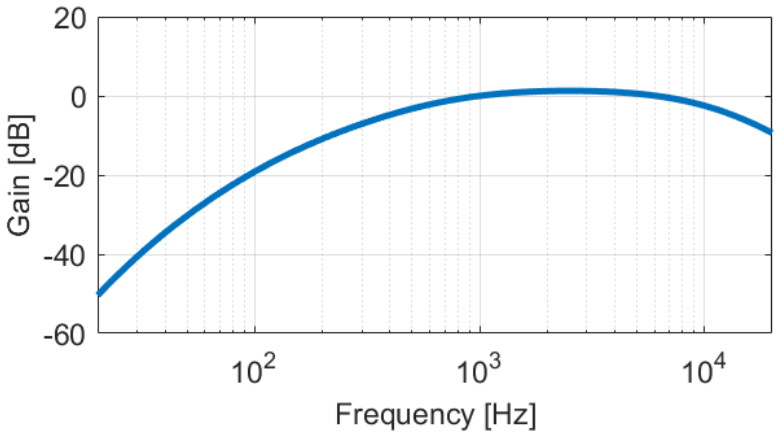


Figure A.2: A-weighting transfer function.

The acoustic overload point (AOP) is the maximum acoustic level for which the performance of the system is considered acceptable, which is in most of the cases limited by distortion. The level of distortion accepted depends on the specific audio application, and is typically between 20

and 40 dB of SNDR. Therefore, in contrast to what is common in other applications, the dynamic range plot of a microphone can have a wide region on which distortion dominates over noise, as shown in Figure A.3. In addition to the $\text{SNDR}_{\text{peak}}$, the AOP and the DR, we have marked the SNDR at 94 dB_{SPL} (i.e., with a pressure variation of 1 Pa_{rms}) which is a reference amplitude commonly used in microphones.

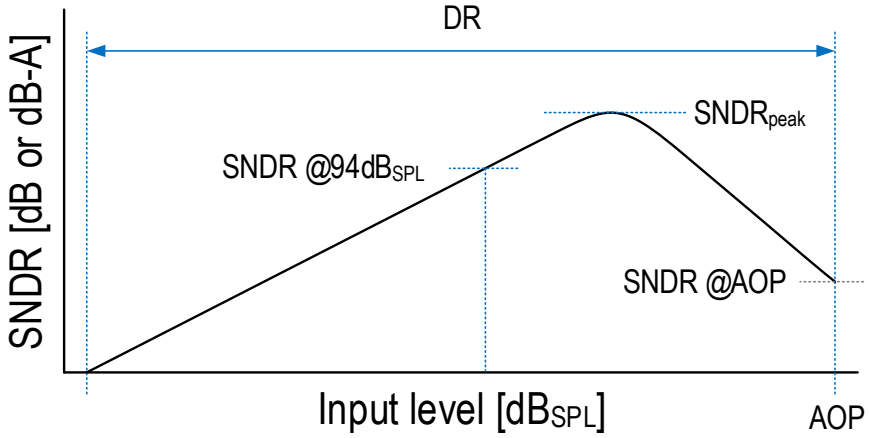


Figure A.3: Typical dynamic range plot in audio acquisition systems.

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